Graphene nanoribbon based negative resistance device for ultra-low voltage digital logic applications

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Negative resistance devices offer opportunities in design of compact and fast analog and digital circuits. However, their implementation in logic applications has been limited due to their small ON current to OFF current ratios (peak to valley ratio). In this paper, a design for a 2-port negative resistance device based on arm-chair graphene nanoribbon is presented. The proposed structure takes advantage of electrostatic doping, and offers high ON current ($\sim$700 μA/μm) as well as ON current to OFF current ratio of more than 10^5. The effects of several design parameters such as doping profile, gate workfunction, bandgap, and hetero-interface characteristics are investigated to improve the performance of the proposed devices. The proposed device offers high flexibility in terms of the design and optimization, and is suitable for digital logic applications. A complementary logic is developed based on the proposed device, which can be operated down to 200 mV of supply voltage. The complementary logic is used in design of an ultra-compact bi-stable switching static memory cell. Due to its compactness and high drive current, the proposed memory cell can outperform the conventional static random access memory cells in terms of switching speed and power consumption. © *2013 American Institute of Physics*.
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Negative resistance devices are popular in analog applications such as oscillators, mixers, frequency converters, and impedance cancellation circuits. The Esaki tunnel diode—which is composed of a degenerately doped p-n junction with a width of $\sim$10 nm—is the widely used negative resistance device.[1] The Esaki diode exhibits negative resistance between the so-called *peak* and *valley* points on the current-voltage curve.[2] Due to the relatively small peak to valley current ratio (PVCR), these diodes are deemed unsuitable for digital applications.[3] The low PVCR of Esaki diodes is attributed to the existence of deep trap states in the highly doped regions of the semiconductor, which leads to high *excess* current.[2]

In this paper, we propose a negative resistance device based on arm-chair graphene nanoribbon (GNR), which exhibits high PVCR making it suitable for digital applications. The proposed device takes advantage of the electrostatic doping of GNR, which circumvents the possible introduction of trap states through doping. The proposed device works on the principle of tunneling similar to the Esaki diode. The highly improved characteristics for the proposed device are achieved by the device design and the superb characteristics of the GNR. GNRs exhibit several key advantages over conventional semiconductors. GNRs have a highly tunable bandgap (E_g), which provides flexibility in device design.[4] GNRs are ultra-thin (0.34 nm), which leads to perfect electrostatic control of gate over channel. Furthermore, due to their pristine nature, GNRs have less surface defects compared to conventional materials. Due to their superior properties, GNRs have become very attractive to the electronics community and in design of metal-oxide-semiconductor field-effect transistors (MOSFETs),[5,6] and tunneling field effect transistors.[7,8] Moreover, patterned GNRs have been exhibited experimentally with sub-10 nm width.[9–11]

The proposed device structure is shown in Fig. 1 in a 3D view, and in top view in Fig. 2(a). The GNR consists of narrow source and drain regions (with width W_{SD}) and a wide intrinsic channel (with width W_{Ch}). The width of each section determines the GNR bandgap. The source and drain regions are heavily n- and p-doped, respectively, and their respective lengths are denoted by L_S and L_D. The doping in GNR can be accomplished by either a chemical doping or an electrostatic doping through extra gate electrodes (not shown in the figure).[12–15] A bottom gate (BG) and a top gate (TG) cover the channel area with lengths L_{BG} and L_{TG} as shown in Fig. 2(a). In this paper, we set $L_S = L_D = L_{TG} = L_{BG} = 5$ nm,

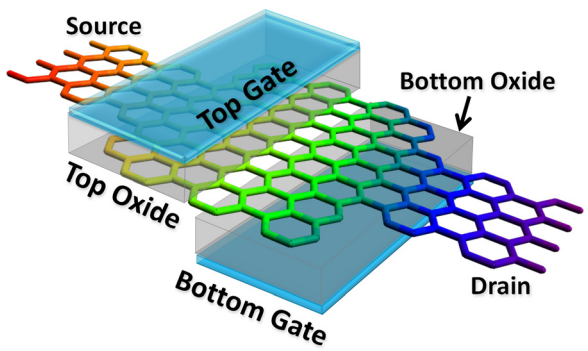

FIG. 1. Schematic illustration of the proposed negative resistance device. The device consists of a GNR semiconductor, bottom oxide and bottom gate, and top oxide and top gate, each covering half of the channel. The GNR consists of doped source and drain regions and an intrinsic channel region (as shown in Fig. 2(a)). The carbon rings are shown for illustrative purposes and do not represent the actual dimensions for the device.

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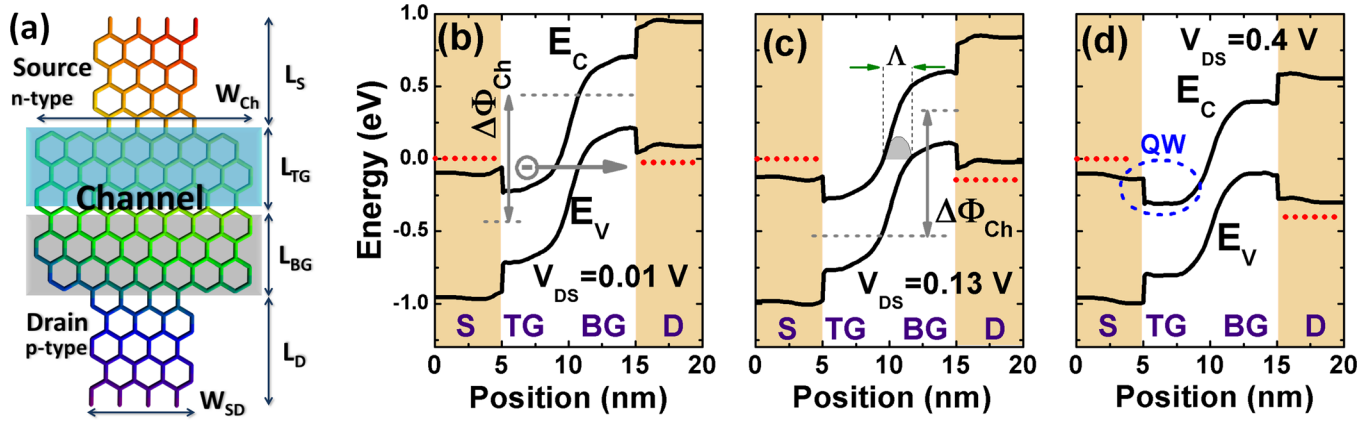

FIG. 2. (a) Schematic top view of the proposed negative resistance device in Fig. 1 and band diagram in GNR for V_{DS} of (b) 0.01 V, (c) 0.13 V, (d) 0.4 V. Source and drain regions are denoted by S and D, respectively. The channel is divided into two regions. TG represents the half of the channel under the top gate, and BG represents the half of the channel over the back gate. Conduction and valence bands are shown by E_C and E_V, respectively. The potential difference at the two ends of the channel is denoted by $\Delta\Phi_{Ch}$. A schematic illustration of the potential barrier for tunneling is shown in (c) with the shaded region with Λ as the width of the barrier. The quantum well formed at the left side of the channel is shown by QW in (d). Maximum current is observed in (c), where the E_F at source and drain aligns approximately with E_V at drain and E_C at source, respectively. The WF for BG and TG electrodes is 5.2 eV, and for the GNR is 4.5 eV with $V_{TG} = 1.2$ V. We can choose a lower value for V_{TG} using a lower WF for the TG electrode.

and W_{SD} and W_{Ch} are varied to tune the E_g. An effective oxide thickness of 1 nm is considered. Each gate controls the channel potential under the corresponding gate electrode. The bottom gate electrode is tied to the drain electrode, and a fixed voltage is applied to the top gate. A voltage is applied to the source and drain electrodes, and the device is used in a 2-port configuration.

The simulation of the device is carried out by an in-house ballistic device simulator,[16] which uses a self-consistent approach to solve the Poisson and Schrodinger equations within the non-equilibrium Green's function (NEGF) formalism in real space.[17] A tight binding Hamiltonian with an atomistic p_z orbital basis set is used for GNR with coherent transport. We have assumed hydrogen passivated edges for the GNR, and the ballistic simulations are done at room temperature. The gate leakage current and the edge roughness of GNR are not included in the simulations. This is because the gate leakage can be kept low by choosing a high-k dielectric, and by reducing L_{TG} and L_{BG}. The edge roughness can lead to creation of states in the forbidden gap region, which can degrade the performance. However, the recent demonstrations of fabricated GNRs with atomically smooth edges[18,19] provide credible evidence of realizing such GNRs in the near future. Moreover, the possible introduction of trap states in GNRs from oxide deposition can be suppressed by incorporation of multi-layer graphene[20] or an oxide with atomically smooth surface such as hexagonal boron nitride.[21]

The band diagram of a sample device is shown in Fig. 2 for different values of the drain-source voltage (V_{DS}). In Fig. 2, the bandgap in the source and drain regions ($E_{g,SD}$) is 0.86 eV corresponding to $W_{SD} = 1.7$ nm. The channel bandgap ($E_{g,Ch}$) is 0.5 eV with $W_{Ch} = 2.8$ nm. A constant voltage is applied to the top gate such that in equilibrium ($V_{DS} = 0$ V), the conduction band (E_C) in the left half of the channel is below the E_C at source. The value of the applied top gate voltage (V_{TG}) depends on the workfunction (WF) of the gate material with respect to the WF of the GNR, and can be varied to tune the performance of the device as will be discussed later. The bottom gate is tied to the drain electrode and its WF is chosen such that the valence band (E_V) in the right side of the channel is above the E_V at drain (see the Fig. 2 caption for detailed values). The I-V characteristics of the device in Fig. 2 are shown in Fig. 3 (line 4) and in Fig. 4 with the solid line and will be discussed in conjunction with the band diagram.

In Fig. 2(b), the band diagram is shown for $V_{DS} = 0.01$ V. In this case, the Fermi level (E_F) of drain is 0.01 eV lower than the E_F at source, and a narrow tunneling junction is formed in the middle of the channel through which the electrons tunnel across the junction contributing to a net current flow from drain to source. The qualitative behavior of the device can be understood by assuming a constant electric field at the junction, which leads to a potential barrier for tunneling as schematically shown with the shaded region in Fig. 2(c). This leads to the Wentzel–Kramers–Brillouin (WKB) tunneling probability within the electron-hole duality picture:[22]

$$T_{WKB} = \exp\left(\frac{-\pi E_g^2}{4e\hbar v_F F}\right), \quad (1)$$

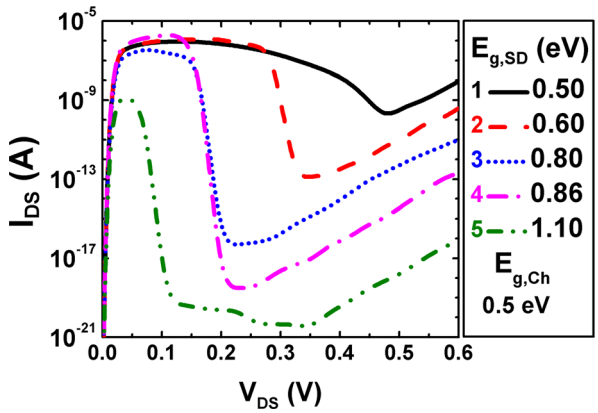

FIG. 3. Current-voltage (I-V) characteristics of the proposed negative resistance devices. $E_{g,Ch} = 0.5$ eV, and $E_{g,SD}$ varies between 0.5 eV and 1.1 eV. A peak and a valley point are observed on each curve and marked in Fig. 4. The gate WF and V_{TG} are the same as in Fig. 2.

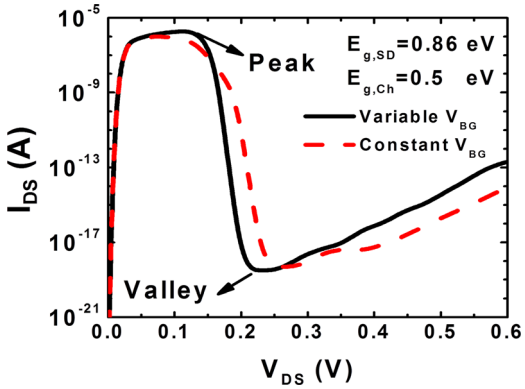

FIG. 4. Current-voltage characteristics for the proposed negative resistance device with two design approaches: variable V_{BG} and constant V_{BG}. In variable V_{BG} design, the BG electrode is tied to the drain electrode, while in the constant V_{BG} design, a constant voltage is applied to the BG. The variable V_{BG} approach offers improved characteristics. The peak and valley points are marked on the curve. The gate WF and V_{TG} are the same as in Fig. 2.

where $F = E_g/e\Lambda$ is the electric field, Λ is the horizontal spacing between E_C and E_V at each energy level, e is the unit electronic charge, v_F is the Fermi velocity in graphene, and $\hbar$ is the reduced Planck's constant. The purpose of this qualitative picture is to provide intuitive insight into the behavior of the proposed devices. We note that in our simulations, we implement a NEGF solver, which takes the actual shape[22] of the potential barrier as well as the quantum capacitance into account, and the WKB approximation is not required.

The tunneling current depends on T_{WKB}, the density of states, the Fermi levels at the two sides of the tunneling junction and the energy window (EW) over which the tunneling is allowed,[3,23] and can be increased by application of a positive V_{DS}. From Eq. (1), it can be observed that the tunneling probability is a strong function of E_g and Λ. A variation of the WF of TG/BG or V_{TG} and V_{BG} leads to a variation of the potential difference at the two ends of the channel denoted by $\Delta\Phi_{Ch}$ (Fig. 2(c)). A higher value of $\Delta\Phi_{Ch}$ leads to a higher F and a lower Λ at the junction, and thereby to a higher tunneling probability. Therefore, the tunneling probability can be tuned by the gate electrodes. It can be observed from this qualitative picture that the tunneling current can be increased by reducing the channel bandgap, by reducing Λ (increasing $\Delta\Phi_{Ch}$) or by increasing the energy window (through V_{DS}).

As the drain voltage increases, the EW increases, which leads to a higher tunneling current. The band diagram of the device for $V_{DS} = 0.13$ V is shown in Fig. 2(c), which is the bias voltage for the *peak* current observed (see Fig. 4). Due to the larger EW, a higher tunneling current flows through the device compared to Fig. 2(b). The smaller value of $\Delta\Phi_{Ch}$ leads to a reduction of the tunneling current. However, the effect of the larger EW is more prominent, which leads to an overall increase of the current.

A further increase of V_{DS} beyond 0.13 V leads to a smaller tunneling current as shown in Fig. 4. Fig. 2(d) shows the band diagram for the device for $V_{DS} = 0.4$ V. It can be observed that the potential difference at the drain-channel junction is approximately the same as in Fig. 2(b). This is due to the application of the same voltage to both the drain and bottom gate electrodes, which subsequently leads to a smaller $\Delta\Phi_{Ch}$. In Fig. 2(d), the tunneling current is blocked by the forbidden gap at the source and drain regions. In addition, due to the lower value of $\Delta\Phi_{Ch}$ at the tunneling junction, the tunneling current is further reduced compared to Fig. 2(c). Therefore, the proposed device exhibits a negative resistance behavior. Further increase of V_{DS} leads to a rise in the current due to the diffusion of carriers between the source and the drain, which is widely discussed in forward biased p-n junctions.[3] The phonon assisted tunneling current is not included in this work, and may degrade the device characteristics. However, the degradation is expected to be small due to weak electron-phonon interactions in graphene.

The I-V characteristics of the proposed device is shown in Fig. 3, where the $E_{g,Ch}$ is fixed at 0.5 eV and the $E_{g,SD}$ is varied between 0.5 eV and 1.1 eV. A doping with an effective molar fraction (the ratio of doping-induced charge density to carbon atom density) of 0.003 per atom in the source/drain regions is considered. At zero bias, the proposed devices show zero current flow. As the V_{DS} increases, the I_{DS} increases and reaches a peak value (I_{Peak} or I_{ON} at V_{Peak}). Further increase of V_{DS} leads to lower current until the current reaches a minimum called the valley current (I_{Valley} or I_{OFF} at V_{Valley}) due to the reduced tunneling current. The peak and valley points are marked in Fig. 4. Eventually, the I_{DS} increases with a slope of ~60 mV/dec, where the device behaves similar to a forward biased diode. It can be observed that the PVCR can be improved to values as high as 10^{14}. We note that the inclusion of gate leakage current can degrade these values, but due to the small gate length, the PVCR is expected be very high. For $E_{g,SD} = 0.5$ eV, the device consists of a homo-junction GNR. In this case, a PVCR of $> 10^3$ is observed. As $E_{g,SD}$ increases, the diffusion current becomes smaller due to the blocking of the carriers by the higher bandgap at source/drain regions. It can be observed that the increase of $E_{g,SD}$ leads to the reduction of V_{Valley}, which is due to the steeper drop in the tunneling current for $V_{Peak} < V_{DS} < V_{Valley}$ and due to the reduction of the diffusion current.

Three main factors contribute to the steepness of the current drop between the peak and valley points: the change of Fermi level position at source/drain with bandgap (or width), the blockade of carrier tunneling by the higher bandgap, and the formation of quantum wells in the channel. For a higher bandgap at source/drain, the relative position of E_F with respect to E_C (E_V) at source (drain) reduces, which leads to a lower energy window, a lower tunneling current, and a steeper current drop. Furthermore, a higher value of $E_{g,SD}$ leads to a faster blockade of carriers at source/drain regions as V_{DS} increases, which leads to a steeper drop in the tunneling current. The height of the QW (Fig. 2(d)) depends on the bandgap difference between source/drain and the channel and the gate electrode bias. A higher QW height leads to a higher quantization of energy states (lower DOS) in the QW, which subsequently leads to a reduced tunneling current. The reduced tunneling current (from higher $E_{g,SD}$) also affects the I_{peak}. It can be observed from Fig. 3 that, the I_{Peak} reduces by a factor of 10^4 as $E_{g,SD}$ increases from 0.86 eV to 1.1 eV. We note that although an increase of $\Delta\Phi_{Ch}$ (by tuning the gate WF and V_{TG}) can lead to a lower tunneling barrier width, it also increases the height of the QW which can lead to an overall smaller tunneling current.

Therefore, the gate WF and V_{TG} must be chosen carefully for device optimization.

Another possible design is to apply a constant voltage to the back gate electrode. We refer to this design as the constant V_{BG}, and refer to the design discussed earlier as the variable V_{BG}. In the constant V_{BG} design, the electric potential difference at the drain-channel junction is no longer constant, but varies with the increase of the drain-source voltage bias. This leads to a $\Delta\Phi_{Ch}$ considerably higher than that in the variable V_{BG} design. In Fig. 4, the *I-V* characteristics for the constant V_{BG} and variable V_{BG} designs are shown for a device with $E_{g,Ch} = 0.5\,\text{eV}$ and $E_{g,SD} = 0.86\,\text{eV}$. The gate WF is the same for both devices. Therefore, at $V_{DS} = 0$, both devices exhibit similar behavior. However, the constant V_{BG} design exhibits smaller peak current and a higher value of V_{Valley}. The smaller I_{Peak} is due to the modification of the DOS in the quantum wells formed in the channel. The increased value of V_{Valley} is due to the higher electric field at the tunneling junction, which leads to a less steep drop in the current between the peak and valley points.

The device discussed earlier shows the characteristics of an n-type device. Next, we discuss the complimentary p-type device, which in combination with the n-type device will be used in design of an ultra-compact and low-voltage static memory cell. The p-type negative resistance device uses the same structure and gate WF values as the n-type device. The only differences are that the n-type region is called drain and the p-type region is called source, and the drain electrode is connected to the TG terminal while a constant voltage is applied to the BG terminal. The schematic illustrations of the n-type and p-type devices are shown in Fig. 5. In the p-type device, for $V_{DS} = -0.01\,\text{V}$, the band diagram is exactly the same as in Fig. 2(b). As V_{DS} reduces to more negative values, the tunneling current increases due to the larger energy window. Then the current reaches a maximum value, and starts reducing to the valley point. For lower values of V_{DS}, the current increases again due to the diffusion of carriers similar to a forward biased p-n junction diode.

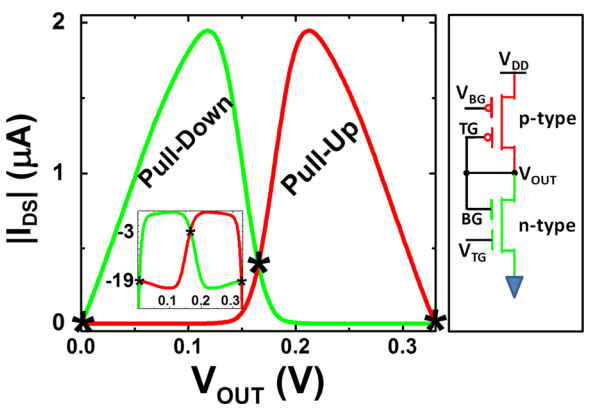

FIG. 5. I-V characteristics and implementation of a bi-stable static memory cell based on the proposed negative resistance devices. The n-type device corresponds to the pull-down network, and the p-type device corresponds to the pull-up network. An arbitrary value of $V_{DD} = 0.33\,\text{V}$ is chosen for the cell. The two curves cross at 3 points marked by *stars*. The inset shows $\log_{10}(I_{DS})$ vs. V_{OUT}. The peak current is $\sim 700\,\mu\text{A}/\mu\text{m}$ for $E_{g,Ch} = 0.5\,\text{eV}$, and can be further increased by lowering $E_{g,Ch}$.

The value of V_{Valley} determines the minimum power supply voltage that can be used to operate the devices. The gate WF and V_{BG} can be adjusted to tune the performance of the devices. With the proposed designs, the n- and p-type devices have similar structures, and the p-type device can be fabricated by a simple tweaking of the n-type device. This simplifies the fabrication process and lowers the cost of processing for the proposed devices.

Next, we discuss a bi-stable static memory circuit based on the proposed negative resistance devices. We use a complimentary logic based on one n-type and one p-type device to build a static memory cell as shown in Fig. 5. The source of the p-type device is connected to $V_{DD} = 0.33\,\text{V}$, and the source of the n-type device is connected to the ground. The drain electrodes of the devices are connected to the output node. The output node is also connected to the top gate of the p-type device and the bottom gate of the n-type device as discussed earlier. The output node stores the data being 0 or 1. The I_{DS} for both the devices is shown in Fig. 5 as a function of V_{OUT} on a linear scale and in the inset in a log-linear scale. The n-type device is much stronger than the p-type device in the left half of the I-V curve, and pulls down the output node voltage. The p-type device pulls up the voltage when the state of the device is in the right half of the I-V curve. There are 3 points where the two curves cross each other, and are marked by the *stars* on the figure. The points at $V_{OUT} = 0$ and 0.33 V are the stable points, while the middle point is unstable. If the device is biased at $V_{OUT} \sim 0\,\text{V}$, and V_{OUT} increases to a value less than V_{Peak} of the n-device, the n-device supplies much higher current than the p-device and brings V_{OUT} back to ~ 0. Similarly, the p-device keeps the V_{OUT} at $\sim V_{DD}$. Therefore, the proposed circuit can be used as a bi-stable switching cell.

The stable value of V_{OUT} at left (right) of the I-V curve depends on the magnitude of the I_{DS} of the p-type (n-type) device at $V_{DS} = V_{DD}$. The reason is that the current in both devices (referred to as leakage current, $I_{Leakage}$) must match. So, the output voltage adjusts itself until the currents of the 2 devices become equal. Due to the high PVCR in the proposed devices, the devices exhibit ultra-low current around the valley point, which leads to ultra-low leakage current and full rail-to-rail swing at the output node. For example, in the device considered in Fig. 5, the leakage current is on the order of 10^{-18} A. Another advantage of the proposed design is the flexibility in selection of V_{DD}. Basically, the bi-stable circuit works for any value of V_{DD} larger than V_{Valley} provided that the leakage current is smaller than the peak current. The optimum value of V_{DD} is V_{Valley}, because the devices exhibit the lowest current at V_{Valley} ($\geq 200\,\text{mV}$ in Fig. 3). However, if the peak and valley points of the n- and p-type devices do not match, we can choose a higher V_{DD}. Although the leakage current increases with a higher value of V_{DD} due to the diffusion current, the leakage current can be lowered to very small values compared to the peak current (Fig. 3). This provides more flexibility in selection of V_{DD} and adjusting the properties of the bi-stable switch. Furthermore, similar to conventional static random access memory (SRAM) cells, an access transistor can be used to read/write values from/to the cell. We note that the proposed devices can be further modified by choosing a different value of $E_{g,Ch}$ to improve the tunneling current.

In conclusion, we have proposed complimentary designs for 2-port GNR based negative resistance devices. The proposed negative resistance devices exhibit very high peak to valley current ratios ($\sim 10^{14}$), which is essential in digital applications. The devices are highly configurable, and their properties can be adjusted and optimized by the selection of voltages applied and the gate WF values. The fabrication and integration of the proposed n- and p-type devices are simple and cost-effective due to the similarities between their structures. Moreover, we have designed a bi-stable switching memory cell that can be used as an SRAM cell. The proposed memory cell is very compact in terms of area and works at ultra-low voltages and exhibits ultra-low leakage. Due to the high ON current ($\sim 700\ \mu A/\mu m$) supplied by the proposed devices, and due to the compactness of the cell and elimination of extra transistors and capacitances compared to a conventional SRAM cell, we predict that the proposed memory cells can operate at frequencies higher than MOSFET based SRAM cells.

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