2-Dimensional Tunnel Devices and Circuits on Graphene: Opportunities and Challenges

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Abstract: 2-dimensional (2D) electronic materials such as graphene have emerged as attractive candidates for tunnel devices and circuits for achieving ultra-high energy-efficiency. This paper highlights a few novel tunnel device and circuit concepts based on graphene. Major challenges of 2D materials relevant to such applications are discussed as well.

Introduction: As conventional Field-Effect-Transistors (FETs) (**Fig.1(a,c,e)**) approach their limits in controllability of power consumption (mainly due to the "Boltzmann tail" that causes OFF-current, as shown in **Fig. 1(c)**), Tunnel-FETs (TFETs) (**Fig.1(b)**) are being considered as promising candidates for future low-power and energy-efficient logic circuit applications **[1]**, which employ the tunneling of electrons/holes through the semiconductor band gap (E_g) **[2]** (**Fig. 1 (d,f)**) and can switch ON/OFF with subthreshold swing (*SS*) smaller than 60 mV/dec.

Nano-scale TFETs based on conventional 3D materials have a severe scaling issue that the E_g's vary uncontrollably with the bulk dimensions (in nm regime) and thereby cause variations in tunneling currents. However, 2D materials have intrinsic thickness of a few Å/layer (**Fig.2(a)**), and controllable precise band gaps as a function of number of layers, which enable the scaling of TFETs without inducing performance variations. TFETs based on graphene may also utilize the band gap tunability by width variation of graphene (**Fig.2(b),3(a,b)**) to achieve high ON-OFF ratio (I_{ON} /I_{OFF}). Moreover, 2D materials have further advantages in terms of device topology (**Fig. 2(c,d)**), which benefits from excellent electrostatics (due to atomically thin body) and thus high ON-current (I_{ON}, tunneling current in ON state). In addition, the pristine interfaces of 2D materials without dangling bonds can prevent TFETs from being influenced by the interface states (**Fig.2(e,f)**). Besides, while the 3D density of states (DOS) varies as square root of energy and limits the most optimal design of TFETs, 2D DOS is either constant or linear (in case of graphene) with energy (**Fig.2(g)**), which allows more abrupt turn-on in TFETs, as illustrated in **Fig.2(g)**. Hence, in summary, 2D materials, especially graphene (which has outstanding mobility compared with other 2D materials) exhibit high potential for building tunnel devices such as TFETs, and can pave the way for future ultra energy-efficient integrated circuits.

Graphene Tunnel Devices: Band gap opening caused by etching of graphene into graphene nanoribbons (GNRs) (**Fig.3(a,b)**), can be employed to build GNR Tunnel-FETs (GNRTFETs) (**Fig.3(c)**). The GNRTFET's performance is highly dependent on the length and width scaling **[3]**. Channel length scaling leads to significant reduction of I_{ON}/I_{OFF}, increase of I_{OFF} and *SS* due to direct source-to-drain tunneling, while the I_{ON} and I_{OFF} both decrease by scaling the GNR width. Hence, in order to exploit the small E_g of wide-GNR to achieve high I_{ON} and the high E_g of narrow-GNR to attain low I_{OFF}, a hetero GNRTFET (**Fig.3(d), Fig.4**) has been proposed **[4]**. I_{ON} up to 1.3 mA/μm, I_{ON}/I_{OFF} up to 10^9, and *SS* down to 10 mV/dec at V_{DD}=0.5 V were attained (via simulations), which represent 2-fold and 10^4-fold improvement in I_{ON} and I_{ON}/I_{OFF} ratio, respectively, compared to 25-nm CMOS technology.

TFET biosensors have been shown to surpass the performance of conventional FET biosensors by several orders (**Fig.5**). **[5].** Due to the tunability of E_g and thereby the optimization of *SS*, GNRs can also be attractive for making low-power biosensors based on TFETs (**Fig.3(e)**). On the other hand, a recently proposed GNR based negative differential resistance (NDR) device (**Fig.3(f)**) **[6]**, in the form of an Esaki diode, exhibits a peak-to-valley current ratio of 10^5 (**Fig.6**), and operation voltage of 200 mV, which significantly exceeds the performance of conventional Esaki diodes.

Graphene Tunnel Circuits: Graphene is also attractive for novel circuits based on tunnel devices. A unique all-graphene circuit scheme (**Fig.3(g)**) **[7]** has been recently proposed and theoretically explored, in which graphene was employed to fabricate both active (GNRTFETs) and passive (interconnects) devices in a seamless manner. Simulation results summarized in **Fig.7** indicate that the all-graphene logic circuit exhibits better performance from the aspects of static noise margin, inverter gain, minimum delay, and dynamic power consumption, compared to state-of-the-art CMOS technology. Meanwhile the GNR based NDR device in **[6]** can be used in the design of ultra-compact bi-stable static random access memory (SRAM) cell (**Fig.3(h), Fig.8**). Due to the compactness and high drive current, the proposed SRAM can outperform conventional SRAM cells in terms of switching speed and power consumption **[6]**.

Major Challenges: Challenges in applications of graphene in tunnel devices and circuits include material synthesis, lithography, doping and contacts. So far, beside micromechanical exfoliation, although large area mono- and bi-layer graphene growth on metal substrate by chemical vapor deposition has been demonstrated with record mobilities **[8],** wafer-scale growth and transfer remain challenging. Moreover, precise lithography and doping technologies need to be developed to provide feasibility for the above mentioned applications of graphene **[6],[7]**. Additionally, the parasitic contact resistance between metal electrodes and graphene (including both top and edge contacts) is another key factor in device/circuit applications that demands careful attention to device/contact layout **[9],[10]**.

Summary: In this paper, some novel tunnel devices and circuits uniquely enabled by 2D materials (especially graphene) are discussed. Such devices/circuits can open up unprecedented opportunities for next generation ultra energy-efficient electronics. Potential challenges arising from employing 2D materials for such applications are also highlighted.

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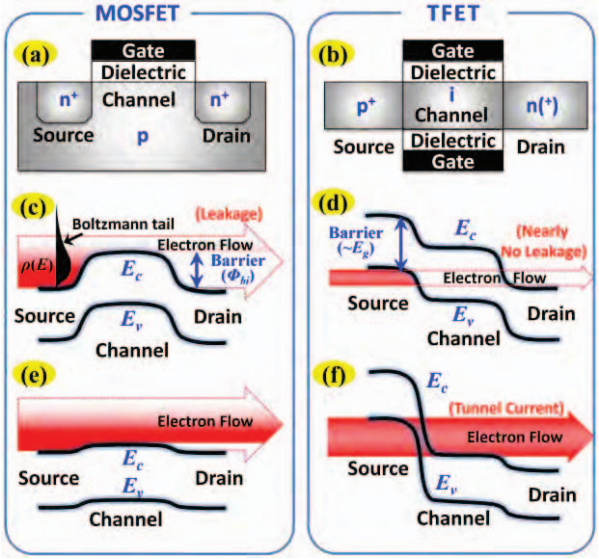

Figure 1. Schematic of **(a)** a typical n-type MOSFET and **(b)** a typical double-gated n-type TFET; Band diagram and electron flow of **(c)** MOSFET and **(d)** TFET in OFF state; Band diagram and electron flow of **(e)** MOSFET and **(f)** TFET in ON state. The red arrows indicate direction of electron flow.

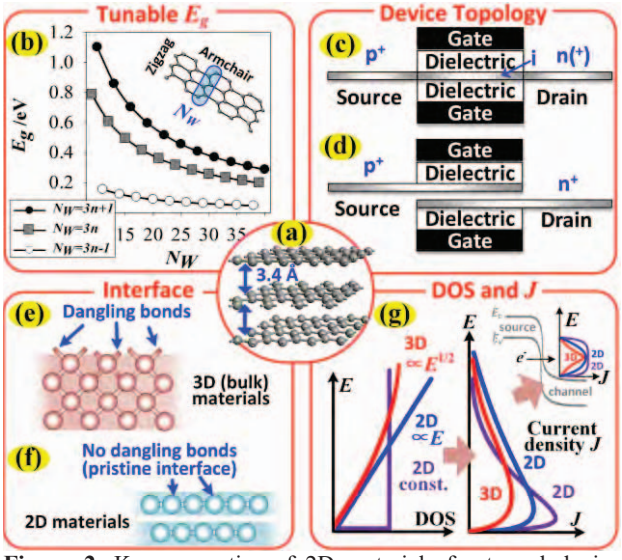

Figure 2. Key properties of 2D materials for tunnel device applications: **(a)** ultra-thin thickness, **(b)** tunable E_g of graphene (armchair chirality), where N_W represents number of C atoms along width direction; **(c,d)** lateral and vertical tunnel device topology; **(e,f)** absence of dangling bonds; **(g)** 2D DOS that cause abrupt turn-on of tunnel current.

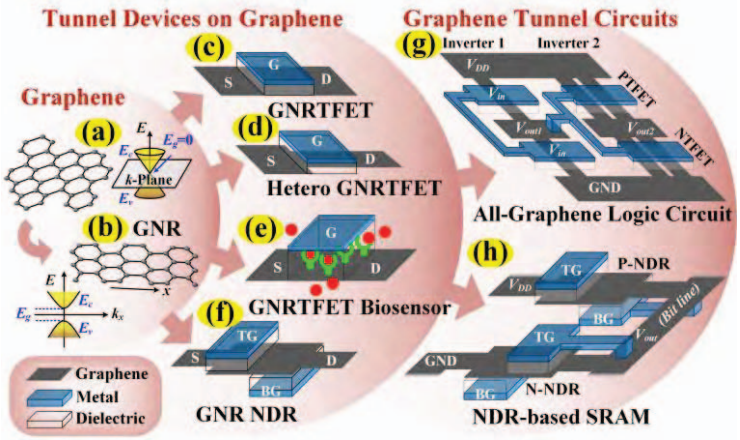

Figure 3. Atomic structure and energy dispersion of **(a)** Graphene and **(b)** GNR; Device structure schematic of **(c)** GNRTFET, **(d)** Hetero GNRTFET, **(e)** GNRTFET biosensor and **(f)** GNR NDR device. Circuit schematic of **(g)** all-graphene circuit (2-stage inverter chain) and **(h)** NDR-based SRAM cell.

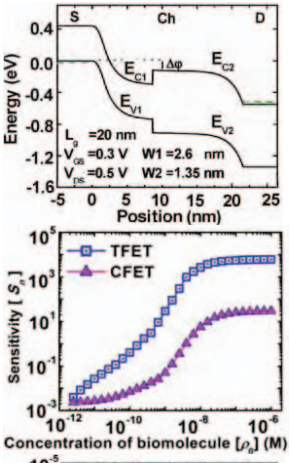

Figure 4. Band diagram of the hetero GNRTFET in Fig.3(d) in the ON state. The low E_g near source (W1) enhances I_{ON}, and the high E_g near drain (W2) reduces I_{OFF}.

Figure 5. Sensitivity of TFET and conventional FET (CFET) for sensing of biomolecules as a function of biomolecule concentration.

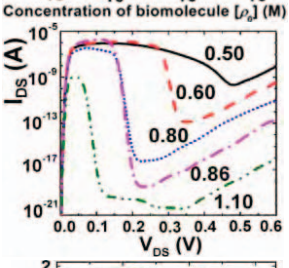

Figure 6. I-V curves of the proposed GNR NDR devices. E_g of channel is 0.5 eV, and E_g of source and drain varies between 0.5 and 1.1 eV (marked on the curves).

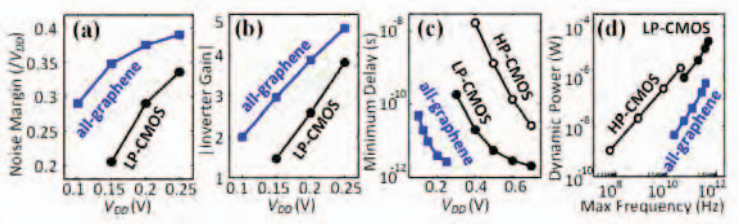

Figure 7. Performance of 22-nm (channel length of TFETs) 2D all-graphene inverter circuit (fan-out=2) scheme compared to that of 22-nm low-power (LP) and high-performance (HP) CMOS in terms of **(a)** static noise margin; **(b)** gain; **(c)** minimum delay and **(d)** dynamic power consumption.

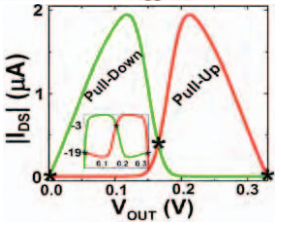

Figure 8. I-V curves of a bi-stable SRAM cell in Fig.3(h), based on the GNR NDR devices. The pull-down network is an n-type NDR, and pull-up network is a p-type NDR. V_{DD}= 0.33 V.