

High-Performance Field-Effect-Transistors on Monolayer WSe₂

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Monolayer Tungsten Diselenide (WSe₂) exhibits tremendous advantages as a channel material for next-generation field-effect-transistors (FETs). This paper reviews the relevant physics and properties of WSe₂ and highlights the excellent scalability of monolayer WSe₂ for ultra-short channel (sub-5 nm) FETs. The crucial role of metal-WSe₂ contacts in determining the performance of monolayer WSe₂ FETs is also emphasized using experiments guided by ab-initio density functional theory (DFT). With a suitably chosen contact, a back-gated monolayer WSe₂ FET on Al₂O₃ substrate is shown to exhibit both high mobility and high ON-current.

Introduction

Monolayer Transition Metal Dichalcogenides (TMD), a family of 2D semiconductor layers arranged in a hexagonal lattice, have attracted tremendous attention due to their pristine interfaces (without out-of-plane dangling bonds), thermal stability, and high scalability in device application.¹⁻⁵ Monolayer WSe₂ is a member of this family, beside the widely studied monolayer molybdenum disulfide (MoS₂) that has been experimentally demonstrated with high crystal and electronic quality.^{4, 5} Compared to MoS₂, WSe₂ has smaller electron/hole effective mass (as listed in Table I) and thus higher mobility. Recent experiments show that WSe₂ can be used for making both n-type⁴ and p-type⁵ FETs, as well as complementary inverters⁶, which has not yet been achieved on MoS₂. In addition, monolayer WSe₂ FET has been demonstrated with an ideal sub-threshold swing (SS) of 60 mV/decade⁵. Therefore, WSe₂ seems promising for future FET applications.

Basic Properties of Monolayer WSe₂

Table I. Comparison of the basic properties of WSe₂ and MoS₂^{4, 5, 7-9}.

	Band gap (eV)	Electron affinity (eV)	m _{electron/hole} (m ₀)	Bulk FET mobility electron/hole (cm ² /V.S)	Monolayer FET mobility electron/hole (cm ² /V.s)
WSe₂	~1.6	~3.9	~0.33 /0.46	NA/~500	~140/~250
MoS₂	~1.8	~4.2	~0.57/0.66	~470/480	~63/NA

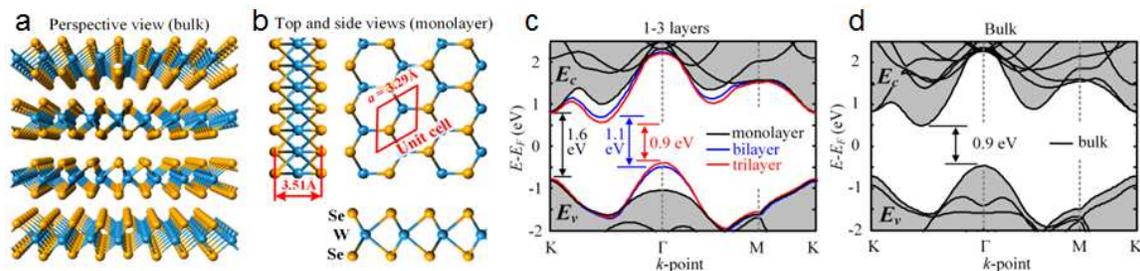


Figure 1. Various views of the lattice structure of (a) bulk and (b) monolayer WSe₂. In each layer of WSe₂, a W-atom plane is sandwiched between two Se-atom planes. Each in-plane parallelogram unit cell contains two Se atoms and one W atom. (c), (d) Band structures of monolayer, bilayer, trilayer and bulk WSe₂ respectively, indicating that monolayer WSe₂ is a direct band gap semiconductor with a band gap of ~1.6 eV. These data are calculated using the Atomistix Tool Kit (ATK) tool¹⁰.

Fig. 1a, b show the lattice structure of bulk side (perspective) view and monolayer (top and side views) WSe₂ with a distance of 3.51 Å between Se-atom planes, in-plane unit cell and lattice constant (3.29 Å) indicated in (b). Se atoms at the surfaces are fully bonded with neighboring atoms, which avoids dangling bonds and thus reduces the possibility of interface trap generation, benefiting the carrier mobility and device reliability. Fig. 1c, d show the band structures of monolayer, bilayer and trilayer WSe₂ and bulk WSe₂. Bulk WSe₂ has an indirect band gap (E_g) of 0.9 eV, which is in contrast with the direct band gap of 1.6 eV observed in monolayer WSe₂.¹¹ From the viewpoint of quantum confinement, the valleys in charge of electron/hole conduction in bulk WSe₂ are raised up/down when the number of WSe₂ layer is reduced. The confinement effect is not apparent until the layer number becomes less than three. As shown in the transition from bulk to trilayer, to bilayer and eventually to monolayer WSe₂, valleys at K point in k-space gradually take over the carrier population (conduction band minima and valence band maxima both move to K point), resulting in the direct band gap. It is worthwhile to note that, due to the lack of inversion symmetry (different atomic orbitals (of W and Se) on two sides of the unit cell, as shown in Fig. 1b), monolayer WSe₂ does not exhibit the gapless and linear dispersion relation as in graphene in spite of its graphene-like hexagonal lattice (with same C orbitals on both sides of the unit cell).

Monolayer WSe₂ based FET

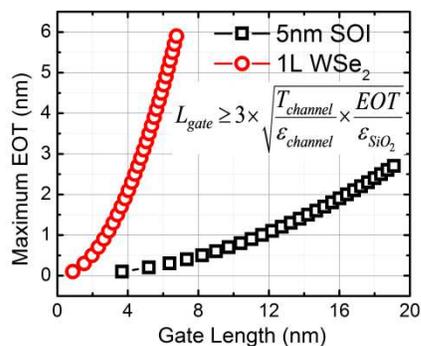


Figure 2. Curves showing the projected maximum effective oxide thickness (EOT) vs. gate length for 5 nm Si SOI FET and monolayer (1L) WSe₂ FET, which indicates that compared to 5 nm Si, 1L WSe₂ as FET channel material significantly relieves the strict requirement on the EOT scaling, which may introduce gate leakage.

The atomic-scale thickness (~0.65 nm) of monolayer WSe₂ makes it extremely promising as channel material in FETs, because it guarantees excellent FET electrostatics and thus

device scalability. Natural length ($\sqrt{T_{\text{channel}} EOT / \epsilon_{\text{channel}} \epsilon_{\text{SiO}_2}}$ for single gate device, where T_{channel} is channel thickness, $\epsilon_{\text{channel}}$ is dielectric constant of Si, and ϵ_{SiO_2} is dielectric constant of SiO_2) is normally used to characterize the scalability of FETs¹². For sufficient immunity against short channel effect, natural length is required to be shorter than one third of the gate length, which is fixed for a given technology node. According to the expression for natural length, the thicknesses of gate dielectric and channel should be scaled to meet this condition. Reducing gate dielectric may risk severe gate tunneling leakage and process variation. In comparison, shrinking the channel thickness reduces the natural length without causing those problems. As shown in Fig. 2, due to the much thinner channel thickness, monolayer (1L) WSe_2 FET (fabricated on thick SiO_2) significantly relieves the requirement of EOT scaling compared to the 5 nm Si FET (SOI structure), thereby leading to more robust device performance.

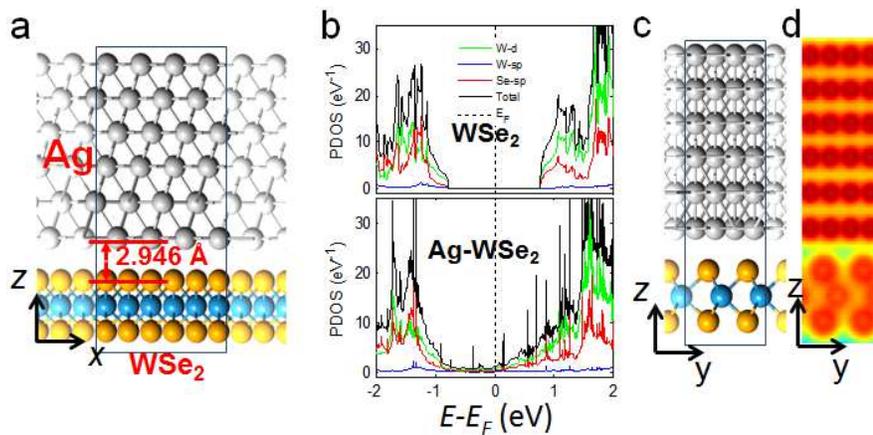


Figure 3. (a, c) Side views of the relaxed contact regions at the interface between WSe_2 and Ag (111) surfaces, respectively, from different directions; the (111) face of Ag has the lowest energy. (b) Partial density of states (PDOS) (from top to bottom) of W and Se electron orbitals, for monolayer WSe_2 , and Ag-WSe_2 system. The green, blue, red and black curves represent d-orbital of tungsten (W) atoms, sp-orbital of W atoms, sp-orbital of Selenium (Se) atoms, and the total PDOS of WSe_2 as indicated by the legend inside the top plot. (d) Contour plot of the electron density in planes normal to the interface in (c). The contour plots represent the average electron density along the x-axis.

The interface between 2D semiconductors and three-dimensional (3D) metal contacts is one of the major parameters, which determines the performance of 2D material based nanoelectronic devices. The contact resistance has been found to be a key factor that can significantly influence device performance of bulk WSe_2 FETs¹³. Hence, it is necessary to explore methods to form low-resistance contacts to 1L WSe_2 to achieve high performance WSe_2 FETs. Our recent work^{4,13} has shown that it is possible to form n-type ohmic contact to 1L WSe_2 by suitable contact metals, thereby providing guidance to experimental exploration of high-performance n-type WSe_2 FETs. In our previous work we found that In forms excellent contact with monolayer WSe_2 .⁴ However, In has poor adhesion with substrate and low melting point. Hence, we need to explore new contact metals for high performance monolayer WSe_2 FET. Ab-initio DFT calculations were employed to simulate the metal- WSe_2 system in a similar spirit as earlier studies in related TMD materials¹³. Fig.3a shows side views of the relaxed contact regions (which have the lowest energy) at the interface between monolayer WSe_2 with Ag (111) – an

intentionally chosen small-work-function metal in order to form good contact for n-type device. PDOS projections onto selected W and Se orbitals for monolayer WSe₂ (Fig. 3b) were calculated based on the structure shown in Fig.3a. As shown in Fig. 3b (top), there are almost no states near the Fermi level of monolayer WSe₂, indicating that monolayer WSe₂ in its natural state is intrinsic. However, after depositing Ag onto the monolayer WSe₂, the Fermi energy (E_F) moves towards the conduction band (Fig. 3b, bottom) and electron states are induced between E_F and the conduction band, exhibiting that WSe₂ is n-doped by Ag. The capability of metal doping of WSe₂ can also be gauged by observing the electron density at the metal-WSe₂ interface. The Ag-WSe₂ contact region (in Fig. 3c) has an electron density less than 0.011\AA^{-3} as shown in Fig.3d.

Fig. 4a, b show the optical image of a fabricated monolayer WSe₂ FET and its 3D schematic structure, respectively. 72 nm Al₂O₃ on n⁺⁺ Si is used as substrate, which provides clear optical contrast to identify the number of WSe₂ film layers. Fig. 4c shows the transfer characteristics of the fabricated device, which clearly displays n-type behavior with large ON/OFF ratios exceeding 10^6 and electron mobility reaching $48\text{ cm}^2/\text{V}\cdot\text{s}$, which is significantly higher than that any of fabricated back-gated monolayer MoS₂ FETs ($0.1\text{-}10\text{ cm}^2/\text{V}\cdot\text{s}$)^{2,9}. For monolayer WSe₂ FET with Ag contact, the ON-current is around $110\text{ }\mu\text{A}/\mu\text{m}$ for $V_{bg} = 30\text{ V}$ and $V_{ds} = 4\text{ V}$ as shown by the output characteristics in Fig. 4d. Fig.4d shows a current saturation at $V_{ds} > 2.5\text{ V}$ and $V_{bg} > -6\text{ V}$, which has not been observed on any reported back-gated monolayer MoS₂ FETs, indicating that monolayer WSe₂ has high potential for digital applications since current saturation is crucial in digital circuits. On our back-gated WSe₂ FETs (fabricated on 72 nm Al₂O₃/Si substrate), the subthreshold swing (SS) is around 250-300 mV/dec. As mentioned in our previous work⁴, this high SS can be attributed to the defects/traps in the ALD layer and/or in the Si/ALD interface, it is not indicative of the TMD layer itself. The SS can be reduced by decreasing the thickness of the back gate dielectric film or by fabricating top gated WSe₂ FET with a thin high- κ dielectric film. The high ON-current corresponds to a current density of $1.69 \times 10^7\text{ A}/\text{cm}^2$, which is about 30 times larger than the maximum sustainable current density of copper interconnects¹⁴ employed in nanoscale integrated circuits, and only about an order magnitude below that of graphene¹⁵.

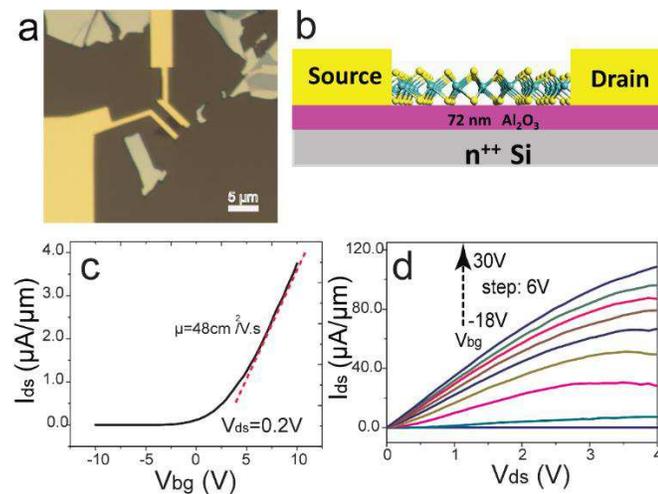


Figure 4. (a) Optical image of a fabricated monolayer WSe₂ FET on 72 nm Al₂O₃/Si substrate. (b) Schematic of back-gated monolayer WSe₂ FET structure. (c) Transfer characteristics of a back-gated monolayer WSe₂ FET with Ag (10 nm)/Au (100 nm) contact. (d) Corresponding I_{ds} - V_{ds} curve from the device in (c). Device size (width/length) is: $1\text{ }\mu\text{m} / 1.5\text{ }\mu\text{m}$.

Summary

In this paper, relevant physics and properties of WSe₂ are reviewed. The scaling analysis indicates that monolayer WSe₂ is highly suitable for ultra-short channel (sub-5 nm) FETs. DFT calculations show that Ag can form a good contact with monolayer WSe₂ by doping WSe₂. Under the guidance of DFT calculations, our fabricated monolayer WSe₂ FET with Ag contact exhibits high ON-current of 110 $\mu\text{A}/\mu\text{m}$ and high mobility of 48 cm^2/V , indicating that monolayer WSe₂ has tremendous advantages as a channel material for next-generation FETs.

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