Vertically Stacked and Independently Controlled Twin-Gate MOSFETs on a Single Si Nanowire

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***Abstract*—For the first time, we demonstrate the fabrication of two independently controlled gate-all-around MOSFETs on a single vertical silicon nanowire using CMOS process technology. The second gate is vertically stacked on top of the first gate without occupying additional area and thereby achieving true 3-D integration. The fabricated devices exhibit very low leakage, tunability in drain current, as well as "AND" gate functionality with 50% reduction in area for both n- and p-type MOSFETs. The twin-gate device structure is also promising for implementing other device types such as stacked SONOS memory and tunneling FET. We anticipate that our vertically integrated device architecture will provide unique opportunities for realizing ultra-dense CMOS logic on a single nanowire.**

***Index Terms*—AND gate, gate-all-around (GAA) FET, inverter, monolithic 3-D IC, nanowire FET, twin-gate, vertically stacked MOSFETs.**

I. Introduction

GATE-ALL-AROUND (GAA) nanowire transistors are one of the most promising nonplanar nanoscale device structures that have demonstrated excellent performance, scalability, and immunity to short-channel effects [1]. The near-ideal subthreshold slope (SS) and high ON/OFF ratio make them ideal candidates for various CMOS applications. From a high-density integration point of view, vertical nanowire transistors have the smallest possible device area ($4F^2$, where F is the half-pitch) [2]. Moreover, the vertical GAA architecture has the greatest potential for stacking devices on top of each other and therefore opens up the possibility of realizing true 3-D integration [3] and novel logic circuit design [4]–[7].

This letter presents the first attempt to fabricate two transistors on a single vertical silicon nanowire (Fig. 1) realizing true 3-D integration. The fabricated device architecture, having two independently controlled MOSFETs connected in series, does not occupy any additional planar area except an extra gate contact. Consequently, compared with the single vertical nanowire transistor, the stacked MOSFETs provided the two-input AND gate functionality with 50% area savings. The drain current I_D could be modulated by either of the gate biases without impacting the V_T of the other transistor in the stack. Furthermore, the tunability of the separation between the two gates, which is 7 nm in the current demonstration, makes the presented device architecture promising for implementing electrically doped tunneling FET (TFET) [8] and stacked SONOS memory cells [9]–[11].

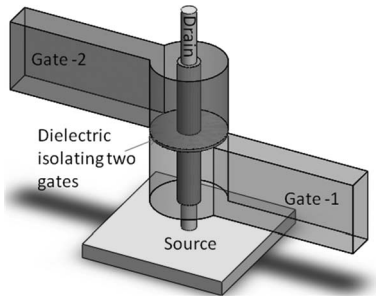

Fig. 1. Schematic showing the 3-D view of the stacked vertical twin-gate nanowire MOSFET.

II. Device Fabrication

The device structure was easily achieved through simple processes shown in Fig. 2 on n- and p-type wafers (doping $\sim 1 \times 10^{15}$ cm^{-3}) for p- and n-type devices, respectively. Vertical nanowire definition was achieved by dot patterning using deep-ultraviolet (DUV) lithography, hard mask, and silicon etching, followed by sacrificial oxidation. Bottom implantation with arsenic (As) or boron (B) [Fig. 2(a)] was performed to devise the bottom electrode. The bottom gate was defined after isolation high density plasma (HDP) oxide deposition and etch back. It comprises gate oxide growth ($\sim$4 nm), α-Si deposition, chemical–mechanical polishing (CMP) [Fig. 2(b)], α-Si etch back using tetramethylammonium hydroxide (TMAH) solution to define the gate length, gate implantation, activation, resist patterning, and etching to define gate extension [Fig. 2(c)]. The gate oxide on the exposed silicon pillar was then etched away and regrown ($\sim$7 nm), which also formed the gate-to-gate oxide separation. Thin ($\sim$50 nm) α-Si was then deposited, and was angle implanted and activated [Fig. 2(d)]. Low-pressure chemical vapor deposition (LPCVD) tetraethyl orthosilicate (TEOS) oxide of 40 nm thick was deposited [Fig. 2(e)], followed by resist coating and blanket etch back in an O_2 ambient [Fig. 2(f)], which determined the top gate length. The exposed oxide was wet etched [Fig. 2(g)], to expose the α-Si tip, which was then isotropically dry etched (selective to oxide). The top electrode

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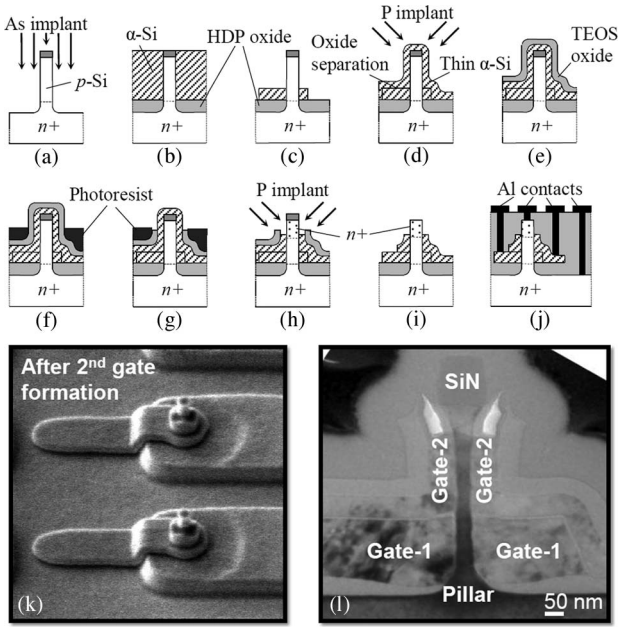

Fig. 2. Fabrication process of the vertically stacked twin-gate nanowire nMOS. (a) Bottom implantation after nanowire definition; (b) after isolation oxide and oxide/α-Si gate stack formation, followed by CMP of α-Si; (c) wet etch back of α-Si, first gate doping and etching using lithography, followed by (d) second gate stack deposition, and angle implantation and activation; (e) TEOS deposition; (f) resist coating and etch back; (g) oxide wet etch; (h) resist strip and isotropic etching of α-Si tip, followed by top implant and (i) second gate patterning; (j) metallization with Al; and (k) tilted SEM micrograph and (l) TEM micrograph after the stacked-gate formation.

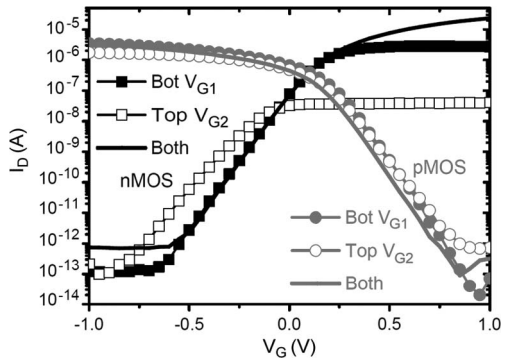

Fig. 3. I_D–V_G characteristics of the stacked twin-gate n- and p-type transistors measured on 35-nm-diameter silicon nanowires. The drain current is obtained by sweeping V_{G1} or V_{G2} while keeping the other one floating, as well as sweeping both V_{G1} and V_{G2} together. The drain voltage is kept at |1.5| V, and the source is grounded.

was then implanted with phosphorous (P) or B at 45° angle and activated [Fig. 2(h)]. Top gate extension was then patterned and etched [Fig. 2(i)] before premetal dielectric deposition, contact lithography and etching, and final metallization [Fig. 2(j)]. Fig. 2(k) and (l) shows the SEM and TEM micrographs after second gate formation, respectively.

III. Results and Discussion

The transfer characteristics of the individual nanowire MOSFETs are shown in Fig. 3, where I_D–V_G were measured on 35-nm-diameter n- and p-type devices. The voltage is applied to one of the gates while keeping the other floating, as well as to both gates together. For the p-type devices,

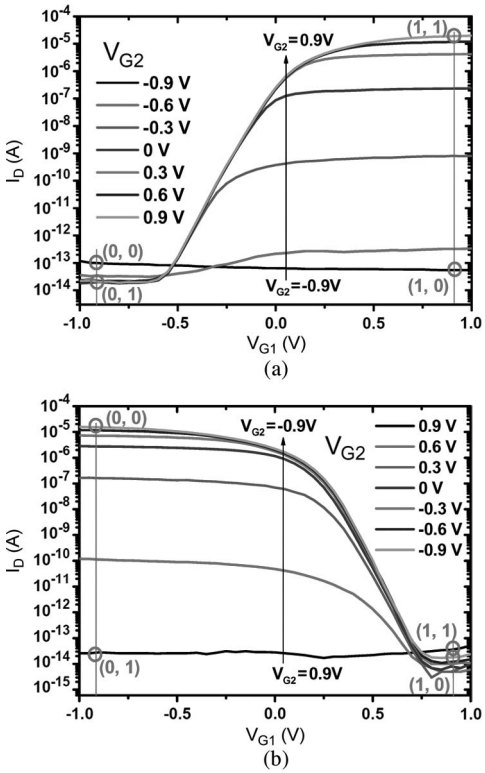

Fig. 4. I_D–V_G characteristics of the stacked-gate vertical nanowire transistor for (a) nMOS and (b) pMOS measured on 35-nm-diameter Si nanowires. The drain current is obtained by sweeping V_{G1} for various V_{G2}. The drain voltage is kept at |1.5| V, and the source is grounded. The circles indicate four different input states (V_{G1}, V_{G2}).

both transistors are almost identical, except for minor degradation of SS of the top gate device, as a result of the thicker gate oxide [i.e., ∼7 nm (top) and ∼4 nm (bottom)]. For the n-type devices, besides SS degradation, the top transistor has a negative threshold-voltage $(V_{\rm th})$ shift with a lower saturation current. As specified in Section II, the S/D implant species for the n-type devices are As at the bottom and P on the top of the nanowire [for the p-type devices, the S/D implant species are both B]. The angle-implanted P diffuses into the channel of the top transistor after dopant activation, which reduces the effective p-doping level of the channel. A more negative $V_{\rm th}$ is therefore obtained. The bottom device is not affected since As is not as diffusive. In the case of pMOS, the implanted B diffuses into the channel from both sides of the nanowire and decreases the $V_{\rm th}$ for both top and bottom transistors [12]. The same reason creates asymmetrical extension resistances for the n-type devices. The drain current of nMOS is affected badly by the larger bottom extension resistance when the bottom gate is inactive. When both gates are swept, $I_{\rm Dsat}$ increases for nMOS since the extension resistance reduces significantly as compared to single-gate operation. The pMOS current, on the other hand, did not improve as the extension resistances with single-gate operation were already low due to B diffusion into the channel, as discussed earlier. Nevertheless, it is worth noting that either of the gates can modulate the drain current independently. The $V_{\rm th}$ values, which are rather low due to no channel implant, could be corrected using either a FUSI gate or a metal gate without impacting the underlap resistance between the gates [2].

The I_D–V_G characteristics when both gates are active are shown in Fig. 4. The bottom-gate voltage V_{G1} is swept from

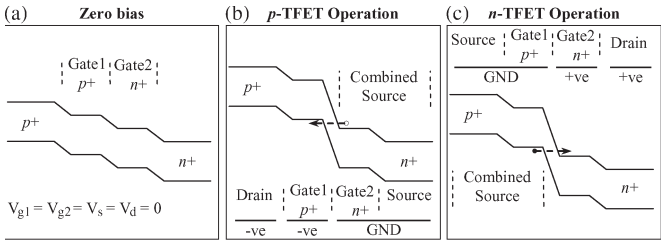

Fig. 5. Band diagrams of the twin-gate TFET at (a) zero bias, (b) p-TFET operation, and (c) n-TFET operation, illustrating the operating principles.

-1.0 to 1.0 V. The top-gate voltage V_{G2} is varied from -0.9 to 0.9 V in steps of 0.3 V. As shown in the figure, the drain current can be independently controlled by both V_{G1} and V_{G2}. As the stacked transistors are connected in series, the $V_{\rm th}$ of the bottom transistor is not affected by the top-gate biasing conditions, unlike the independent double-gate FinFETs [4], [5]. In Fig. 4(a), the device is ON only when both gates are biased at high V_G, e.g., $V_{G1} = V_{G2} = 0.9$ V. If any of the gates is biased low, for example, at -0.9 V, there is no drain current. Similarly, for the p-type devices in Fig. 4(b), there is a drain current only when both gates are low, e.g., $V_{G1} = V_{G2} = -0.9$ V, and no current flows when any of the gates is high, for example, 0.9 V. The "AND" gate functionality is therefore achieved, as indicated by the circles in the figures for four different input states $(V_{G1}, V_{G2}) = (0, 0)$, (0, 1), (1, 0), and (1, 1).

The proposed stacked device structure is also useful for achieving electrically doped TFETs [8] for ultralow-power CMOS applications [13]. By incorporating an extra gate, which would work in tandem with the existing gate to form electrically doped regions of opposite polarity, a narrow tunneling junction can be formed between the gates. Fig. 5 shows the band diagrams illustrating TFET device operation with two gates. In essence, the gate next to the source becomes an assisting gate for forming an abrupt tunneling junction via electrical doping. For p-TFET (n-TFET), the n+ (p+) source and n+ (p+) assisting gate can be shorted, as shown in Fig. 5(b) and (c). Device operation is then similar to that of a conventional TFET, with the assisting gate and source acting as a combined source. Since the tunneling junction is always between the two gates, both source–channel and drain–channel junctions need not be abrupt and can be deliberately made non-abrupt for suppression of ambipolarity by preventing tunneling at these junctions. Essentially, the exact same device can be changed from n-TFET to p-TFET by simply changing bias while still retaining ambipolarity suppression for low OFF current. In addition, $V_{\rm th}$ can be adjusted by varying the combined source bias. It is worth mentioning in this letter that for this device to work more effectively than a conventional TFET, the oxide separating the two gates has to be thin—3 nm or below. The use of high-k dielectrics may further aid in achieving high-performance TFET devices [13].

If the gate oxide of the top transistor is replaced with an O–N–O stack, this device can be transformed into a stacked SONOS memory with a bottom select transistor, which could be very suitable for embedded memory applications [9]–[11].

IV. Conclusion

The first demonstration of true 3-D integrated nanodevices has been achieved by fabricating vertically stacked twin-GAA transistors on a single silicon nanowire with both n- and p-type MOSFETs. Independent control of the drain current has been demonstrated by varying either of the gate biases, and the "AND" gate functionality has been achieved with 50% reduction in footprint compared with the single-gate vertical nanowire transistors. This demonstration opens up the possibility of building ultralow-power and dense 3-D functional devices and circuits. In particular, the proposed device architecture is shown to be attractive for realizing electrostatically doped TFETs and SONOS memory. Many other structures such as CMOS inverters can also be fabricated in a stacked form following the scheme of this letter.

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