A Novel Enhanced Electric-Field Impact-Ionization MOS Transistor

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***Abstract*—A novel enhanced electric-field impact-ionization MOS (E2I-MOS) is proposed, which achieves a subthreshold swing of as low as 6 mV/dec at room temperature while reducing the breakdown voltage by about 1.8 V. The E2I-MOS exhibits $\geq 10\times$ lower OFF-state leakage compared to previously reported I-MOS structures, thus reducing the power consumption and also making the device more scalable. A very high ON current of the order of 1 mA/μm can be obtained. Additionally, the device reliability is expected to be improved by confining hot carrier generation away from the gate dielectric region.**

***Index Terms*—Band-to-band tunneling, breakdown voltage, I-MOS, impact ionization, subthreshold slope.**

I. Introduction

THE impact-ionization MOS (I-MOS) transistor [1]–[3] has been a topic of active research [4]–[18] since its introduction due to its capability of providing an ultralow subthreshold swing (S). It is essentially a gated p-i-n diode structure employing an avalanche breakdown mechanism. However, it faces major challenges due to its high breakdown voltage ($V_{\rm BD}$) needed for normal operation. Moreover, as the device dimensions are scaled down, I-MOS structures become vulnerable to band-to-band tunneling (BTBT) leakage, which severely impedes the scalability of the device [4]. Another serious issue in an I-MOS is the device reliability due to the generation of hot carriers in the vicinity of the gate dielectric [3]. Although various techniques have been proposed for the $V_{\rm BD}$ reduction [10]–[14] and for combating the reliability issues [9], [11], [16], significant improvements remain a necessity. Moreover, very little work has been done for the reduction of the BTBT leakage. Although the lowering of $V_{\rm BD}$ leads to the decrease in the BTBT to some extent, further reduction is necessary to lower the power dissipation as well as to improve the scalability. Thus, there is a compelling need for exploration of novel device structures and materials for the I-MOS which, apart from reducing the breakdown voltage, will also improve its OFF-state leakage performance and reliability.

In this letter, we propose a novel enhanced electric-field impact-ionization MOS (E2I-MOS) employing a heterostructure of two materials having different bandgaps. It is shown that, with proper tuning of band offsets, a low breakdown voltage, even below that of the narrower bandgap material, could be achieved. Our design also provides a reduction of $\geq 10\times$ in the OFF-state BTBT leakage as compared to previously reported I-MOS structures [12], [13], thus reducing the power dissipation and enabling a higher scalability. Additionally, the reliability, which is a serious issue in an I-MOS, is also expected to improve in the proposed device.

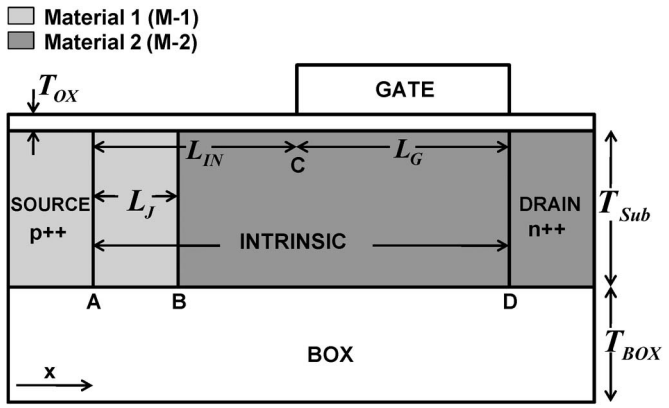

Fig. 1. Basic device structure for n-type E2I-MOS. In all simulations, $L_G = L_{\rm IN}$ and drain voltage $V_D = 0$. Unless mentioned otherwise, the parameters used are as follows: $L_G = L_{\rm IN} = 50$ nm, $L_J = 10$ nm, $T_{\rm OX} = 3$ nm, $T_{\rm Sub} = 40$ nm, $T_{\rm BOX} = 350$ nm, gate work function $\Phi_M = 4.17$ eV, and maximum source/drain doping of 2×10^{20} cm^{-3} with characteristic length of 5 nm.

II. Device Structure and Operation Principle

The schematic of an n-type E2I-MOS is shown in Fig. 1. Although equally feasible on bulk, a heterostructure on the insulator is used because it leads to reduced leakage currents due to the elimination of drain-to-body and source-to-body leakage components [8]. The materials are chosen such that material 1 (M-1) has a higher bandgap (E_g) than material 2 (M-2), and the difference in the bandgaps approximately equals the valence band offset $|\Delta E_g| \approx |\Delta E_V|$ while $\Delta E_C \approx 0$. Si and SiGe are very good choices for the materials to be used as M-1 and M-2, respectively. Such heterostructure could be fabricated using selective epitaxy of SiGe inside recessed silicon. Ge condensation with cyclic annealing can be used to convert the Si seed layer (a layer of single crystal Si used to start the SiGe epitaxy) into SiGe, which can also enhance the Ge concentration in the deposited SiGe [19]. The fabrication process can be simplified by designing this device in vertical wire/pillar architecture where Si/SiGe can be a base wafer and the other material, SiGe/Si, is epitaxially deposited. The pillars can be

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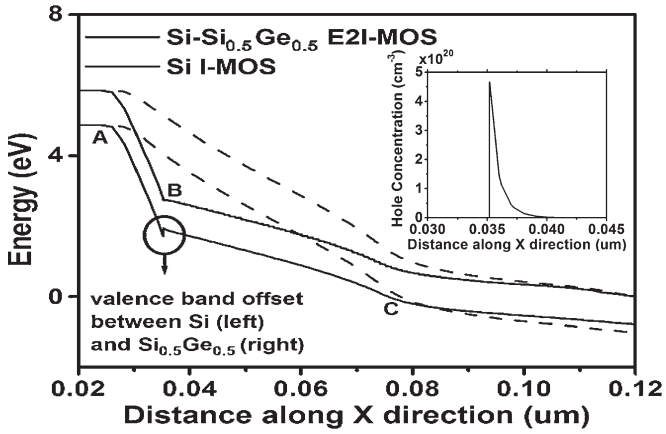


Fig. 2. Band diagrams for n-type E2I-MOS and I-MOS ($V_S = -4.8$ V and $V_G = 0$ V for both cases) during ON state. The points A, B, and C correspond to those in Fig. 1. Fermi–Dirac distribution function is employed. Temperature and mole-fraction dependent density of states and effective masses are used [20]. For the same applied bias, E2I-MOS ($|\Delta E_g| \approx |\Delta E_V| \approx 0.22$ eV) has much sharper band bending and, hence, higher electric field near the source than that in I-MOS. Inset figure shows the accumulation of holes, which causes the band bending. From the simulations, it is found that breakdown voltage has been reached for E2I-MOS but not for I-MOS at the biases shown.

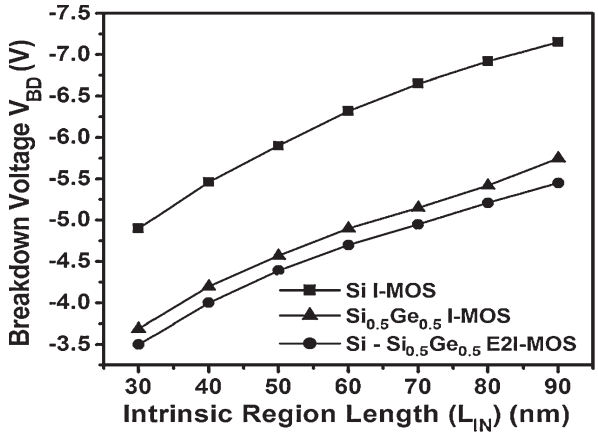


Fig. 3. Comparison of $V_{\rm BD}$ of n-type Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS with Si I-MOS and $Si_{0.5}Ge_{0.5}$ I-MOS at various $L_{\rm IN}$'s. E2I-MOS exhibits lower $V_{\rm BD}$ due to the enhanced electric field near the source.

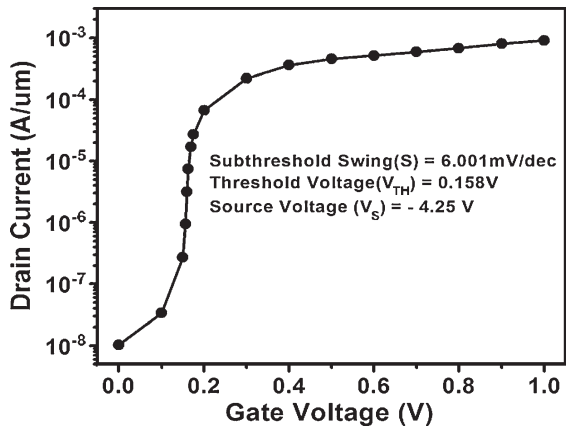


Fig. 4. Simulated I_D–V_G characteristics of n-type Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS ($V_{\rm BD} = -4.4$ V). Subthreshold swing is measured at the inflection point.

formed through simple patterning and dry etching. In this way, we can get a source, channel, and drain in a single heterojunction pillar without any intermixing of materials. As the gate can be defined using deposition and etch back, precise control on the gate edge is possible. Thus, a structure close to being self-aligned is possible without a self-aligned method. Furthermore, the obtained structure will be gate-all-around, providing even better electrostatic control over the channel and, hence, better electrical characteristics. For a p-type E2I-MOS, the material requirement is such that $\Delta E_g \approx \Delta E_C$ with $\Delta E_V \approx 0$.

The device simulations were done using a local-field impact-ionization model [20], which suffices since the nonlocal dead space effect is cancelled by the velocity overshoot effect in small p-i-n junctions ($<$ 100 nm) [21]. Previous experimental results [3] have proved the validity of the local-field model. Since the dimensions used ($L_G, L_{\rm IN},$ and L_J) are well above the threshold value ($\sim$5 nm), below which the quantum effects become important [15], this model is reasonably accurate in our case. To correctly model the transport across the abrupt heterojunction between M-1 and M-2, both the thermionic emission and tunneling have been taken into account.

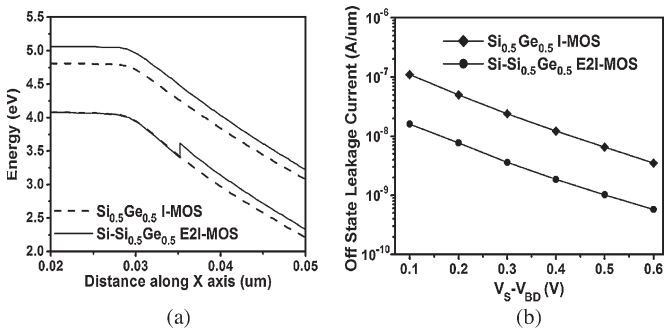
The operation principle of an n-type E2I-MOS is discussed in the following paragraph.

When a negative bias is applied to the source, with the drain grounded, electron-hole pairs are generated due to the impact ionization in the intrinsic region. The electrons are swept away by the electric field toward the drain; however, the holes created at $x > L_J$ are obstructed from moving toward the source due to the valence band offset, leading to the accumulation of holes at the heterojunction. The accumulated holes pull the bands down, increasing the electric field near the source (see Fig. 2). Since the impact ionization coefficient rises exponentially with the electric field [22], the increase in the electric field enhances the electron-hole pair generation. This leads to the accumulation of more holes which, in turn, increases the electric field further. Thus, the accumulation of holes acts as a positive feedback to the impact ionization, and the increased electric field near the source results in the reduction of the breakdown voltage.

From Fig. 2, it is clear that the E2I-MOS has much sharper band bending and, hence, a higher electric field near the source compared to that of the standard I-MOS for the same applied bias. Although the reduction in $V_{\rm BD}$ through the manipulation of the electric field has been reported in some previous works [12], [13], our structure is based on a completely different device design platform. In Fig. 3, $V_{\rm BD}$ of the Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS (M-1: Si; M-2: $Si_{0.5}Ge_{0.5}$) is compared with the Si I-MOS and $Si_{0.5}Ge_{0.5}$ I-MOS at various intrinsic region lengths ($L_{\rm IN}$ in Fig. 1). For the Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS, a $V_{\rm BD}$ reduction of about 1.8 V compared to the Si I-MOS and 0.2 V compared to the $Si_{0.5}Ge_{0.5}$ I-MOS can be obtained. It is to be noted that the lowering of $V_{\rm BD}$ achieved in the E2I-MOS is not due to strain effects which, when included, could lead to further improvement due to the strain-induced bandgap reduction. The transfer characteristic of the Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS is presented in Fig. 4. A very low S of about 6 mV/dec and a high drive current of 1 mA/μm have been obtained.

III. Off-State Leakage and Reliability

As the device dimensions are scaled down, the OFF current of the I-MOS increases severely due to the BTBT leakage. A solution to this problem would be to use wide bandgap materials.



(a) (b)

Fig. 5. (a) Band diagrams during OFF state for n-type Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS and $Si_{0.5}Ge_{0.5}$ I-MOS at same bias voltages. For the same applied bias, electric field for both devices is same in the OFF state, as there is no accumulation of holes in E2I-MOS. However, the tunneling barrier for E2I-MOS is higher than that in I-MOS because E2I-MOS has higher bandgap material near the source. (b) Leakage currents are compared for same values of $V_S - V_{\rm BD}$ ($Si_{0.5}Ge_{0.5}$ I-MOS having higher $V_{\rm BD}$ should be biased at higher negative source voltage than that of Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS to obtain the same $V_{\rm TH}$). Leakage in E2I-MOS is much smaller than that in I-MOS due to the higher tunneling barrier and lower $V_{\rm BD}$.

However, the use of higher bandgap materials leads to a higher breakdown voltage. Moreover, for the same $V_S - V_{\rm BD}$ or $V_{\rm TH}$, the I-MOS with a wider bandgap material would have a higher BTBT than that with a narrower bandgap material. This is because the wider bandgap material requires higher V_S, which gives rise to a higher electric field and, hence, an enhanced BTBT. On the other hand, the uniqueness of the E2I-MOS is that, it is designed to achieve a substantial reduction in $V_{\rm BD}$ even though the bandgap of the material (M-1) near the source is higher. Thus, the leakage due to the BTBT is significantly lowered. Fig. 5 illustrates that the Si-$Si_{0.5}Ge_{0.5}$ E2I-MOS exhibits a $10\times$ reduction in the OFF-state leakage compared to the $Si_{0.5}Ge_{0.5}$ I-MOS because of its higher tunneling barrier as well as lower $V_{\rm BD}$. This leads to the reduction in the power dissipation, and since the BTBT severely limits the scalability of the intrinsic region $(L_{\rm IN})$, the E2I-MOS, having a substantially lower BTBT, also allows a higher scalability. Furthermore, for the E2I-MOS during the ON state, the electric field is increased near the source in the M-1 region while the field in M-2 is reduced (see Fig. 2); thus, the generation due to impact ionization caused by sharp band bending arising from the accumulation of holes can mostly be confined to M-1, which is away from the gate dielectric region. This is expected to reduce the $V_{\rm TH}$ instability and improve the reliability of the device.

IV. Conclusion

A novel high-performance E2I-MOS has been presented. It has been shown that, using a heterostructure composed of two materials having different bandgaps, a breakdown voltage lower than that of both materials can be obtained. Using TCAD simulations for the Si-$Si_{0.5}Ge_{0.5}$ heterostructure, a breakdown voltage reduction of 1.8 V, a subthreshold swing on the order of 6 mV/dec at room temperature, and a drive current of 1 mA/μm have been demonstrated. An order of magnitude reduction in the OFF-state leakage current is achieved in the E2I-MOS by lowering the BTBT. The proposed device is also expected to have a better reliability due to the confinement of the carrier generation away from the gate dielectric.

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