High-Current Failure Model for VLSI Interconnects Under Short-Pulse Stress Conditions

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***Abstract*—Short-time high joule heating causing thermal breakdown of metal interconnects in ESD/EOS protection circuits and I/O buffers has become a reliability concern. Such failures occur frequently during testing for latchup robustness and during ESD/EOS type events. In this letter, heating and failure of passivated TiN/AlCu/TiN integrated circuit interconnects in a quadruple level metallization system of a sub-0.5 μm CMOS technology has been characterized under high-current pulse conditions. A model incorporating the heating of the layered metal system and the oxide surrounding it has been developed which relates the maximum allowable current density to the pulse width. The model is shown to be in excellent agreement with experimental results and is applied to generate design guidelines for ESD/EOS and I/O buffer interconnects.**

VERY large scale integration (VLSI) interconnects frequently suffer short-time high joule heating under electrostatic discharge (ESD: > 1 A; < 200 ns event) and electrical overstress (EOS: > 1 μs event) conditions which are pervasive reliability hazards that affect IC devices of all categories [1]. Protection circuits are generally designed to minimize damage caused by these events. For improving reliability, these circuits are usually tested by subjecting them to typical discharge pulses to which the IC may be exposed during manufacturing or handling. Metal interconnections in protection circuits are heavily stressed during these tests and also during actual ESD/EOS type events. Interconnects are also known to experience similar stress conditions during testing for latchup robustness and also during the operation of certain field programmable gate arrays (FPGA's) that employ metal-to-metal voltage programmable links (VPL's) [2], [3] to make permanent connections in the wiring channels between logical elements. Aggressive scaling of IC devices have reduced the dimensions of interconnects. This has increased their susceptibility to damage caused by these high-current pulses [4]. Recently, thermally accelerated open circuit metal failures have been reported during ESD testing [5]. The purpose of this work is to comprehend IC metal heating under single high-current pulse stress and to formulate a model that can be used to generate robust interconnect design guidelines, including ESD/EOS and I/O buffer.

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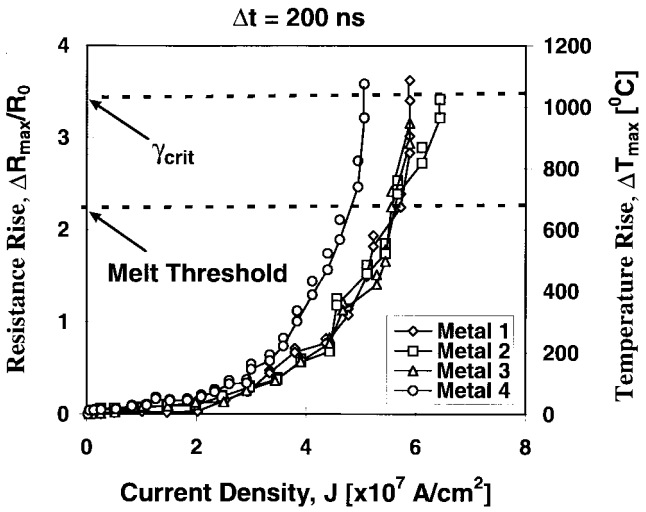

Fig. 1. Maximum instantaneous resistance and temperature rise of the metal lines stressed by a 200 ns pulse, plotted against the current density J. Identical temperature rise of metal 1, 2, and 3 is because the lines have identical thermal capacity. Metal 4 shows higher joule heating due to its bigger thermal capacity. The final open-circuit failure, the last data point on each curve, results when the stress due to molten metal expansion exceeds the fracture strength of ($\sim$ 1 Gpa [12]) of nitride overlayer.

A quadruple level (TiN/AlCu(0.5%)/TiN) metallization system in a state of the art sub-0.5 μm CMOS technology was used in this study. The interlevel dielectrics were approximately 1 μm thick. The oxide/nitride passivation layer was $\sim$ 2 μm thick. All the metal lines were 3×1000 μm (W×L) standard NIST recommended structures. For metal 4 the AlCu thickness was doubled. Initially the DC joule heating was measured for each level and, as expected, the thermal impedance increased with increasing underlying oxide thickness. A standard transmission line pulsing technique [6] was then used to generate constant current pulses of varying widths (50–500 ns) and amplitudes. The voltage, and hence the resistance of the metal lines increased roughly linearly with time during all the pulsing events in agreement with [7] where heating under the charged device model (CDM, a < 1 ns event) was analyzed. The input pulse energy was calculated using the equation

$$E = \int_0^{\Delta t} I \cdot V dt \approx \frac{1}{2} I^2 \cdot \Delta t \cdot [R_0 + R_f]. \qquad (1)$$

Here, I = current through the metal line, V = voltage developed across the line, Δt = pulse width in ns, R_0 = initial resistance of the unstressed line, and R_f = maximum resistance of line reached during the pulsing event. In Fig. 1

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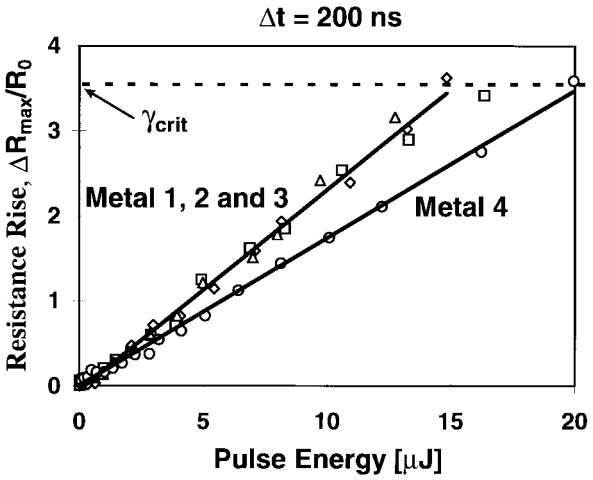

Fig. 2. The pulse energy versus resistance rise of the metal lines stressed by a 200 ns pulse. The thermal capacity $C_{\rm th}$ can be extracted from the relation, $E = C_{\rm th}\gamma(\mathrm{TCR})^{-1}$. Difference in slopes between metal 1, 2, 3, and metal 4 is due to the bigger thermal capacity of metal 4.

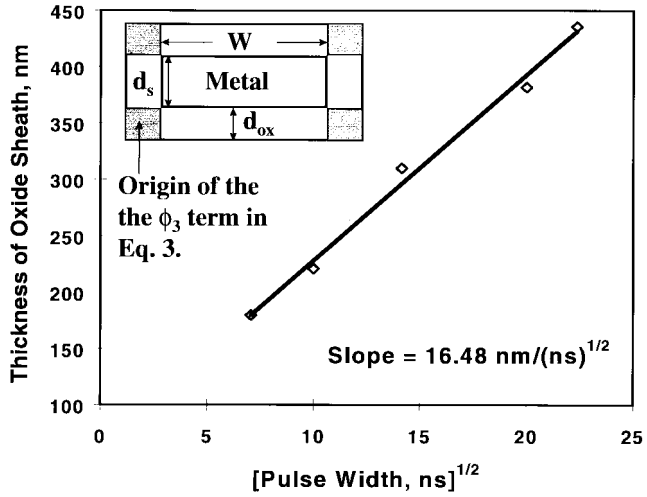

Fig. 3. Thickness of the heated oxide sheath $d_{\rm ox}$ around the metal lines increases with increasing pulse width (Δt). The heat diffusion constant $a_d = 1.65 \times 10^{-6}$ cm/(ns)$^{1/2}$, was extracted from this graph, and the corresponding thermal diffusivity of the oxide is $\sim 1.0 \times 10^{-3}$ cm^2/s. This value is in rough agreement with those reported for deposited thin silicon dioxide films at high temperatures [13]–[15].

the maximum resistance (and temperature) rise above initial room temperature value, ($\Delta R_{\max}/R_0 = \gamma$, where $\Delta R_{\max} = R_f - R_0$), for each metal level has been plotted against the current density, for a 200 ns pulse. It can be observed that metal 1, 2, and 3, lines with equal dimensions have nearly identical resistance (or temperature) rise unlike the DC case. Also, for all the metal levels γ rises superlinearly with J, the current density, and they all fail when γ goes beyond a critical value $(= \gamma_{\rm crit})$. Similar joule heating behavior was observed for the other pulse widths. The values of $\gamma_{\rm crit}$ were independent of the pulse width and the metal level. The thermal capacity is proportional to the inverse of the slopes of γ versus energy curves. The thermal capacity of metal 1, 2, and 3 from Fig. 2 is 15.09×10^{-9} J/°C. This is larger than the 8.25×10^{-9} J/°C calculated for the TiN/AlCu/TiN stack. The difference between the theoretically and experimentally determined values of the thermal capacity suggests that a sheath of oxide around the metal was heated. This difference between the thermal capacities has been used to calculate the thickness of the oxide sheath. From heat diffusion theory [8] we expect the thickness of the oxide sheath to be proportional to the square root of the pulse width, $(\Delta t)^{1/2}$. This is confirmed by the linear dependence of the heated oxide sheath thickness $(d_{\rm ox})$ with $(\Delta t)^{1/2}$, as shown in Fig. 3.

A physical model is now presented that incorporates aluminum metal, barrier metal, and surrounding oxide heating. The critical pulse energy, $E_{\rm crit}$, for open circuit failure can be expressed as

$$E_{\rm crit} = [m_i c_i + m_j c_j + m_k c_k]\gamma_{\rm crit}(\mathrm{TCR})^{-1} + m_i L_{\rm fi}. \quad (2)$$

Here, m is mass, c is specific heat, TCR is the temperature coefficient of resistance, and $L_{\rm fi}$ is the latent heat of fusion of aluminum. Subscripts i, j, and k are for AlCu, TiN, and oxide sheath, respectively. The relation between maximum allowable current density $J_{\rm crit}$ and the pulse width can be obtained by combining (1) and (2) and using an oxide sheath of volume $V_{\rm ox}$ around the metal lines where $V_{\rm ox} = [4Ld_{\rm ox}^2 + 2L\{W + d_s\} \cdot d_{\rm ox}]$. Here, d_s is the thickness of the metal stack, $d_{\rm ox} = (a_d \Delta t)^{1/2}$,

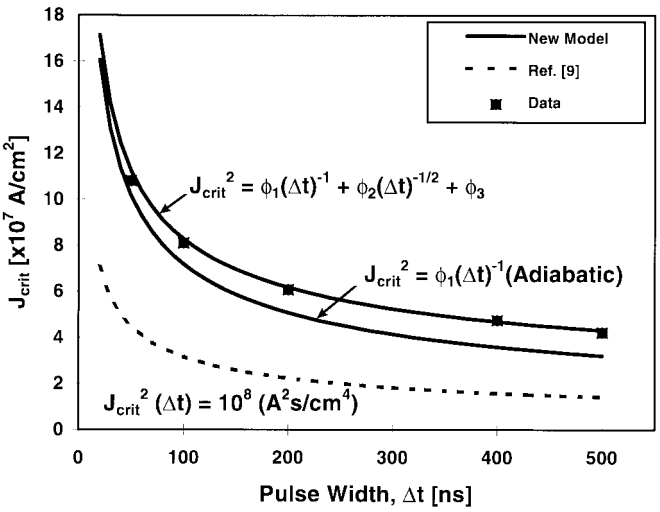

Fig. 4. The maximum allowable current density $(J_{\rm crit})$ versus pulse width (Δt), showing the close agreement between the model and experimental data. The model from [9] is also plotted for comparison. The constants are given by $\phi_1 = \lambda_0[(m_i c_i + m_j c_j)\gamma_{\rm crit}(\mathrm{TCR})^{-1} + m_i L_{\rm fi}]$ A$^2 \cdot$ s/cm^4, $\phi_2 = \lambda_0[\delta_{\rm k} c_{\rm k} \gamma_{\rm crit}(\mathrm{TCR})^{-1} 2L(W + d_s)(a_d)^{1/2}]$ A$^2 \cdot$ s$^{1/2}$/cm^4, and $\phi_3 = \lambda_0[\delta_{\rm k} c_{\rm k} \gamma_{\rm crit}(\mathrm{TCR})^{-1} 4La_{\rm d}]$ A^2/cm^4. Here, δ is the density and $\lambda_0 = [2/(\rho LA(2 + \gamma_{\rm crit})]$ with ρ as the resistivity and A as the cross-sectional area of AlCu. ϕ_1, ϕ_2, and ϕ_3 are explained in the text and are $\sim 5 \times 10^8$, $\sim 5 \times 10^{11}$, and $\sim 1 \times 10^{14}$, respectively, for these geometries.

and a_d is the heat diffusion constant extracted from Fig. 3. Hence

$$J_{\rm crit}^2 = \phi_1(\Delta t)^{-1} + \phi_2(\Delta t)^{-1/2} + \phi_3 \quad (3)$$

where ϕ_1 is a constant depending on interconnect geometry, material constants, and $\gamma_{\rm crit}$. The constants ϕ_2 and ϕ_3 have dependence on oxide properties too, including a diffusion constant that has been extracted from Fig. 3. For pulse widths <10 ns, near adiabatic condition is reached and the first term dominates. For pulse widths between 10 ns and ~2 μs, both the first and the second terms are significant. The ϕ_3 term

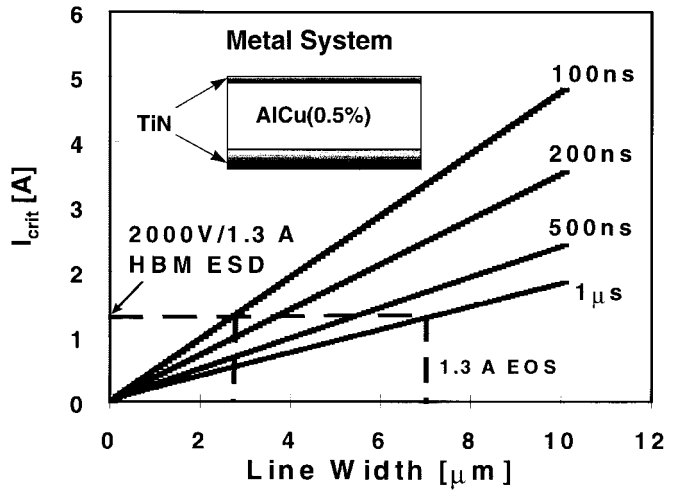

Fig. 5. The proposed model is used here to depict the relation between critical current $I_{\rm crit}$, pulse width Δt, and line width W. From this figure, various design guidelines can be generated for ESD/EOS and I/O buffer interconnects.

which arises from the DC thermal conductance will become significant for longer pulse widths ($>2\ \mu$s). Further, ϕ_2 and ϕ_3 will become increasingly important for narrower line widths. The critical current density values obtained using this relation are in excellent agreement with the experimentally observed values as shown in Fig. 4. This model can be used to provide interconnect design guidelines for high-current robustness. The adiabatic approximation of (3), i.e., $J_{\rm crit}^2 = \phi_1(\Delta t)^{-1}$ is also plotted. It is clear that heat dissipation into the surrounding oxide is significant under pulsed conditions of approximately 100 ns and hence the ϕ_2 term must be included in the model. In Fig. 4, we also compare an earlier work [9] that proposed a theoretical relationship ($J_{\rm crit}^2 \Delta t = 10^8$ A^{2}s/cm^4) and it is shown to be lower than the experimental values. The model in [9] did not take into account any heat dissipation into the surrounding oxide nor the latent heat of fusion, and was formulated using a critical temperature value of 300 °C based on work [10] where unpassivated metal lines deposited on window grade quartz substrates were studied under pulsed stress. This is much lower than the 1000 °C which is extracted from the present experimental work. Detailed thermal simulations of joule heating under a high-current pulse, by Gui *et al.* [11] had also indicated that the model from [9] has limitations for pulse widths bigger than ~2 ns. From (1) and (2), the critical value of the current pulse can be expressed as

$$I_{\rm crit} = \left(\frac{W(Wa_1 + a_2 V_{\rm ox})}{\Delta t} \right)^{\frac{1}{2}}. \tag{4}$$

Again, a_1 and a_2 are constants that depend on the geometry and material constants of the interconnect metal and the oxide. Finally, the model developed in the form of (4) can be used to determine the critical current for open circuit metal failure in terms of the pulse width and the line width as shown in Fig. 5. These curves provide design guidelines for ESD/EOS protection circuit interconnects. For example, a typical Human Body Model (HBM) ESD pulse, which can be described as a ~ 100 ns/1.3 A event [1] would require the width of the metal line to be greater than $\sim 2.5\,\mu$m. Similarly for an electrical overstress (EOS) event of 1 μs the minimum line width should be more than $\sim 7\ \mu$m. Hence a safe design guideline for these stress conditions would be $\sim 10\,\mu$m.

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