Thermal Characteristics of Submicron Vias Studied by Scanning Joule Expansion Microscopy

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***Abstract*—Thermal characteristics of submicron vias strongly impact reliability of multilevel VLSI interconnects. The magnitude and spatial distribution of the temperature rise around a via are important to accurately estimate interconnect lifetime under electromigration (EM), which is temperature dependent. Localized temperature rise can cause stress gradients inside the via structures and can also lead to thermal failures under high current stress conditions, such as electrostatic discharge (ESD) events. This letter reports the first use of a novel thermometry technique, scanning Joule expansion microscopy, to study the steady state and dynamic thermal behavior of small geometry vias under sinusoidal and pulsed current stress. Measurement of the spatial distribution of temperature rise around a submicron via is reported with sub-0.1 μm resolution, along with other thermal characteristics including the thermal time constant.**

***Index Terms*—AC temperature rise, atomic force microscope, current crowding, dc temperature rise, deep sub-micron via, electrostatic discharge, interconnect reliability, interconnect thermometry, scanning Joule expansion microscopy, spatial temperature distribution, thermal characteristics, thermal time constant, via electromigration.**

I. Introduction

CONTINUOUS scaling of VLSI interconnects has resulted in an increase in the aspect ratio of the vias (connection between adjacent metallization levels) and increase in the current density and associated thermal effects, namely self-heating. The magnitude and spatial distribution of the temperature rise around a via can strongly influence the EM performance of multilevel interconnect structures consisting of leads and vias, which has an exponential dependence on the inverse metal temperature [1], [2]. Furthermore, current crowding and localized temperature rise [3]–[5] in the via can cause stress gradients around the via structures and can also lead to thermal failures under short-duration high current stress conditions, such as ESD events [6], [7]. Hence, a suitable thermometry technique is necessary to allow measurements of the magnitude and spatial distribution of the temperature rise around submicron vias in order to accurately model their reliability and provide design guidelines for preventing thermal failures.

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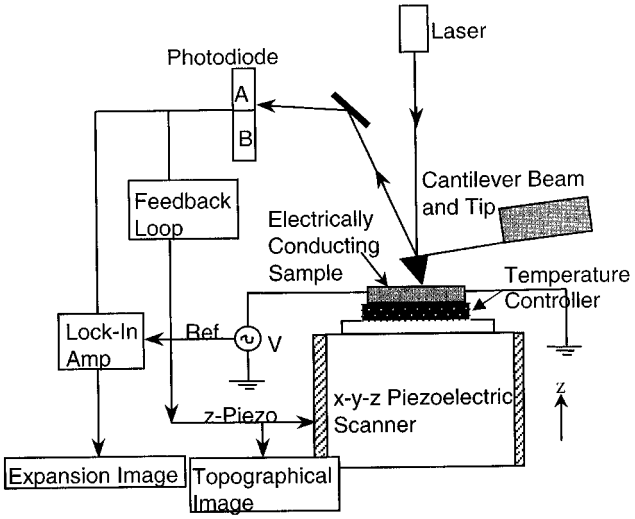

Fig. 1. Schematic diagram of the experimental setup used for the scanning Joule expansion microscopy (SJEM).

In general, interconnect thermometry based on temperature-dependent electrical resistivity of the interconnect metal is used to calculate a spatially averaged temperature rise along the interconnects [6], [8]. However, this does not provide local temperature rise which may be much higher around vias. The spatial resolution of far-field optical techniques, such as scanning thermoreflectance thermometry [9], infrared thermography [10] and liquid crystal thermography [11], is diffraction-limited to about 1 μm. This is insufficient to probe submicrometer vias in the size range of 0.1–0.5 μm. Near-field optics can be employed to overcome the diffraction limit [12], but it is still under development. A new thermometry technique, called scanning Joule expansion microscopy (SJEM), has recently been developed with spatial resolution in the sub-0.1 μm range [13]–[15]. In this letter, SJEM is used to study the thermal characteristics of small geometry W-plug vias.

II. Experimental

Fig. 1 shows the schematic diagram of the SJEM system. An atomic force microscope (AFM) is used to bring a sharp tip into force-controlled contact with the sample surface and perform a raster scan. The sample was attached to a temperature controller (maintained at room temperature), and then mounted on the AFM piezo scanner. A sinusoidal or pulsed voltage is applied to the electrically conducting sample (W-Via) which produces

sample Joule heating and temperature rise, resulting in sample thermal expansion. The AFM photodiode detects the cantilever deflection due to both expansion and sample topography. Since the feedback controller of the AFM has a bandwidth of 5 kHz, the photodiode signal below 5 kHz is processed for feedback control of the z-piezo to image surface topography under constant tip-sample force or cantilever deflection. The Joule heating frequency is kept above 5 kHz to avoid feedback response. The lock-in amplifier is tuned to the Joule heating frequency, which detects only the expansion signal and provides this to an auxiliary AFM channel to form the expansion image. The system can also be operated without feedback in which case the heating frequency can be below the controller bandwidth.

The via structures were fabricated in a state-of-the-art 0.25-μm industrial CMOS process flow employing chemical mechanical polishing (CMP) for planarization. The samples used in the experiments contained 0.6 μm-thick Al-Cu interconnects (with top and bottom layers of 0.05 and 0.1 μm-thick TiN) at two levels of metallization that were separated by a layer of 0.9-μm-thick silicon dioxide. These interconnects crossed each other forming an overlapping region and were bridged in this region by a single W-plug via with diameter $d = 0.4$ μm. Both levels of interconnects had a width of 1.6 μm. The samples were coated with a passivation layer of 1.0-μm thick silicon dioxide followed by a capping layer of 0.3-μm thick ilicon nitride. Since the thermal expansion coefficients of silicon dioxide and silicon nitride are very low, a 0.28 μm thick film of poly methyl methacrylate (PMMA) was spin coated on top of the passivation layer to amplify the expansion signal [13]–[15]. The thermal expansion coefficient of PMMA was measured to be $(65.9 \pm 3.3) \times 10^{-6}$ K^{-1}. The noise in the expansion measurements was found to be 1.53×10^{-12} m in a 26 Hz bandwidth,[1] producing a temperature resolution of about 0.08K.

III. Thermal Characterization Results

Fig. 2 (top) shows the spatial dc temperature profile around the via sample. The dc temperature contour image (center) shows the hot region on top of the via. Although the vias were 0.4 μm in diameter, diffusion in the passivation layers spread the temperature peak to about 10 μm at full-width half-maximum. It must be noted that despite this lateral spread, the temperature drop across the thickness of the passivation layer and the PMMA film can be expected to be quite small. This is because the temperature rise exponentially decays from the heat source with the decay length given by $\sqrt{\alpha/\pi f}$ where α is the thermal diffusivity of the material and f is the applied frequency. The thermal diffusivity of PMMA is the lowest of the three passivation materials, and is $\sim 10^{-7}$ m^2/s [16]. Hence, if the modulation frequencies are kept below 50 kHz, the penetration depth should be larger than 0.8 μm, which is much larger than the PMMA film thickness.

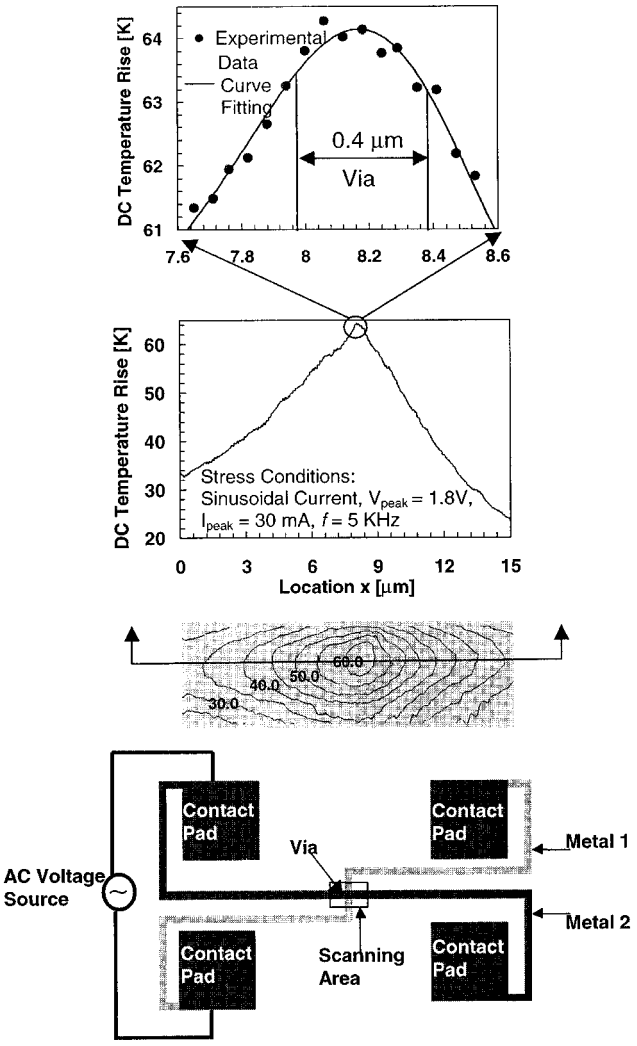

Fig. 2. Spatial dc temperature profile and the dc temperature contour map around the 0.4 μm W-plug via sample. The peak current density in the via and in the interconnects are 2.39×10^7 A/cm^2 and 3.13×10^6 A/cm^2, respectively. The dc temperature rise was estimated from the SJEM measurements of ac temperature rise using the analysis discussed in the text. Also shown is the top-view of the via sample. The box indicates the scanning area of the AFM cantilever.

In addition to an ac temperature rise under an ac bias, there is also a dc temperature rise due to the RMS power dissipation. The dc temperature rise is often much higher than the ac component and is, therefore, of interest. Since SJEM measures only the ac component, estimation of the dc component requires analysis. The thermal behavior follows a first-order system [17] and is characterized by a time constant τ. Hence, the maximum ac and dc temperature rises can be related as $T_{\rm ac} = T_{\rm dc}/\sqrt{1 + (4\pi f\tau)^2}$ [18]. The inset in Fig. 3 plots experimental data indicating this behavior and yields a time constant $\tau = 26$ μs. Using this first-order analysis, $T_{\rm dc}$ was found as a function of *sinusoidal* current and plotted in Fig. 3, where the $T_{\rm dc} \propto I^2$ behavior can be seen.

The internal time constant of the W-plug via, $\tau_{\rm via} = d^2/\alpha_W$, is on the order of 1 ns, where d is the via diameter,

[1]This bandwidth of lock-in amplifier was used for SJEM experiments, which is of interest here. The reason to choose 26 Hz as bandwidth is described in [14]. For compatibility between the lock-in bandwidth Δf and the AFM scan rate $f_{\rm AFM}$, the relation $\Delta f = N f_{\rm AFM}/2\pi$ Hz ($N = 256$) should be used, where N is the number of data points per line. Considering the trade-off between imaging speed and noise amplitude, a threshold scan rate $f_{\rm AFM}$ of 0.638 Hz was chosen, therefore $\Delta f = 26$ Hz ($N = 256$).

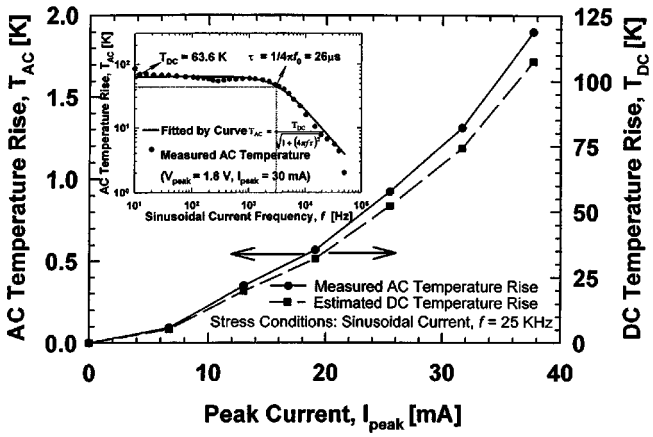

Fig. 3. Measured ac temperature rise and the corresponding estimated dc temperature rise under different sinusoidal current stress on top of the via. The electrical resistances of the W-plug vias were measured by a four-point probe technique to be about 3.6 Ω at 25 °C. The dc temperature rise was estimated from the measured ac temperature rise using the method described in the text and also shown in the inset. The experimental data below $f = 5$ kHz in the inset was obtained without feedback.

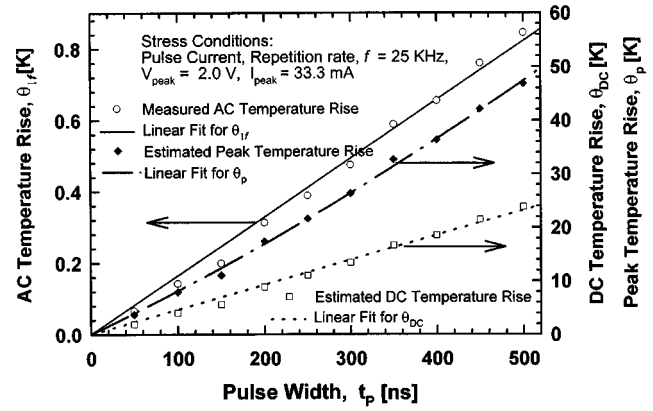

Fig. 4. First harmonic, dc (average) and peak temperature rise on top of the via as a function of the pulsed width of applied pulsed current.

$\alpha_W = 6.83 \times 10^{-5}$ m^2/s is the thermal diffusivity of W. Hence, the observation of $\tau = 26$ μs suggests that the surrounding materials, composed mainly of oxide and nitride, must dominate the thermal resistance. To study its thermal characteristics under a *pulsed* bias, experiments were conducted at different pulse widths, $t_p = 50$–500 ns, with a repetition rate of $f = 25$ kHz and pulse amplitude of 2 V. The first harmonic of the via temperature rise, θ_{1f}, at 25 kHz was measured using SJEM. Fig. 4 shows that θ_{1f} varies linearly with pulse width, in accordance with the Fourier analysis of heat conduction in a first-order system, which suggests that $\theta_{1f} = ((I_{\rm peak}^2 R)/(C))\,((f\tau)/(\sqrt{1+(2\pi f\tau)^2})t_p)$ [18], where $I_{\rm peak}$ is the peak current, R and C are the electrical resistance and thermal capacitance of the via, respectively. The dc temperature rise, $\theta_{\rm dc}$, and the peak temperature rise, θ_p can be found by this analysis to be $(\theta_{1f})/(\theta_{\rm dc}) = (1)/(\sqrt{1+(2\pi f\tau)^2})$ [18] and $(\theta_{\rm dc})/(\theta_p) = (f\tau)[1-\exp(-1/f\tau)]$ [18], which are also shown in Fig. 4.

IV. Conclusions

In conclusion, this work demonstrates that SJEM can be used to measure the spatial temperature distribution around single submicrometer vias and to study their steady-state and dynamic thermal behavior under sinusoidal and pulsed current stress. The thermal time constant of the via structure has been determined from the measured ac frequency dependence of the temperature rise. Furthermore, the average (dc) and peak temperature rise under pulsed stress condition have been estimated from the measured first harmonic temperature rise. The sub-100 nm resolution of SJEM can be potentially used to thermally probe current crowding effects in deep submicron interconnect and via structures.

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