A Quasi-Analytical SET Model for Few Electron Circuit Simulation

Santanu Mahapatra, Adrian Mihai Ionescu, *Member, IEEE,* and Kaustav Banerjee, *Member, IEEE*

***Abstract*—A novel quasi-analytical model for single electron transistors (SETs) is proposed and validated by comparison with Monte-Carlo (MC) simulations in terms of drain current and transconductance. The new approach is based on the separate modeling of the tunneling and thermal components of the drain current, and verified over two decades of temperature. The model parameters are physical and an associated parameter extraction procedure is also reported. The model is shown to be accurate for SET logic circuit simulation in both static and dynamic regimes and is attractive for hybrid (SET-CMOS) circuit co-simulation.**

***Index Terms*—Few-electron circuit, semiconductor device modeling, SET-CMOS co-simulation, single-electron transistor.**

I. Introduction

SINGLE Electron Transistors (SETs), which are attractive candidates for post-CMOS VLSI and hybrid (CMOS-SET) ICs due to their ultra-small size and low power dissipation, demand accurate analytical models in order to obtain more insights into SET characteristics and to design SET/hybrid circuits, rather than Monte-Carlo (MC) simulation [1], [2] or macro-modeling [3], [4]. This letter reports on a novel model (named **MIB**, after the authors of this paper) for the drain current of SETs and the associated parameter extraction procedure. The proposed approach is different and simpler than that presented by Uchida *et al.* [5], and is able to explicitly describe the effect of the second gate on the drain current (which is critical for SET logic circuits [6]–[8]). MIB is validated in static and dynamic regimes, at both device and logic circuit levels, by comparison with the largely accepted MC simulator SIMON [1] with realistic values of the device parameters [7], [8] over two decades of temperature (100 mK to 10 K).

II. MIB Modeling and Parameter Extraction

MIB is founded on the "orthodox theory of single electron tunneling" [9]. It uses two basic assumptions: i) $|V_{DS}| \leq e/C_{\Sigma}$, where V_{DS} is the SET drain-to-source voltage, e is the elementary electronic charge and C_{Σ} is the total capacitance associated with the SET island to ground, and ii) the interconnect capacitance associated with the gate, source and drain terminals are much larger than the device capacitance. In the proposed approach, the SET drain current, I_{DS}, is modeled via two components: i) the tunneling current, I_{DSU}, which is independent of temperature, T, and ii) the thermal current, I_{DSTH}, which fully include the effect of temperature as

$$I_{DS} = I_{DSU} + I_{DSTH} = \frac{I_D I_S}{I_D + I_S} + I_{DSTH} \qquad (1)$$

where I_{DSU} is subsequently modeled based on the individual calculations of the drain I_D, and source I_S tunneling components (considered to be proportional to the tunneling rates [10]: at zero temperature, the transmission probability $\Gamma(\Delta F) = -\Delta F/(e^2 R_T)$ for $\Delta F < 0$, and $\Gamma(\Delta F) = 0$ for $\Delta F \geq 0$, where ΔF is the generalized Gibbs energy [1] and R_T is the tunnel resistance). Thus, I_{DSU} is modeled (as half of the *harmonic mean* of I_S and I_D) based on the assumption that, if the external bias can provide a potential higher than $e/(2C_{\Sigma})$ across a junction, then the electron tunneling is possible, otherwise not. It does not consider any effect of the thermal energy. However, in reality, even if the external bias across the junction is less than $e/(2C_{\Sigma})$, some electron tunneling is still possible if they have sufficient thermal energy (kT). In this work, the current due to thermal effects is considered as a temperature dependent leakage current, I_{DSTH}. The proposed physical/analytical linear expressions of I_D and I_S, dictated by the island potential V_{island}, that controls the electron-tunneling-probability, are detailed in Fig. 1. The

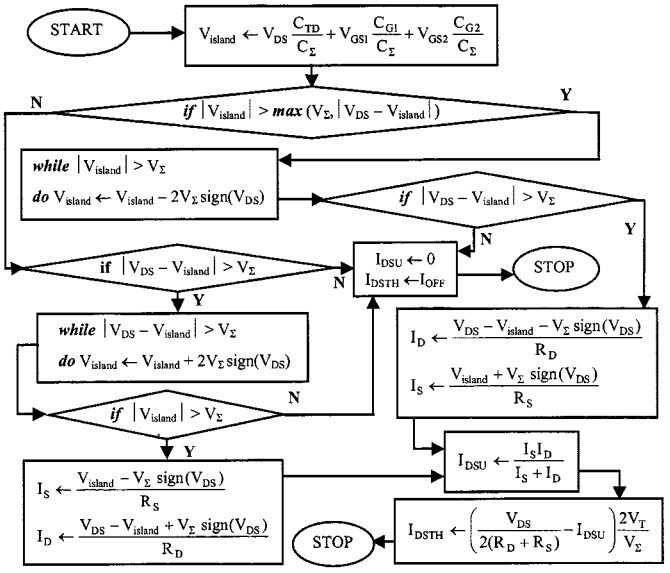

Fig. 1. Simplified flow chart of the computing subroutine f for SET currents I_{DSU} and I_{DSTH}. Here, the sign (V_{DS}) function holds the sign of V_{DS}, $\max(a, b)$ subroutine returns the maximum between a and b, V_T is the thermal voltage ($=kT/e$, k is the Boltzmann's constant), $V_{\Sigma} = e/(2C_{\Sigma})$, and $C_{\Sigma} = C_{TS} + C_{TD} + C_{G1} + C_{G2}$.

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S. Mahapatra and A. M. Ionescu are with the Electronics Laboratory (LEG), Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland (e-mail: santanu.mahapatra@epfl.ch; Adrian.Ionescu@epfl.ch).

K. Banerjee is with the Center for Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: kaustav@cis.stanford.edu).

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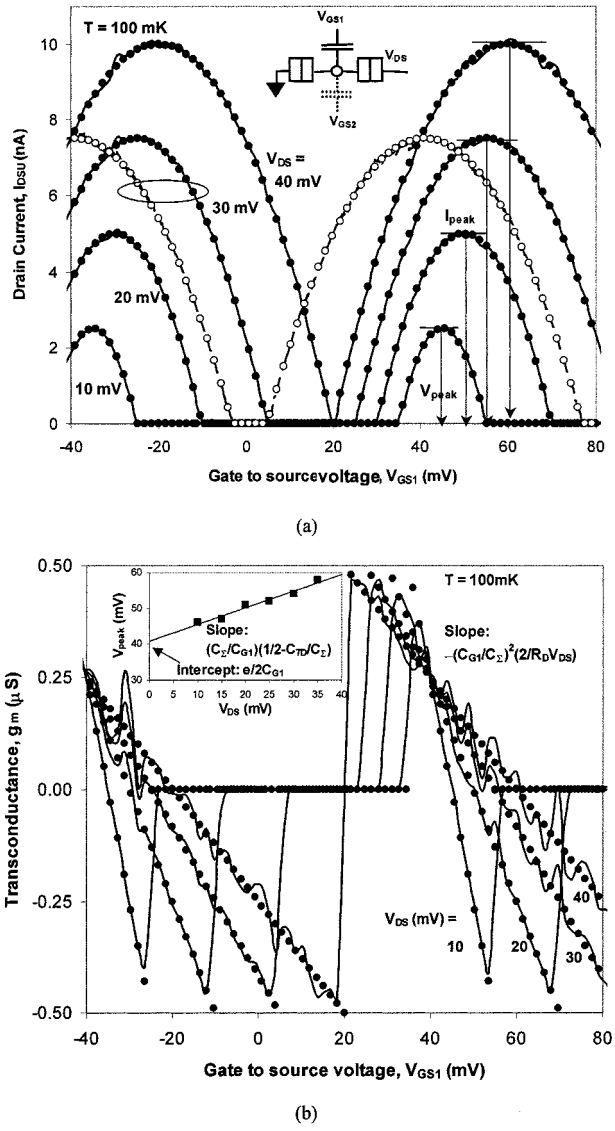

Fig. 2. (a) I_{DSU} model validation with $C_{G1} = 2$ aF, $R_S = R_D = 1$ MΩ, $C_{TS} = C_{TD} = 1$ aF, and for $V_{DS} = 10$ mV, 20 mV, 30 mV, and 40 mV at $T = 100$ mK, where the symbol "•" represents MIB model and the solid line represents SIMON simulations for a single gate SET. In the same figure (for $V_{DS} = 30$ mV), "○" represents MIB and the dotted line represents SIMON simulations for *a double gate SET* with $C_{G2} = 0.8$ aF and $V_{GS2} = 50$ mV. (b) Single gate SET transconductance g_m ("•" = MIB model, thick solid line = SIMON) as a function of V_{GS1} [for different V_{DS} and the same parameters as in Fig. 2(a)] obtained by numerical derivation of the characteristics that appear in Fig. 2(a). The ***inset*** of Fig. 2(b) shows a linear plot of V_{peak} versus V_{DS} for model-parameter extraction using a self-consistent validation method. The extraction assumes that $C_{TD} = C_{TS}$, $I_{peak} \leq e/\{2C_\Sigma(R_D + R_S)\}$ and corresponds to single-gate SET.

overall calculation of the drain current is performed using: $I_{DS} = f(V_{GS1}, V_{GS2}, V_{DS})$, where V_{GS1} and V_{GS2} are the gate-to-source voltages of the two SET gates and f is a computing subroutine (reported in Fig. 1). It is worth noting that all the model parameters of I_{DSU} are physical: i) drain and source tunneling capacitances, C_{TD} and C_{TS}; ii) first and second gate capacitances, C_{G1}; and C_{G2}; and iii) drain and source tunnel junction resistances, R_D and R_S.

Special attention is paid to model I_{DSTH} in order to extend the validity of the model over a larger temperature range, as given in Fig. 1. I_{DSTH} can be calculated using the following proposed quasi-empirical equations:

$$I_{DSTH} = \begin{cases} (I_{peak} - I_{DSU})\dfrac{2V_T}{V_\Sigma} \\ \quad \text{when } I_{DSU} \neq 0 \end{cases} \tag{2a}$$

$$I_{DSTH} = \begin{cases} I_{OFF} = \dfrac{V_T}{2(R_D+R_S)} \ln\left(1+e^{1-(V_\Sigma/nV_T)}\right), \\ \quad \text{when } I_{DSU} = 0 \end{cases} \tag{2b}$$

where n is a fitting coefficient and $I_{peak} = V_{DS}/2(R_D + R_S)$ [1]. The off-state current I_{OFF}, which is a function of temperature and the device-size, has been checked to agree with MC Simulation over two decades of temperature (0.1 K to 10 K) for a fixed value of $n = 10$.

The various plots reported in Fig. 2(a) for single and double-gate SET configurations at various V_{DS} demonstrate the accuracy of the proposed model. MIB is further validated in terms of SET transconductance ($g_m = dI_{DS}/dV_{GS1}$): the quasi-linear plot in Fig. 2(b) shows the ability of MIB to accurately describe the first derivative of the drain current.

In order to extract the model physical parameters from real measured data, if a symmetrical device is assumed, the drain and source resistances can be extracted as $R_D = R_S = V_{DS}/4I_{peak}$, where I_{peak} is the peak current, as shown in Fig. 2(a). Additionally, if we denote by V_{peak} the minimum positive value of V_{GS1} [Fig. 2(a)] at which the peak appears, it follows that:

$$V_{peak} = \frac{e}{2C_{G1}} + \frac{C_\Sigma}{C_{G1}}\left(\frac{1}{2} - \frac{C_{TD}}{C_\Sigma}\right)V_{DS}. \tag{3}$$

Equation (3) suggests that the plot of V_{peak} versus V_{DS} is a straight line [see inset of Fig. 2(b)], the slope of which and whose intercept with the vertical axis can be used to extract C_{TD} and C_{G1}, respectively. If the second gate of the SET is active or the device is asymmetrical in terms of drain and source tunneling capacitances, the parameter extraction needs to exploit also the $g_m - V_{GS}$ plot, the negative slope of which is modeled as a function of C_G, C_Σ and R_D [Fig. 2(b)]. MIB and extraction procedure have been validated using a self-consistent approach: a set of realistic model parameters are used as inputs to the MC simulator (SIMON) and the SET is simulated, following which, the parameters can be estimated by applying the proposed extraction procedure to the simulated characteristics. One should note that in Fig. 2(a), I_{DSU} (and not I_{DS}) is plotted along with the values obtained from the SIMON [1] for different values of V_{DS} at $T = 100$ mK, which reveals that although I_{DSU} is independent of temperature, it is able to correctly predict the drain current for a low T [i.e., when $T \ll e^2/(kC_\Sigma)$]. At higher temperatures, I_{DSTH} must be added to I_{DSU} in order to provide a more accurate model. We have fully validated our model up to a temperature of $e^2/(40C_\Sigma k)$ [11], and observed that as the temperature increases, the on-state to off-state current ratio decreases and, hence the performance of the SET as a digital switch degrades.

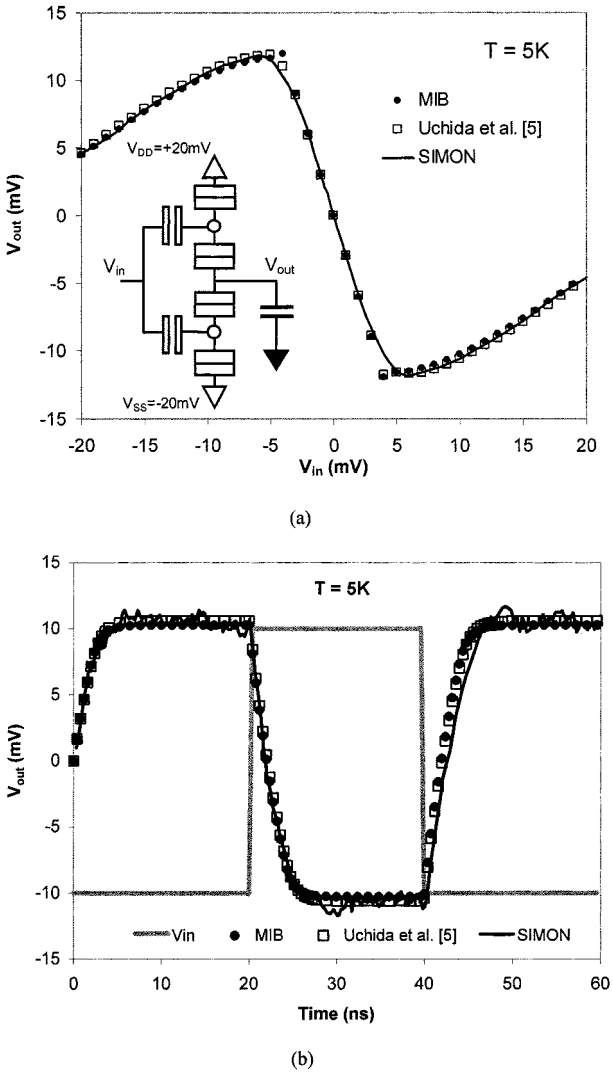

Fig. 3. (a) Static and (b) transient characteristics of an SET inverter cell, as predicted by MIB, SIMON, and Uchida's model [5]. The SET parameters are $R_S = R_D = 1$, MΩ, $C_{TD} = C_{TS} = 1$ aF, $C_{G1} = 3$ aF, and the output load capacitor is $C_L = 1$ fF.

III. Circuit Simulation

Special attention is also paid in order to demonstrate the usefulness of MIB for SET circuit simulation. Static and transient responses of an inverter cell are successfully predicted [Fig. 3(a) and (b)]. Comparison and good agreement with MC simulation and Uchida's analytical model demonstrates the accuracy of our physical analytical model in both static and dynamic regimes.

IV. Conclusion

A new model (MIB) for the drain current of SET devices has been reported and validated using realistic parameters up to a temperature of $T = e^2/(40C_\Sigma k)$ (e.g., 5 K for $C_\Sigma = 5$ aF) for both static and dynamic operations. MIB has some clear advantages: i) it is simple, physically based, and able to accurately describe both the drain current and the transconductance, ii) it is able to incorporate the effect of the second gate; and iii) it allows separate analytical descriptions of the SET tunneling (I_{DSU}) and the thermal (I_{DSTH}) currents. Moreover, for $T \ll e^2/(kC_\Sigma)$, solely the tunneling component, I_{DSU}, is able to accurately predict the overall SET drain current, I_{DS}, and therefore can save significant computation time for circuit simulation because of its simple, linear mathematical formulation. Finally, the model is shown to be sufficiently accurate for the simulation of few-electron logic circuits in both static and dynamic regimes and can also be efficiently used for the simulation of hybrid (SET-CMOS) circuit architectures.

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References

[1] C. Wasshuber and H. Kosina, "SIMON—A simulator for single-electron tunnel devices and circuits," *IEEE Trans. Electron Devices*, vol. 44, pp. 937–944, Aug. 1997.

[2] R. H. Chen, A. N. Korotkov, and K. K. Likharev, "A new logic family based on single-electron transistors," in *Proc. Device Research Conf.*, Charlottesville, VA, 1995, pp. 44–45.

[3] Y. S. Yu, S. W. Hwang, and D. Ahn, "Macromodeling of single electron transistors for efficient circuit simulation," *IEEE Trans. Electron Devices*, vol. 46, pp. 1667–1671, Aug. 1999.

[4] R. Haar, R. H. Klunder, and J. Hoekstra, "SPICE model for the single electron tunnel junction," in *ICECS Tech. Dig.*, vol. 3, pp. 1445–1448.

[5] K. Uchida, K. Matsuzawa, J. Koga, R. Ohba, S. Takagi, and A. Toriumi, "Analytical single-electron transistor (SET) model for design and analysis of realistic SET circuits," *Jpn. J. Appl. Phys. B*, pt. 1, vol. 39, no. 4, pp. 2321–2324, 2000.

[6] S. J. Ahn and D. M. Kim, "Asynchronous analogue-to-digital converter for single-electron circuits," *Electron. Lett.*, vol. 34, no. 2, pp. 172–173, 1998.

[7] A. Fukushima, A. Iwasa, and A. Sato, "Single electron transistor with two gate inputs," in *Proc. Precision Electromagnetic Measurements Digest*, 2000, pp. 591–592.

[8] Y. Ono and Y. Takahashi, "Single electron pass transistor logic and its application to a binary adder," in *Proc. Symp. VLSI Circuits*, 2001, pp. 63–66.

[9] K. K. Likharev, "Single electron devices and their applications," *Proc. IEEE*, vol. 87, pp. 606–632, Apr. 1999.

[10] X. Wang and W. Porod, "Analytic I–V model for single-electron transistors," in *IWCE Glasgow*, 2000, pp. 71–72.

[11] *Ext. Abst. 1994 Int. Conf. Solid-State Devices and Materials*, Tokyo, Japan, 1994, p. 328.