2D Electronics: Graphene and Beyond

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According to the International Energy Agency:

i) Electronic devices currently account for 15% of household electricity consumption

ii) Energy consumed by information and communications technologies as well as consumer electronics will **double by 2022 and triple by 2030** to 1,700 Terawatt hours

= the entire total residential electricity consumption of US and Japan in 2009!!!

With improved efficiency of IT usage, around 30% reduction per year in GHG is achievable, which is equivalent to gross energy and fuel savings of **315 billion U.S. dollars!!!**
On-die global interconnect energy scales slower than compute. On-die data movement energy will start to dominate.

**DRAGON ENERGY**

**Need Green Interconnects**

**Need Green Transistors**

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**Vampire Power**

<table>
<thead>
<tr>
<th>Device Description</th>
<th>Average Watts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mobile Phone Charger (On, Charging)</td>
<td>50</td>
</tr>
<tr>
<td>Desktop Computer (Sleep)</td>
<td>37.5</td>
</tr>
<tr>
<td>Laptop Computer (Sleep)</td>
<td>25</td>
</tr>
<tr>
<td>LCD Computer Display (Sleep)</td>
<td>12.5</td>
</tr>
<tr>
<td>CRT Computer Display (Sleep)</td>
<td>0</td>
</tr>
<tr>
<td>Set-top Box, digital cable with DVR (Off by Remote)</td>
<td>50</td>
</tr>
<tr>
<td>Cable Modem (Standby)</td>
<td>37.5</td>
</tr>
<tr>
<td>Game Console (Ready)</td>
<td>25</td>
</tr>
</tbody>
</table>

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**S. Borkar (Intel)**

- Interconnect Energy: 6X
- Compute Energy: 1.6X

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So, How can we design Green Electronics?

I will use 2D electronic materials:
Graphene and Beyond
2D Electronic Materials

**Graphene family**
- h-BN (dielectric) ($E_g > 5eV$)
- Silicene (semiconductor) ($E_g = 0.6$ eV, experimentally)
- Graphene (semi-metal) ($E_g = 0eV$)

**TMD family**
- NbSe$_2$, etc (superconductor)
- MoS$_2$, WSe$_2$, etc (semiconductors)
- VO$_2$, VS$_2$, etc (metals)
- CrO$_2$, CrS$_2$, etc (half-metals) ($0 < E_g < 1$ eV)

**Other families**
- Bi$_2$Sr$_2$Co$_2$O$_8$
- Ti$_2$C, Ti$_2$CF$_2$, Ti$_2$C(OH)$_2$
- etc

2D family tree
Advantages of 2D – Ultra Thin Body

- Covalent bonds
- band gap varies uncontrollably with thickness
- cause variations when scaled

3D
Potato-like

2D
Onion-like
Layered structure
- Can be exfoliated
- Van der Waals force
- few Å

- intrinsic thickness < 1nm/L
- controllable precise band gap
- enable scaling in nm regime
- lead to novel applications

Covalent bonds
Advantages of 2D – Ultra Thin Body (contd.)

- mobile carriers exist at >1 nm away from the surface
- limited gate electrostatics
- short-channel effects

- carriers confined to <1 nm thickness
- excellent gate electrostatics
- reduce short-channel effects

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Advantages of 2D – Pristine Interface

3D

Unsaturated atoms

Dangling bonds (may form traps)

- suffer from interface traps
- Fermi level pinning, increased scattering, etc.

2D

saturated atoms

No dangling bonds (pristine interface)

- fewer interface traps
- increase stability/reliability
Forms of Carbon...

Carbon atom can form several distinct types of valence bonds.

- 0D: fullerenes
- 1D: nanotube
- 1D: nanoribbon
- 2D: graphene
- 3D: diamond
- 3D: graphite
2D and 1D Carbon Nanomaterials

Graphene (Thinnest 2D Crystal)

Single-wall CNT (1D)

Multi-wall CNT (1D)

Monolayer Graphene NanoRibbons (GNRs) (1D)

Multi-layer GNR (1D)

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Crystal & Band Structure of Graphene

- Zero bandgap
- Linear $E$-$k$ near Dirac point
- Close to zero effective mass
- Electrons and holes are equal

$E(k_x, k_y) - E_F i = \pm \hbar v_F \sqrt{k_x^2 + k_y^2}$
Chiralities and Band Gap Tuning of Graphene

Graphene NanoRibbon (GNR)

Graphene

Simulations (n = 1, 2, ...):
- Experimental
- Empirical

- ZZ
- ac, \( N_W = 3n - 1 \)
- ac, \( N_W = 3n \)
- ac, \( N_W = 3n + 1 \)

\[ E_{\text{g}}(E) \]

Bandgap opening


ESSDERC, Bucharest, Sep. 19, 2013.
# Superb Properties of CNT and Graphene

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>Cu</th>
<th>SWCNT</th>
<th>MWCNT</th>
<th>Graphene or GNR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max current density (A/cm²)</td>
<td>-</td>
<td>10⁷</td>
<td>&gt;1x10⁹</td>
<td>&gt;1x10⁹</td>
<td>&gt;1x10⁸</td>
</tr>
<tr>
<td>Melting point (K)</td>
<td>1687</td>
<td>1356</td>
<td>3800 (graphite)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tensile strength (GPa)</td>
<td>7</td>
<td>0.22</td>
<td>22.2 ± 2.2</td>
<td>11-63</td>
<td></td>
</tr>
<tr>
<td>Mobility (cm²/V-s)</td>
<td>1400</td>
<td></td>
<td>&gt;10000</td>
<td></td>
<td>&gt;10000</td>
</tr>
<tr>
<td>Thermal conductivity (x10³ W/m-K)</td>
<td>0.15</td>
<td>0.38</td>
<td>1.75-5.8</td>
<td>3.0</td>
<td>3.0-5.0</td>
</tr>
<tr>
<td>Temp. Coefficient of Resistance (10⁻³ /K)</td>
<td>-</td>
<td>4</td>
<td>&lt;1.1</td>
<td>-1.37</td>
<td>-1.47</td>
</tr>
<tr>
<td>Mean free path (nm) @ room temp.</td>
<td>30</td>
<td>40</td>
<td>&gt;1,000</td>
<td>25,000</td>
<td>~1,000</td>
</tr>
</tbody>
</table>
Graphene Preparation

**Top-down approach**
- Mechanical exfoliation of graphite
- Liquid phase exfoliation

**Bottom-up approach**
- CVD from hydrocarbon (Large-area, high quality)
- Epitaxial growth on SiC
- Organic synthesis

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**Graphene Transfer**

- Carrier Layer (PMMA/PDMS)
- Releasing graphene
Graphene FETs with Record Mobility:
- synthesized using CVD;
- controlled synthesis of monolayer and bilayer graphene demonstrated

Controllable Synthesis of AB Stacked Bilayer Graphene

- Wafer scale AB stacked bilayer graphene
- >98% AB stacking order with high quality
- Most reliable method of synthesizing AB stacked BLG

W. Liu et al., UCSB/Rice, (2013) (under review)

- Typical electron diffraction pattern of AB stacked bilayer
- Synthesized bilayer graphene shows high ON/OFF ratio
Applications of Graphene

Passive Devices
- Inductor
- Interconnect
- Transparent Electrode
- Floating-Gate Memory

Active Devices
- FETs (Graphene FET, GNRTFET, etc.)
- All-graphene Logic Circuit
- NDR-based SRAM
- Inverter
- Inductor
- VDD
- GND
- Vout
- Vin
- Floating-Gate Memory
- NDR-based SRAM
- Transparent Electrode
- Inductor
- Interconnect
Interconnect Power Dissipation

- **Interconnect**: 51%
- **Logic (gate capacitance)**: 34%
- **Logic (diffusion capacitance)**: 15%

Global interconnects must be optimally pipelined to meet clock period and power criteria.


N. Magen et al., SLIP, pp. 7-13, 2004.
Low Power Interconnects

Inverter insertion configuration:

Lower delay allows larger distance between inverters, thus reduces the power

If delay is kept identical to Cu optimal delay CNT/GNR global interconnect could save ~50% power!!

High-Q CNT/GNR based Low-Loss Inductors

- CNTs can provide better performance than Cu
- MWCNT gives 2.4X higher Q factor than that of Cu
- GNR shows an improvement of:
  ~20% over Cu
  ~50% over 1/3 metallic SWCNT

H. Li and K. Banerjee, *TED*, vol. 56, no. 9, 2009
Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects

Hong Li, Student Member, IEEE, Chuan Xu, Student Member, IEEE, Navin Srivastava, Student Member, IEEE, and Kaustav Banerjee, Senior Member, IEEE

Abstract—This paper reviews the current state of research in carbon-based nanomaterials, particularly the one-dimensional (1-D) forms, carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), whose promising electrical, thermal, and mechanical properties make them attractive candidates for next-generation integrated circuit (IC) applications. After summarizing the basic physics of these materials, the state of the art of their interconnect-related fabrication and modeling efforts is reviewed. Both electrical and thermal modeling and performance analysis for various CNT- and GNR-based interconnects are presented and compared with conventional interconnect materials to provide guidelines for their prospective applications. It is shown that single-walled, double-walled, and multiwalled CNTs can provide better performance than that of Cu. However, in order to make GNR interconnects comparable with Cu or CNT interconnects, both intercalation doping and high edge-specularity must be achieved. Thermal analysis of CNTs shows significant advantages in tall vias, indicating their promising application as through-silicon vias in 3-D ICs. In addition to on-chip interconnects, various applications exploiting the low-dimensional properties of these nanomaterials are discussed. These include chip-to-packaging interconnects as well as passive devices for future generations of IC technology. Specifically, the small form factor of CNTs

First Demonstration of Long Horizontal CNT Bundle Interconnects @ UCSB


- Longer than 120 µm horizontal CNT bundle
- Thickness ranges from 100nm – 2 µm
First Demonstration of Horizontal CNT Bundle Based Manhattan Structure


First demonstration of a Kanji character using horizontal CNT bundles

100 µm
First Demonstration of Carbon Nanotube Inductor


- First time demonstration of CNT bundle based inductor
- Single turn with diameter 100-150 μm
- Segment width 10-30 μm, thickness 300nm - 2 μm
**Transparent Electrodes**

- **Mainstream: ITO** *(limited)*
  - Limited Indium supply
  - Fabrication/Integration Cost
  - Lack of flexibility

- **Alternatives (under research)**
  - Metal grids
  - Metal oxides
  - Thin film

- **Industry requirement:**
  - Optical transmission >90%
  - Electrical conductivity <10 Ω/sq

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**Graphene Electrode Advantages**

- Low cost fabrication (CVD)
- Large-area high quality sheets
- High electrical conductivity
- High mobility
- High optical transparency
- Mechanical flexibility
- High thermal stability
- Impermeability to moisture

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**Transparent electrode market by year**

![Graph showing transparent electrode market by year](image1)

**Graph showing transmittance (%)**

![Graph showing transmittance (%)](image2)
Graphene Electrode Applications

**Touch Panels**

**Solar Cells**

**Light Emitting Devices**

**Light Sensors**

**Display**
First ESD Characterization of Graphene (UCSB/Intel)


- Breakdown current: 4.5 mA/µm for 100 ns TLP and 8 mA/µm for 10 ns TLP
- Maximum Current density: 2-5x 10^8 A/cm^2
- Graphene devices show clear “open cut” in the channel after breakdown
### CMOS Transistor Scaling Issue

<table>
<thead>
<tr>
<th>Dimension scaling</th>
<th>Increase transistor density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide thickness scaling</td>
<td>Higher Performance</td>
</tr>
<tr>
<td>$V_{DD}$ scaling</td>
<td>Energy Efficiency</td>
</tr>
</tbody>
</table>

#### Energy Efficiency

$$E \propto V_{DD}^2$$

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**Aggressive scaling leads to an exponential increase in leakage power!!!**

- **High Off Current**
- **Low Off Current**

**Solution to leakage Issue:**

- Steeper turn on

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**Diagram Notes:**

- $\log(I_D)$ vs. $V_G$
- $V_{DD}$ scaling

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Ideal-Switch: Greenest Transistor!

An ideal switch

Solid-state devices

\[ S = \frac{\Delta V_{gs}}{\Delta \log(I_d)} \]

\( \Delta V_{gs} \)
\( \Delta \log(I_d) \)
\( V_{th} \)

Gate voltage (\( V_{gs} \))

Drain current (log(\( I_d \)))

Subthreshold Swing (\( S \)) should be as low as possible!!
MOSFET vs. Tunnel-FET

**ON State**
- **MOSFET**
  - ON Current
  - Source \( E_V \) to Drain \( E_V \)
  - \( S \geq 60 \text{ mV/decade} \)

- **Tunnel-FET**
  - ON Current
  - Source \( E_V \) to Drain \( E_V \)
  - \( S \ll 60 \text{ mV/decade} \)

**OFF State**
- **MOSFET**
  - OFF Current
  - Source \( E_C \) to Drain \( E_C \)
  - Leakage

- **Tunnel-FET**
  - OFF Current
  - Source \( E_C \) to Drain \( E_C \)
  - Nearly No Leakage

**Notes**
Due to excellent electrostatics, band gap tunability and direct band gap, GNR is a great material for Tunnel-FETs....

All-Graphene Monolithic Logic Circuits

Performance Evaluation

- **22nm-CMOS (Low Power Model)**
- **22nm-CMOS (High Performance Model)**
- **All-Graphene Monolithic Logic Circuits**

### Parameters
- **Inverter Noise Margin**
- **Inverter Gain**
- **Inverter Delay**
- **Power Consumption**

#### Graphs
- **Noise Margin (V_{DD})**
- **Inverter Gain**
- **Minimum Delay (s)**
- **Power Consumption (W)**

**Values**
- **22nm-CMOS (Low Power Model)**
- **22nm-CMOS (High Performance Model)**
- **All-Graphene Monolithic Logic Circuits**

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GNR based Negative Differential Resistance (NDR) Device

- Top and bottom gates dope the channel electrostatically
- Low gap states
  - Pristine GNRs
  - No dopants
- Bottom gate connected to drain
- Fixed voltage on top gate
- High current density: 700\(\mu\)A/\(\mu\)m


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Compact SRAM Cell based on GNR NDR Devices


- Complementary devices
- Currents matching in n- and p-type devices
- An access transistor used for read/write
- Minimum $V_{DD}$: $V_{valley}$
- n-device keeps $V_{OUT} \approx 0$
- p-device keeps $V_{OUT} \approx V_{DD}$

Stable points
Low voltage operation

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First Proposal for Tunnel-FET Biosensors: Ultra-Low Power and Ultra-Sensitive

TFET Biosensor in Research Highlights of Nature Nanotechnology

FIELD-EFFECT TRANSISTORS
Biomolecular turn-ons

D. Sarkar and K. Banerjee

Transistors can make good biosensors. The usual approach is to functionalize the gate oxide of a field-effect transistor with receptors for specific, charged biomolecules. When these are captured, they modulate the conductance of the channel, which can be measured. Deblina Sarkar and Kaustav Banerjee of the University of California, Santa Barbara have now predicted that tunnel field-effect transistors could be used to make biosensors that are even better.

NATURE NANOTECHNOLOGY | VOL 7 | MAY 2012 | www.nature.com/naturenanotechnology
Beyond Graphene Electronic Materials – TMD Family

Transition Metal Dichalcogenides

- **Semiconductor** ($E_g$: 1-2 eV)
  - Example: MoS$_2$, WSe$_2$
- **Superconductor**
  - Example: NbSe$_2$
- **Half-metal** ($E_g$: 0-1 eV)
  - Example: CrO$_2$, CrS$_2$
- **Metal**
  - Example: VO$_2$, VI$_2$

- Layered material
- Hexagonal lattice

- ~50 members known
- $E_g$ up to 2.2 eV

$E_v$: valleys, $E_c$: conduction band
$1.8$ eV: MoS$_2$
$1.6$ eV: WSe$_2$
$1.1$ eV: MoTe$_2$
$2.2$ eV: SnS$_2$
Two-dimensional atomic crystals

K. S. Novoselov*, D. Jiang*, F. Schedin*, T. J. Booth*, V. V. Khotkevich*, S. V. Morozov†, and A. K. Geim**

- Demonstration of exfoliated MoS$_2$
- Measured mobility 0.5 $\sim$ 3 cm$^2$/Vs
- Low gate modulation

Crystal and Electronic Structures of MoS$_2$
Synthesis of MoS$_2$ – CVD Methods

Thermal decomposition of $(NH_4)_2MoSO_4$

Single crystalline MoS$_2$ directly grows on dielectric film ($Al_2O_3$, BN, SiO$_2$ et al.,) as the reactants

MoO$_3$ + S powders as the reactants

Mo film + S as the reactants


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Applications of TMD materials: TMD Transistors

- Demonstration of transistor performance boosting by using high-κ dielectrics

Contact resistance dominates TMD FET performance (1-3 order higher than that of CMOS)

Single-layer MoS$_2$ transistors

SS ~ 74 mV/dec
On/Off Ratio ~ $10^8$
Mobility ~ 200 cm$^2$/Vs
(15 after recent correction..)

ON current = 2.5uA/um
@ Vds = 0.5 V

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Three Main Issues in TMD Transistor Applications

- Contact
- Substrate (dielectric)
- Doping

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Main Issues 1: Contact
A Framework to Evaluate and Optimize Contacts to 2D Semiconductors

Step 1: Choosing Metals
- 

Step 2: Interface Modeling

Step 3: Density Function Theory (DFT) Calculation
- Mulliken Population
- Partial Density of States
- Effective Potential

Step 4: Contact Evaluation
- Orbital Overlap (Bonding)
- Schottky Barrier
- Tunnel Barrier

High Performance Monolayer n-type WSe$_2$ FET

Monolayer WSe$_2$ with a bandage of 1.6-1.7 eV
Optical contrast and Raman mapping can estimate thickness of few layer WSe$_2$

High mobility: $142 \, \text{cm}^2/\text{V.s}$
Record On Current: $210 \, \mu\text{A}/\mu\text{m}$

Main Issues 2: Doping of TMD

Currently there is no stable and reliable doping method for TMD semiconductors
• chemical doping: volatile
• electrostatic doping: raise new questions
  – manufacturability, alignment and additional parasitics

Chemical p-doping of single layered WSe$_2$ by NO$_2$

First Demonstration of MoS$_2$ FET Biosensor @UCSB

- 74-fold higher sensitivity than graphene
- Femto-molar detection
- Highly scalable

D. Sarkar, W. Liu, X. Xie, A. C. Anselmo, S. Mitragotri and K. Banerjee (under review)
Applications of TMD materials: Floating-Gate Transistors based on Graphene/TMD

Graphene floating gate
MoS$_2$ (WSe$_2$) channel
Gate dielectric (i.e. h-BN)

Advantages:

- Graphene as FG
  - Immune to cell-to-cell interference
- TMD as channel
  - Small Vth roll-off
  - Small SS

W. Cao, J. Kang, S. Bertolazzi, A. Kis and K. Banerjee (under review).

Selected 2D-nanocrystals can significantly extend the lifetime of the FG based memory cell
Applications of TMD materials: “All-2D” Hybrid Circuit Design Scheme

- utilize the promising properties of various 2D electronic materials
- future ultra-dense high-efficiency and low-power digital circuits
- a simple example:

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All-2D Heterostructures: Lateral & Vertical


Voltage transfer curve and gain

Vertical 2D inverter: MoS$_2$ as N-device; BSCO as P-device

fabrication of planar graphene/h-BN structure with controlled domain

graphene/h-BN transferred to PDMS
A creative child
We researchers

A future 2D “Legoland”

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Acknowledgments

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