Quasi-Analytical Modeling of Drain Current and Conductance of Single-Electron Transistors with MIB

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Abstract

A novel quasi-analytical model for Single Electron Transistors (SETs) is proposed and validated for both symmetric and asymmetric devices by comparison with Monte Carlo simulations in terms of both drain current and conductances. The proposed method is based on the separate modelling of the tunnelling and thermal components of the drain current, and verified over two decades of temperature. For the first time, accurate modelling of SET (trans) conductance is demonstrated. The model parameters are physical and an associated parameter extraction procedure is also reported. The model is shown to be accurate for SET logic circuit simulation in static and dynamic regimes and appears attractive for hybrid (SET-CMOS) circuit co-simulation.

1. Introduction

Single Electron Transistors (SETs), which attract considerable attention for post-CMOS VLSI and hybrid (CMOS-SET) ICs due to their ultra small size and low power dissipation, demand accurate analytical models in order to obtain more insights into SET characteristics and to design SET/hybrid circuits, rather than Monte-Carlo (MC) simulation [1, 2] or Macro Modelling [3, 4]. This work reports on a novel model (extension of our recent analytical model MIB [5]) for the drain current and conductances of both symmetric and asymmetric SET and the associated parameter extraction procedure. MIB is different and simpler than that presented by Uchida et al. [6], and is able to explicitly describe the effect of the second gate on the drain current (which is critical for SET logic circuits [7-9]) and equally applicable for both symmetric and asymmetric devices. MIB is validated in static and dynamic regimes, at both device and logic circuit levels, by comparison with the largely accepted Monte Carlo simulator SIMON [1] with realistic values of the device parameters [8, 9] over two decades of temperature (100 mK to 10 K).

2. Modelling and Parameter Extraction

MIB is founded on the "orthodox theory of single electron tunnelling" [10] with two basic assumptions: (i) $|V_{DS}| \leq e/C_{\Sigma}$, where V_{DS} is the SET drain-to-source voltage, e is the elementary electronic charge and C_{Σ} is the total capacitance associated with the SET island with respect to ground, and (ii) the interconnect capacitance associated with the gate, source and drain terminals are much larger than the device capacitance. In MIB, the drain current, I_{DS}, is modelled via two components: (i) the tunnelling current, I_{DSU}, which is independent of temperature, T, and (ii) the thermal current, I_{DSTH}, which is a function of temperature and thus:

$$I_{DS} = I_{DSU} + I_{DSTH} = \frac{I_D I_S}{I_D + I_S} + I_{DSTH} \quad (1)$$

where I_{DSU} is subsequently modelled based on the individual calculations of the drain, I_D, and source, I_S, tunnelling components (considered to be proportional to the tunnelling rates [11]). The proposed physical/analytical linear expressions of I_D and I_S, dictated by the island potential V_{island}, that controls the electron-tunnelling-probability, are detailed in Fig. 1. The overall calculation of the drain current is performed using: $I_{DS} = F(V_{GS1}, V_{GS2}, V_{DS})$, where V_{GS1} and V_{GS2} are the gate-to-source voltage of the two SET gates and F is a computing subroutine (reported in Fig.1). It is worth noting that all the model parameters of I_{DSU} are physical: (i) drain and source tunnelling capacitances, C_{TD} and C_{TS}, (ii) first and second gate capacitances, C_{G1} and C_{G2}, (iii) drain and source tunnel junction resistances, R_D and R_S.

A special attention is additionally paid to model I_{DSTH} in order to extend the validity of the model over a larger temperature range (Fig. 1) by proposing a new quasi-empirical expression for the off-state current, I_{OFF}:

$$I_{OFF} = \frac{V_T}{2(R_D + R_S)} \ln\left(1 + e^{1-\frac{\alpha}{nV_T}}\right) \quad (2)$$

which is a function of the temperature and the device-size. MIB has been checked to agree with MC simulation over two decades of temperature (0.1K to 10K) for a value of the fitting co-efficient n~10. The various plots reported in Fig. 2(a) for single and double-gate SET configurations at various V_{DS}, demonstrate the accuracy of the proposed model.

In order to extract the model physical parameters from real measured data, if a symmetrical device is assumed, the drain and source resistances can be extracted as: $R_D = R_S = V_{DS}/4I_{peak}$, where I_{peak} is the peak current as shown in Fig. 2(a). Additionally, if we denote by V_{peak} the minimum positive value of V_{GS1} [Fig. 2(a)] at which the peak appears, then for a single gate device it follows that

$$V_{peak} = \frac{e}{2C_{G1}} + \frac{C_{\Sigma}}{C_{G1}}\left(\frac{1}{2} - \frac{C_{TD}}{C_{\Sigma}}\right)V_{DS} \quad (3)$$

Eq. (3) suggests that the plot of V_{peak} versus V_{DS} is a straight line [as shown in Fig. 2(b)], the slope of which and whose intercept with the vertical axis can be used to extract C_{TD} and C_{G1} respectively. MIB and extraction procedure have been validated using a self-consistent approach: a set of realistic model parameters are used as inputs to the MC simulator (SIMON) and the SET is simulated, following which, the parameters can be estimated by applying the proposed extraction procedure to the simulated characteristics.

A very useful assessment of SET's application for both analog and digital hybrid SET-CMOS domain concerns the accurate evaluation of SET conductance in various operating regimes. MIB includes analytical *formulations* of transconductance ($g_m = dI_{DS}/dV_{GS1}$) and output conductance ($g_{ds} = dI_{DS}/dV_{DS}$) for *symmetric* SET. Similar to the drain current modelling approach, the conductances (g_m and g_{ds}) of SET are also decomposed into tunnelling component and thermal component (i.e., $g_m = g_{mu} + g_{mth}$; where $g_{mu} = dI_{DSU}/dV_{GS1}$ and $g_{mth} = dI_{DSTH}/dV_{GS1}$ and $g_{ds} = g_{dsu} + g_{dsth}$; where $g_{dsu} = dI_{DSU}/dV_{DS}$ and $g_{dsth} = dI_{DSTH}/dV_{DS}$) as appears in Fig. 1, where, according to the different bias conditions:

$$g_{dsu} = \frac{\left[\begin{array}{l} V_{DS}\{V_{island} + (C_{TD}/C_{\Sigma})(V_{DS} - 2V_{island} - 2\alpha\zeta) + \alpha\zeta\} \\ -(V_{DS} - V_{island} - \alpha\zeta)(V_{island} + \alpha\zeta) \end{array}\right]}{V_{DS}^2 R_D} \quad (4a)$$

or:

$$g_{dsu} = \frac{\left[\begin{array}{l} V_{DS}\{V_{island} + (C_{TD}/C_{\Sigma})(V_{DS} - 2V_{island} + 2\alpha\zeta) - \alpha\zeta\} \\ -(V_{DS} - V_{island} + \alpha\zeta)(V_{island} - \alpha\zeta) \end{array}\right]}{V_{DS}^2 R_D} \quad (4b)$$

Figures 3 and 4 demonstrate the ability of MIB to accurately describe the SET transconductance, g_m and output conductance, g_{ds}.

The validity of the MIB *drain current model* is not only limited for symmetric device but also equally applicable for asymmetric one. As shown in Fig. 5, MIB is able to predict the asymmetric SET characteristics quite accurately for both single and doubled gate device. We found that the minimum error in trans/output conductance model study is less than 3% and the maximum error is less than 10%, which mostly occurs in the transition between Coulomb blockade and non Coulomb blockade regions.

One should note that in Fig. 2(a), I_{DSU} (and not I_{DS}) is plotted along with the values obtained from the SIMON [1] for different values of V_{DS} at T = 100mK, which reveals that although I_{DSU} is independent of temperature,it is able to correctly predict the drain current for $T << e^2/(kC_{\Sigma})$. At higher temperatures, I_{DSTH} must be added to I_{DSU} in order to provide a more accurate model.

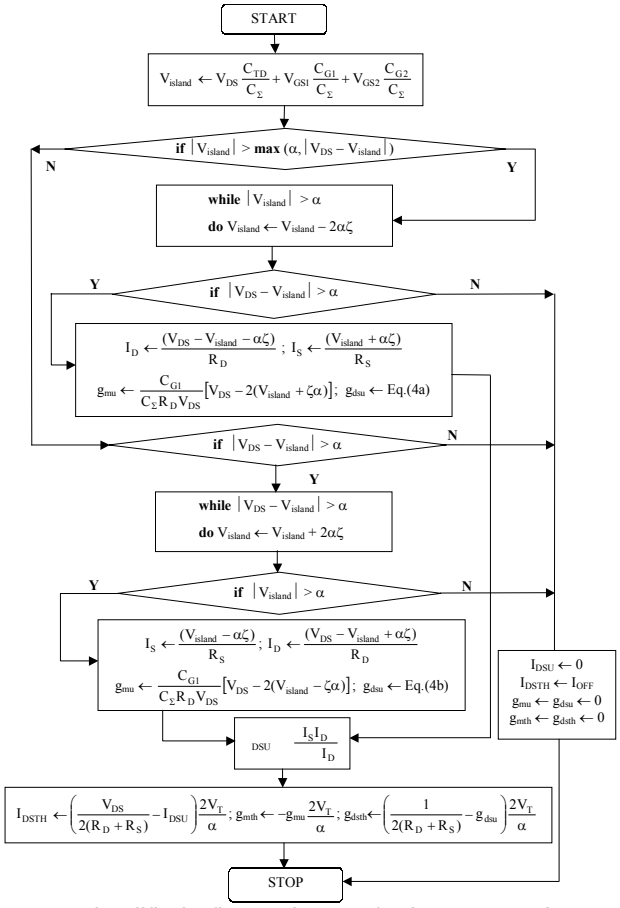


Fig.1. Simplified flow chart of the computing subroutine for SET currents, I_{DSU} and I_{DSTH}. Here ζ function holds the sign of V_{DS}, max(a,b) subroutine returns the maximum between a and b, V_T is the thermal voltage (= kT/e, k is the Boltzmann's constant), $\alpha = e/(2C_{\Sigma})$, and $C_{\Sigma} = C_{G1} + C_{G2} + C_{TS} + C_{TD}$.

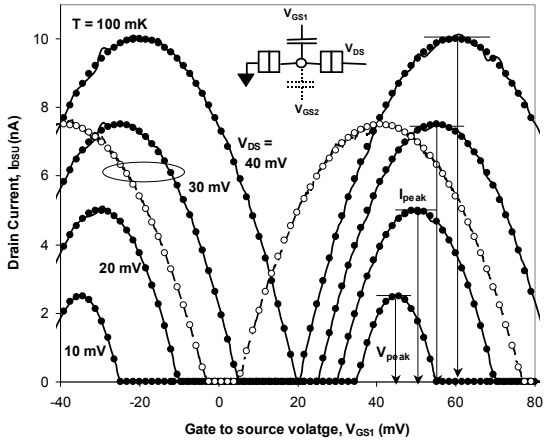


Fig. 2 (a) I_{DSU} model validation with: C_{G1} = 2aF, R_S = R_D = 1MΩ, C_{TS} = C_{TD} = 1aF and for V_{DS} = 10mV, 20mV, 30mV and 40mV at T = 100mK, where the symbol "●" represents MIB model and the solid line represents SIMON simulations for a single gate SET. In the same figure (for V_{DS} = 30mV), "○"represents MIB and the dotted line represents SIMON simulations for *a double gate SET* with C_{G2} = 0.8aF and V_{GS2} = 50mV.

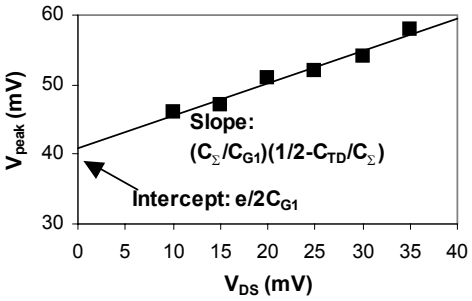


Fig.2(b) linear plot of V_{peak} versus V_{DS} for model parameter extraction using a self-consistent validation method. The extraction assumes that $C_{TD} = C_{TS}$, $I_{peak} \leq e/2C_\Sigma(R_D+R_S)$ and corresponds to single-gate SET.

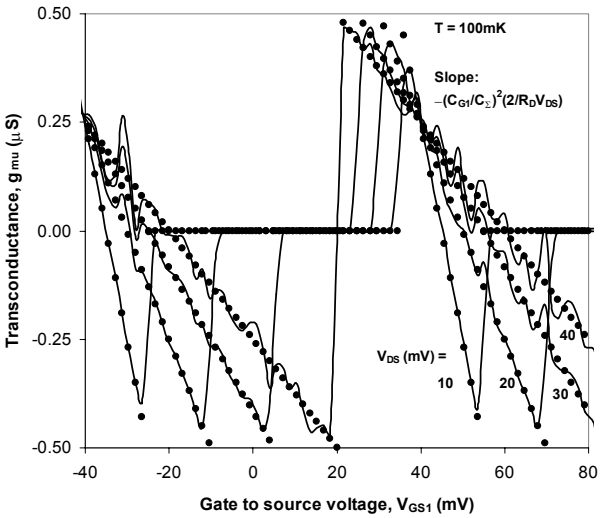


Fig. 3. Validation of MIB transconductance model for single gate symmetric device with same parameters as Fig. 2(a), where the symbol "●" represents MIB model, the thick line denotes the SIMON simulation.

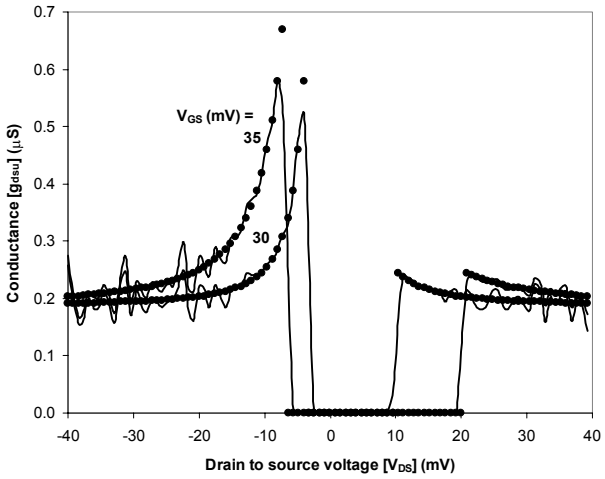


Fig.4. Validation of MIB output conductance model for single gate symmetric device at T = 100mK with same parameters and notations as Fig. 2(a).

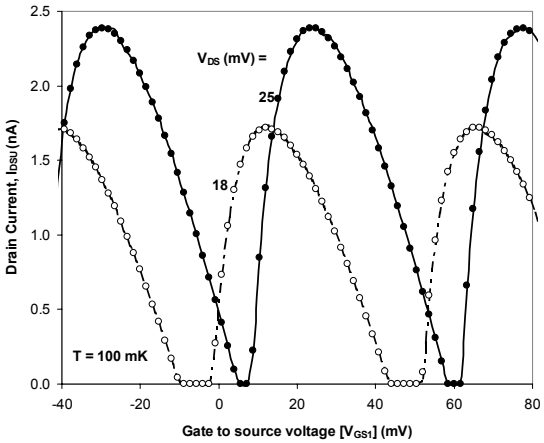


Fig.5. I_{DSU} model validation for asymmetric SET with: C_{G1} = 3aF, R_S = 1MΩ, R_D = 5MΩ, C_{TS} = 0.8aF, C_{TD} = 2.2aF where the symbol "●" represents MIB model, the thick line SIMON simulations for a single gate SET. In the same figure "O"represents MIB and dotted line represents SIMON simulations for a *double gate* SET with C_{G2} = 1.5aF and V_{GS2} = 30mV.

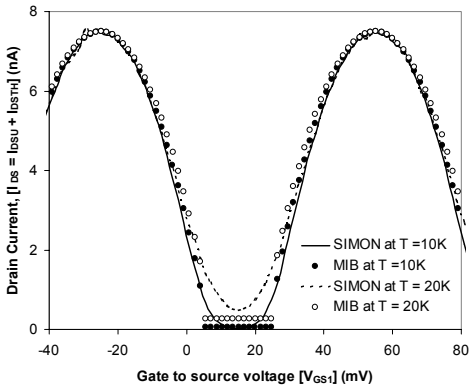
I_{DSU} is modelled with the assumption that, if the external bias can provide a potential higher than $e/(2C_\Sigma)$ across a junction then the electron tunnelling is possible, otherwise not. It does not consider any effect of thermal voltage. However, in reality, if the external bias cannot produce a voltage more than $e/(2C_\Sigma)$ across a junction, electron tunnelling still possible if there is enough thermal energy. The current due to this unwanted tunnelling can be consider as a leakage current in the off-state. I_{DSTH} is modelled empirically (which is a function of T) in order to track this leakage current. We have fully validated our model up to a temperature of $e^2/(40C_\Sigma k)$ [12], and observed that [Fig.6(a) and 6(b)]as the temperature increases, the on-state to off-state current ratio decreases and, hence the performance of the SET as a digital switch degrades.

3. Simulation

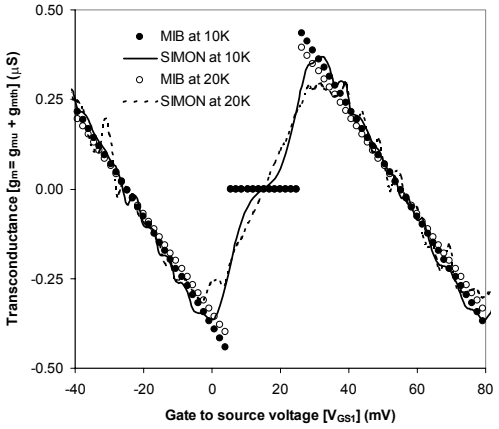
Static and transient responses of an inverter cell are successfully predicted [Fig. 7(a) and (b)] and good agreement with MC simulation and Uchida's analytical model demonstrates the accuracy of our physical analytical model in both static and dynamic regimes.

4. Conclusion

A new quasi analytical model for drain current and conductances of SET devices has been reported and validated using realistic parameters for both static and dynamic operations. The new MIB model has some clear advantages: (i) it is simple, physically based, and able to accurately describe both the drain current and the conductances (ii) it is able to incorporate the effect of the



(a)



(b)

Fig. 6(a) and (b) Validation of MIB drain current and transconductance model at high temperature for single gate SET with the same device parameter as Fig. 2(a).

second gate, (iii) it can also be applicable to asymmetric SET device (iii) it allows separate analytical descriptions of the SET tunnelling (I_{DSU}) and the thermal (I_{DSTH}) currents. Moreover, for T << $e^2/(kC_\Sigma)$, solely the tunnelling component, I_{DSU}, is able to accurately predict the overall SET drain current and therefore can save significant computation time for circuit simulation because of its simple, linear mathematical formulation. Finally, the model is shown to be very useful for the accurate simulation of few-electron logic circuits in both static and dynamic regimes and can also be efficiently used for the simulation of hybrid (SET-CMOS) circuit architectures.

5. References

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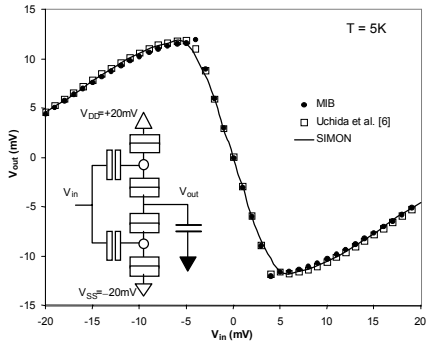
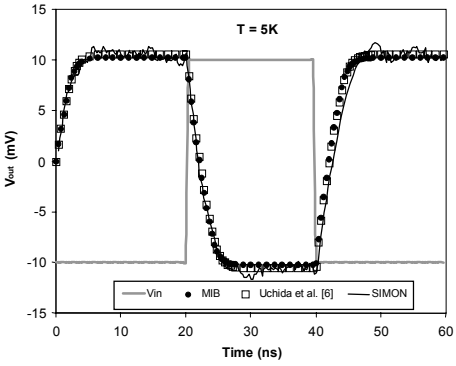


(a)



(b)

Fig.7(a) and (b). Static (a) and transient (b) characteristics of a SET inverter cell, as predicted by: MIB, SIMON and Uchida's model [6]. The SET parameters are: $R_S = R_D = 1M\Omega$, $C_{TD} = C_{TS} = 1$ aF, $C_{G1} = 3$ aF and the output load capacitor is $C_L = 1$fF.

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