low conduction loss converter can be achieved with low cost. To simplify the circuit analysis, it is assumed that all the components are ideal. Moreover, L is treated as a constant current source I_L and the output capacitor voltage is treated as a constant voltage source V_0. For convenient analysis, we will consider only the positive half-cycle of the input source (D_-, D_n, D_{r-}, and D_{a-} are off during this half-cycle). Based on these assumptions the circuit operation in one switching cycle can be divided into eight stages. Fig. 2 shows the theoretical waveforms for this commutation process.

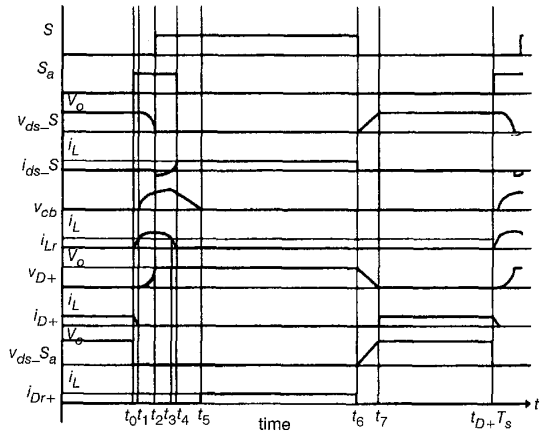

Fig. 2 *Theoretical waveforms of proposed boost converter*

Stage 1 (t_0, t_1): Prior to t_0, S and S_a are off, while D_+ and D_p are conducting. At t_0, S_a is turned on under ZCS and $i_{Lr}(t)$ rises linearly from zero to I_L.

Stage 2 (t_1, t_2): At t_1, D_+ is turned off with soft commutation and $i_{Lr}(t)$ increases continuously owing to the resonance between C_s, C_b, and L_r. During this stage, the charge in C_s is transferred to C_b. This stage finishes when $v_{Cs}(t) = 0$ at t_2.

Stage 3 (t_2, t_3): Because D_s is turned on at t_2, S is allowed to be turned on under ZVS. The resonance between L_r and C_b continues in this stage. This stage finishes when $i_{Lr}(t_3) = I_L$.

Stage 4 (t_3, t_4): In this stage, the current in S_a falls from I_L to zero while the current in S rises from zero to I_L. The equivalent circuit is practically the same as that for the preceding interval. This stage ends when $i_{Lr}(t)$ is equal to zero.

Stage 5 (t_4, t_5): During stage 5, S_a can be turned off in ZCS way and C_b is discharged in a linear way by I_L through D_{a+}. This stage finishes when the voltage on C_b becomes zero.

Stage 6 (t_5, t_6): This stage begins when D_{r+} is turned on under ZVS. The circuit operation is identical to the turn-on state of a conventional PWM boost converter and the current path is $I_L - D_p - v_s - D_{r+} - S - I_L$.

Stage 7 (t_6, t_7): This stage begins when S is turned off under ZVS at t_5. I_L charges C_s linearly, which limits the growth rate of the voltage across S. This stage finishes when $v_{Cs}(t)$ is charged to V_0.

Stage 8 (t_7, t_0): This stage begins when D_+ is turned on under ZVS. The operation of the circuit at this stage is identical to the normal turn-off operation of a PWM boost circuit. At $t = t_0 + T_s$, the auxiliary switch S_a is turned on again and this starts the next switching cycle.

Based on the circuit analysis presented above, both the main switch and the auxiliary switch in the proposed circuit are switched under soft-switching condition without increasing voltage stresses. The ZCS auxiliary resonant circuit is merely activated during the short ZVT switch transition, thus the proposed converter is identical to a common PWM converter most of the time. Moreover, this converter is easily built in conjunction with a PFC circuit.

Experimental results: A 250 W, 100 KHz, 120 V_{rms} AC input prototype of the proposed converter has been implemented and tested ($C_b = 22$ nF, $L_r = 6$ μH, $C_s = 2$ nF, $L = 740$ μH, $C = 680$ μF, and $V_0 = 250$ V). The key experimental results of the proposed converter are shown in Fig. 3. It can be seen that the experimental results are relatively clean and agree with the theoretical analysis. The main switch commutates at ZVS turning on and off, and the auxiliary switch commutates at ZCS turning on and off, respectively. The measured conversion-efficiency of the proposed ZVT-PWM AC-DC boost converter is 96% at the rated load. Fig. 3*b* shows the waveforms of the input line voltage and current for the proposed converter. The result demonstrates that the power factor is practically near unity for the rated load.

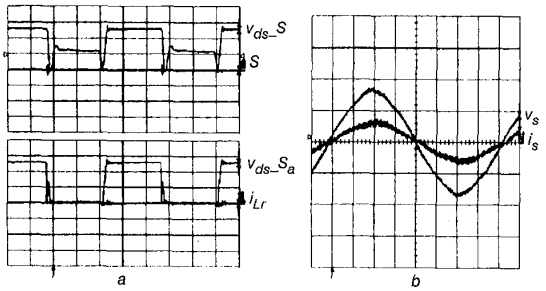

Fig. 3 *Measured waveforms of proposed boost converter*

a v_{ds_S}, $v_{ds\_S_a}$ (100 V/div), i_{Lr} (5 A/div) and S (10 V/div); timebase = 2 μs/div
b v_s (100 V/div) and i_s (5 A/div); timebase = 2 ms/div

Conclusion: A novel ZVT-PWM AC-DC boost converter with a simple ZCS auxiliary resonant circuit has been proposed to improve the efficiency of a unity PFC converter by reducing commutation and conduction losses. Through the proposed topology, the converter always has only two conducting semiconductors in the main current flow paths when the main switch is off. This contributes to the reduction of conduction losses. In addition, the unique locations of the resonant capacitor and inductor ensure low switching stress and commutation losses are obtained using this converter. The proposed converter is very suitable for low conduction loss, low-cost single-phase high PFC universal interface applications.

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SET-based quantiser circuit for digital communications

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A single electron transistor (SET)-based quantiser circuit has been developed for the purpose of digital communication. The proposed circuit, which consists of only two SET devices and one load capacitor, offers ultra-low power dissipation, small quantisation noise error and zero granular noise error. The proposed circuit does not require any external sampling signal for sampling the baseband signal, the sampling rate can be controlled by varying the device capacitor.

Introduction: Single electron transistors (SETs) have recently attracted special attention owing to their very low power consumption and ultra small size (of the order of a few nanometres) [1]. However,

even though some clear functionality has been reported at the device level and a few niche applications have been demonstrated [1, 2], there is still a strong need to identify and develop mainstream circuit applications for SETs. It is worth noting that the operation of the SET devices is based on the Coulomb blockade phenomenon [1, 2], which is quite unique compared to the principle of operation of MOS transistors. This work exploits this particular Coulomb blockade property of SET devices in order to develop a quantiser circuit for the purpose of digital communication.

Objectives: A simple digital communication transmitter system is shown in Fig. 1. In this system, the baseband signal (band limited to 3.3 kHz in the case of audio signal) is sampled and quantised (at Nyquist rate) using a sample-and-hold circuit and then fed to an A/D converter for encoding [3]. A simple sample-and-hold circuit often fails to follow a signal accurately as it produces a considerable amount of quantisation error. To suppress this quantisation error many methods have been proposed (e.g. delta modulation, adaptive delta modulation, compander) [3]. However, all such methods suffer from: (i) much hardware overhead and computation (e.g. the adaptive delta modulation requires a processor to compute the step height) and (ii) granular noise problems [3]. The quantisation circuit reported in this Letter consists of only two SET devices (resulting in a minimal circuit complexity) and one load capacitance (C_L), which is able to quantise any type of signal with a very low quantisation noise error and with zero granular noise error. The circuit validation has been carried out using: (i) the standard, largely accepted, SIMON simulator [2] for single electron devices and (ii) parameters of the SET devices that correspond to reported fabricated and measured devices [4–6]. It is also demonstrated that this circuit does not require any external sampling signal for the quantisation of the baseband signal, the sampling rate of the baseband signal can be controlled by varying the value of the capacitance of the SET devices.

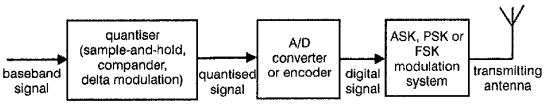

Fig. 1 *Block diagram of simple digital communication transmitter system*

Circuit description: Fig. 2 shows the schematic diagram of the proposed SET-based quantisation circuit. The performance of this circuit is verified with arbitrary input signals as shown in Fig. 3, with realistic values [4–6] of the tunnel and gate capacitance (C_T and C_G, respectively) of the SET device, $C_T = C_G = 2$ aF and a value of the tunnel resistance (R_T) of 100 KΩ at $T = 100$ mK. Fig. 3 plots the input waveform along with the quantised output of the circuit and it is demonstrated that the quantised output follows the input signal quite accurately. Two interesting observations can be made from this Figure. First, it is worth noting that the heights of the quantised steps are all equal to e/C_L (where e is the electronic charge). This is due to a step jump at the output occurring when a single-electron tunnels through the circuit and an elementary charge is trapped at the load capacitor. Therefore this behaviour cannot be mirrored by any CMOS equivalent circuit. It should be noted that the output of the circuit is in the order of μV (due to e/C_L ratio) for $C_L = 1$ pF. However, the output can be boosted up by decreasing the value of C_L, e.g. if the value of C_L is changed from 1 to 0.1 pF the output of the proposed circuit will be multiplied by 10. The only requirement for the circuit to work properly is $C_L \gg C_G$, C_T, which is easily achievable in practice. Secondly, the widths of these quantised steps vary, which is in contrast to conventional MOS-based quantisers. Note also that in Fig. 3 the input signal is divided into six regions corresponding to the different signal slopes. It is very important to note that the width of the quantised steps is constant for each region characterised by a constant slope and hence the quantised output of this circuit is frequency modulated. Another exclusive characteristic of this circuit is that it does not encourage any granular noise in region 5 (flat signal). Therefore, the proposed SET circuit can be uniquely used to quantise any type of baseband signal and the output of this circuit (i.e. the quantised signal) is frequency modulated. It follows that present sample-and-hold-compander-delta-modulation-systems could be replaced by this proposed very tiny (comparable with the size of a SET inverter [7]) SET circuit. The power dissipation of the proposed circuit is eventually dynamic, i.e. the proposed circuit draws current from the input voltage source only when the output changes from one step to another (i.e. when the electron tunnelling happens) as shown in Fig. 3. It follows that the circuit has an ultra-low power dissipation compared to any other conventional solutions. However one specific overhead of the proposed SET circuit is related to the specific encoding of the quantised output into digital format. In the proposed circuit, the information of the baseband signal is captured by the step width of the quantised signal and not by its step height.

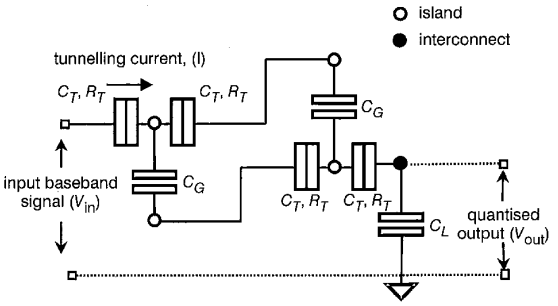

Fig. 2 *Circuit diagram of proposed SET-based quantiser*
C_G and C_T: gate and tunnel capacitance, respectively; R_T: tunnel resistance; C_L: load capacitance ($C_L \gg C_G$, C_L)

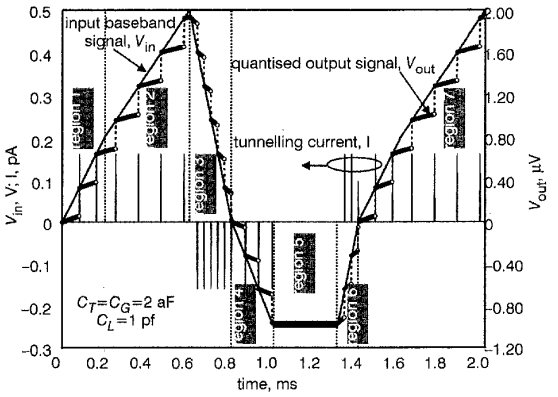

Fig. 3 *Evaluation of performance of proposed circuit with arbitrary input signal, using SIMON single electron simulator [2] at $T = 100$ mK*
Tunnelling current also plotted against time

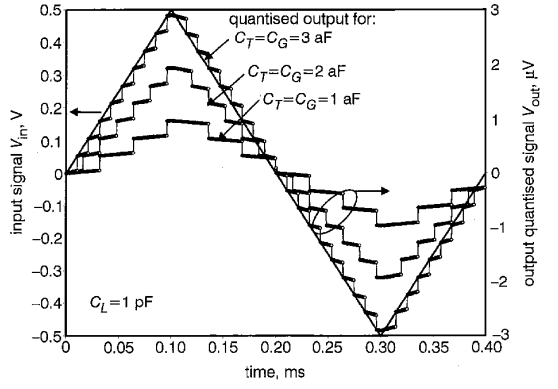

Fig. 4 *Effect of device capacitance on sampling rate for three values of device capacitance (1, 2 and 3 aF)*

Results and discussion: In our investigation, particular attention has been paid to the control of the sampling rate of the input signal by varying the value of the capacitance of the tunnel junction and the gate. Fig. 4 shows the effect of different values of tunnel and gate capacitance on the sampling rate for a 2.5 KHz (principle frequency) signal. The Figure shows that the sampling rate increases with

increasing value of the capacitance. This is due to the Coulomb blockade voltage being proportional to $(e/2C_\Sigma)$, where C_Σ is the total capacitance associated to the island. Hence, as the value of island capacitance increases, a smaller value of the voltage is needed for the electron to tunnel through the device and hence, for higher value of the capacitance, the sampling rate increases. In this connection it can be observed that as the device capacitance reduces, the ability of the proposed quantiser to handle higher amplitudes increases.

Although in this work the performance of this circuit is demonstrated only for audio frequency signal (i.e. signal frequency <3.3 KHz), it appears that the system exhibits similar performance even in very high frequency range (above MHz range), which is very useful for other communication applications. This is basically due to the principle of this circuit being solely based on the Coulomb blockade phenomenon, which is transparent to the frequency of the baseband signal. Only the value of the capacitance of the SET devices (i.e. the dimension of the island) has to be tuned for proper operation. Finally, it should be noted that the proposed circuit, using $C_T = C_G = 2$ aF, can accurately quantise the input signal up to a temperature of 2 K. The working temperature of the quantiser can be increased by properly scaling down the device capacitance (C_T and C_G) values.

Conclusion: A novel circuit based on SET devices for the quantisation of baseband signal has been proposed and validated. The functionality of the proposed circuit has been verified using the SIMON simulator and reported parameters for fabricated and measured SET devices. The circuit exhibits excellent performance in quantising various types of baseband signals in the audio frequency range. It has also been demonstrated that the sampling rate can be controlled without using any external sampling signal by simply varying the value of the device capacitance. Finally, it is worth noting that the proposed minimal quantiser-circuit architecture (using two SETs), demonstrates unique advantages in terms of: (i) quantising performance over any frequency range, (ii) ultra-low power dissipation and (iii) reduced area consumption. It therefore appears to be a strong candidate for future digital communication applications.

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Digital kernel perceptron

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It is shown that a kernel-based perceptron can be efficiently implemented in digital hardware using very few components. Despite its simplicity, the experimental results on standard data sets show remarkable performance in terms of generalisation error.

Introduction: A practical way to build nonlinear classifiers is to map, via special kernel functions, the input space to a higher, possibly infinite, feature space where one can manipulate simpler linear operators [1]. This is a well-known theory that exploits the reproducing kernel Hilbert space (RKHS) framework, and recently has been applied with success by the machine learning community. Support vector machines (SVMs), designed by Vapnik [2], represent one of the most successful examples of a learning machine based on a kernel method. Other algorithms, that follow the same underlying approach, have been successfully proposed. Here we discuss the use of the Rosenblatt's perceptron in the dual, kernel-based formulation: the kernel perceptron (KP). The choice of the KP is justified by recent studies that have revalued its role in classification tasks, showing the relation between its generalisation ability and the sparsity of the final solution [3].

We show how to let the KP algorithm work only with integer values and suggest an efficient digital architecture for its implementation. We call this variant the digital kernel perceptron (DKP). Tests on several data-sets show the peak performance of our proposal is good in terms of architecture complexity and generalisation performance, which make the KP an appealing approach for building VLSI-based learning systems.

Kernel perceptron: Here we face a classification problem, where a two-class training set, $(\underline{x}_1, y_1), \ldots, (\underline{x}_n, y_n)$, with $\underline{x}_i \in \Re^m$ and $y_i = \{+1, -1\}$ is considered. The simplest machine able to classify such a set, if linearly separable, is the perceptron:

$$f(\underline{x}) = \underline{w} \cdot \underline{x} + b \tag{1}$$

Rosenblatt's learning algorithm is well-known as shown here:

Set:

$$\underline{w} = 0, \quad b = 0, \quad k = 0$$

Repeat until no mistakes occur
For $i = 1$ to n do
Compute

$$MSB = \operatorname{sgn}\left[y_i \left(\sum_{j=1}^{m} w_j x_{ij} + b \right) \right]$$

If $MSB < 0$ then

$$\underline{w} = \underline{w} + \eta \underline{x}_i y_i$$
$$b = b + y_i$$
$$k = k + 1$$

end for

The final vector of the weights can be represented as a linear combination of the input patterns, as follows:

$$\underline{w} = \sum_{i=1}^{n} \alpha_i y_i \underline{x}_i \tag{2}$$

Such an observation permits one to change the domain of work from the vector w to its *dual* α. As a result, one can exploit the well-known theory of kernels by using the following final structure of function f, which allows an implicit nonlinear transformation in a new feature space via the unknown mapping $\Phi(\cdot)$:

$$f(\underline{x}) = \sum_{i=1}^{n} \alpha_i y_i \Phi(\underline{x}_i) \cdot \Phi(\underline{x}) + b = \sum_{i=1}^{n} \alpha_i y_i K(\underline{x}_i, \underline{x}) + b \tag{3}$$

This kind of function is well-known in the machine-learning community and used for classification and function approximation tasks [4, 5]. $K(,)$ is a kernel function that realises a dot product in the feature space. Some examples of typical kernels are: $K(\underline{x}_i, \underline{x}_j) = \underline{x}_i \cdot \underline{x}_j$ (linear), $K(\underline{x}_i, \underline{x}_j) = \exp(-\|\underline{x}_i - \underline{x}_j\|^2 / 2\sigma^2)$ (RBF) and $K(\underline{x}_i, \underline{x}_j) = (\underline{x}_i \cdot \underline{x}_j + 1)^p$ (polynomial). Here we focus on the RBF kernel and set $b = 0$, as in the higher feature space the absence of the bias does not affect, in practice, the performance of the machine (note that the feature space of Gaussian kernels is of infinite dimension [6]). The dual algorithm (KP) is very simple and summarised here, where $q_{ij} = y_i y_j K(\underline{x}_i, \underline{x}_j)$:

Set:

$$\underline{\alpha} = 0, \quad k = 0$$

Repeat until no mistakes occur