Compact Modeling and SPICE-Based Simulation for Electrothermal Analysis of Multilevel ULSI Interconnects

Ting-Yen Chiang, Kaustav Banerjee, and Krishna C. Saraswat

Center for Integrated Systems
Stanford University, Stanford, CA 94305
{tychiang, kaustav, saraswat}@stanford.edu

Abstract

This paper presents both compact analytical models and fast SPICE based 3-D electro-thermal simulation methodology to characterize thermal effects due to Joule heating in high performance Cu/low-k interconnects under steady-state and transient stress conditions. The results demonstrate excellent agreement with experimental data and those using Finite Element (FE) thermal simulations (ANSYS). The effect of vias, as additional heat sinking paths to alleviate the temp erature rise in the metal wires, is included in our analysis to provide more accurate and realistic thermal diagnosis. It shows that the effectiveness of vias in reducing the temperature rise in interconnects is highly dependent on the via separation and the dielectric materials used. The analytical model is then applied to estimate the temperature distribution in multi-level interconnects. In addition, we discuss the possibility that, under the impact of thermal effects, the performance improvement expected from the use of low-k dielectric materials may be degraded. Furthermore, thermal coupling between wires is evaluated and found to be significant. Finally, the impact of metal wire aspect ratio on interconnect thermal characteristics is discussed.

1. Introduction

The scaling of ULSI leads to continuous increase in current density that results in ever greater interconnect Joule heating. In addition, a variety of low-k materials have been introduced to reduce the RC delay, dynamic power consumption and crosstalk noise in advanced technology [1, 2]. Together with the poor thermal conductivity of such materials and more metal levels added, the increasing thermal impedance further exacerbates temperature rise in interconnects [3]. As a result, not only will thermal effects be a major reliability concern [4, 5], but also the linear increase of resistivity with temperature can degrade the expected speed performance. On the contrary, overly pessimistic estimation of the interconnect temperature will lead to overly conservative approach. Hence, performing a more realistic thermal analysis and modeling of interconnects is critical.

The fact that the interconnect temperature does not increase inversely proportional to the nominal thermal conductivity of dielectrics suggests that the vias, which have much higher thermal conductivity, serve as efficient heat dissipation paths. The predicted temperature will be significantly higher than the temperature in practical situation if via effect is not properly considered. Since the cross sectional area of vias is generally smaller than those of the wires, it may raise a concern that the resultant higher current density in the vias may generate significant heat, deteriorating their effectiveness in heat conduction. However, as shown in [6], the temperature rise in the via is not as high as that in the wire. The vias are simply too short to produce enough heat. Furthermore, all the vias are not conducting current at the same time but they always help dissipate heat. Consequently, it is legitimate to consider vias as efficient thermal sink paths.

In this work, using compact models and SPICE-based electrothermal simulations, impact of vias on the thermal characteristics of deep sub-micron interconnects is investigated thoroughly and the temperature distribution along multi-level interconnects is then evaluated. An analytical expression for the effective thermal conductivity of ILD (inter-layer dielectrics), $k_{ILD,eff}$, incorporating via effect is derived. Additionally, the thermal advantage gained by using dummy thermal vias in advanced Cu/low-k interconnects is quantified. All the dimensions of the interconnect structure in this paper were taken from the 100 nm technology node based on the ITRS [7].

2. Thermal Analysis Methodologies Overview

Both analytical models and SPICE based 3-D electrothermal simulation methodology for thermal analysis of interconnects are provided in this paper. Each of the analysis methods (analytical and SPICE) has its own unique advantage and can be complementary. The analytical expressions facilitate quick estimation of temperature profile along metal wires and average temperature rise for multilevel interconnects to provide thermal design guidelines. On the other hand, the SPICE methodology provides more accurate estimation of thermal coupling effects and convenient transient analysis. Furthermore, due to the wide familiarity of SPICE to the circuit design community, this approach, as compared to traditional FE simulation, can be adopted more easily and it requires much less effort to set up as well as less CPU time to run.

2.1 Analytical Model and Assumptions

Various papers are devoted to derive analytical expression for the temperature distribution in IC chips [8-10]. However, most of

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them only consider a single heat source without considering the effect of vias, which is not the realistic case for most interconnects. In addition, the complicated nature of these expressions makes it very difficult to easily apply them to multi-level metal layers. In this work, parallel-array metal wires are considered and a compact analytical thermal model incorporating via effect is developed

In either steady state or transient condition, the first principle of *energy conservation law* must be satisfied at any instance,

$$\dot{E}_{in}+\dot{E}_{gen}-\dot{E}_{out}=\frac{dE_{st}}{dt} \qquad (1)$$

where the thermal energy entering, leaving, and generated in the control volume are E_{in}, E_{out}, and E_{gen} respectively. The rate of change of energy stored within the control volume is designated as dE_{st}/dt. Since the substrate, to which a heat sink is usually attached, is assumed to be the sole heat dissipation path to the outside ambient, only heat conduction downwards is considered in this interconnect thermal modeling. Heat convection to the ambient air is ignored by the application of adiabatic boundary condition on the four side walls and top of the chip. This is a reasonable assumption because, in general, the chip is enclosed by thermally insulated package materials. Heat radiation is simply too small to be taken into account. Therefore, the net heat transfer processes can be quantified by the rate equation known as *Fourier's law*,

$$q'' = -k\nabla T \qquad (2)$$

where q'' [W/m^2] is the heat flux and k [W/m-K] is the thermal conductivity.

2.2 SPICE-Based Electrothermal Simulation Methodology

Based on the thermal-electrical analogy (Fig. 1) a 3-D distributed thermal circuit model has been developed using SPICE. Inclusion of the lateral thermal resistance in the model captures the heat spreading effect and thermal coupling from nearby interconnects. Therefore, there is no need to add any data-fitting modification in the circuit model as in [11]. Furthermore, by employing RC transmission lines in the circuit model, transient thermal effects in interconnects can also be analyzed.

Thermal		Electrical
Temperature T [K]	⇔	Voltage V [V]
Heat Q [J]	⇔	Charge Q [C]
Heat transfer rate q [W]	⇔	Current i [A]
Thermal resistance R_T [K/W]	⇔	Electrical resistance R [V/A]
Thermal capacitance C_T [J/K]	⇔	Electrical capacitance C [C/V]

Governing equations

Steady-State condition

Temperature Rise		Voltage Difference
$\Delta T = q R_T$	⇔	$\Delta V = iR$

Transient condition

Heat diffusion		RC transmission line
$\nabla^2 T = R_t C_T \frac{\partial T}{\partial t}$	⇔	$\nabla^2 V = RC\frac{\partial V}{\partial t}$

Figure 1. Thermal-Electrical analogous quantities.

2.3 Model Validation

Both the closed form analytical thermal model and the SPICE based simulation technique have been validated by comparing with either experimental data [12] or simulation results carried out by ANSYS (Fig. 2), a finite element simulation package. It shows excellent accuracy within 5% agreement.

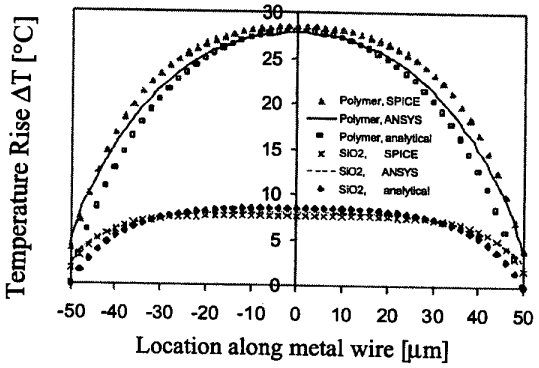

Figure 2. Temperature profile along the Cu wires with 100 μm via separation. $H = t_{ILD} = 0.8$ μm, $w = d = 0.3$ μm, quoted from ITRS [7] 100 nm node for global interconnects.

3. Steady-State Analysis

3.1 Temperature Distribution along Wires

Consider a rectangular metal wire with thickness H, width w, length L, resistivity $\rho(T)$ and thermal conductivity k_M, separated from the underlying layer by ILD of thickness t_{ILD} and thermal conductivity k_{ILD}. With x-coordinate set to zero at the middle of the wire, the two ends, x=±L/2, of the wire are connected to the underlying layer through vias. The temperature at the ends of the wire is assumed to be the same as the underlying layer temperature, T_0, thus $T(\pm L/2)=T_0$. It is further assumed that heat only flows downwards toward silicon substrate for the same reasons explained in Section 2.1. Therefore, under steady state conditions, with uniform root-mean-square current density, j_{rms}, flowing in the wire, from (1) and (2), the governing heat equation is given by,

$$k_M \frac{d^2T}{dx^2} - j_{rms}\,\mu\,\frac{dT}{dx} - \frac{hw_{eff}}{Hw}(T-T_0) + j_{rms}^2\,\rho(T) = 0 \qquad (3)$$

where μ is the Thomson coefficient and $\rho(T)=\rho_0(1+\beta(T-T_0))$, with β being the temperature coefficient of resistivity (TCR). The term $hw_{eff}(T-T_0)/Hw$ represents the heat loss downwards through the dielectrics and h is the heat transfer coefficient k_{ILD}/t_{ILD}. The w_{eff} is used to represent the deviations from one-dimensional heat flow. The Thomson effect is generally small and is neglected hereafter. The temperature distribution along the wire can then be solved as,

$$T(x) = T_0 + \frac{j_{rms}^2 \rho_0}{\frac{k_{ILD} w_{eff}}{H t_{ILD} w} - j_{rms}^2 \rho_0 \beta} [1 - \frac{\cosh(x/L_H)}{\cosh(L/2L_H)}] \quad (4)$$

where $$L_H = [(\frac{k_{ILD} w_{eff}}{H t_{ILD} w} - j_{rms}^2 \rho_0 \beta) \frac{1}{k_M}]^{-1/2} \quad (5)$$

It can be thought that within the range of thermal characteristic length, L_H, from vias, heat generated will flow through the vias to the underlying layer. Beyond L_H, heat will flow through the ILD and the via effect is diminished.

Effect of variation in ρ with temperature was found to be small for practical situations and is ignored here. With further simplification, the resistivity used in this work is assumed to be a constant at $\rho(T_{Die})$ to a first order approximation. Equations (3) and (5) can then be written as,

$$\frac{d^2T}{dx^2} - \frac{T - T_0}{L_H^2} = -\frac{\rho j_{rms}^2}{k_M} \quad (6)$$

and $$L_H \equiv \left[\frac{k_M H t_{ILD}}{k_{ILD}} \left(\frac{1}{s}\right)\right]^{1/2} \quad (7)$$

where heat spreading factor, $s = w_{effective}/w$ (8)

The heat spreading factor, s, is employed to correct the deviation from 1-D heat flow between a metal wire and the underlying layer. w_{eff} is the effective width of the dielectric through which heat conduction takes place. As a result, the spatial temperature distribution along the wire is given by,

$$T(x) = T_0 + \Delta T_{Max} \left(1 - \frac{\cosh(x/L_H)}{\cosh(L/2L_H)}\right), \quad -L/2 \le x \le L/2 \quad (9)$$

where $\Delta T_{Max} (= j_{rms}^2 \rho L_H^2 / k_M)$ is the temperature rise in the wire when via effect is ignored. In the above equation, T(0) is the temperature at the middle of the wire (x=0) which represents the maximum temperature in the metal wire.

The commonly used Bilotti's equation [10] is not adopted in this work to account for the deviations from 1-D heat flow. This is due to the fact that it assumes a single unpassivated heat (line) source, whereas, in typical IC layouts, there are multiple heat sources due to parallel metal wire array. A new expression of heat spreading factor, s, is therefore derived here. For the worst case scenario, all metal wires are assumed to carry the maximum RMS current density and to be separated by spacing d. As shown in Fig. 3, the Joule heat transfers downward as well as spreads laterally in the ILD. Hence, the total cross sectional area through which heat conduction takes place can be divided into two regions whose per unit length thermal resistances are R_{spr} and R_{rect}. Assuming the lateral spreading to increase linearly with vertical coordinate, the spreading thermal resistance, R_{spr}, can be derived as

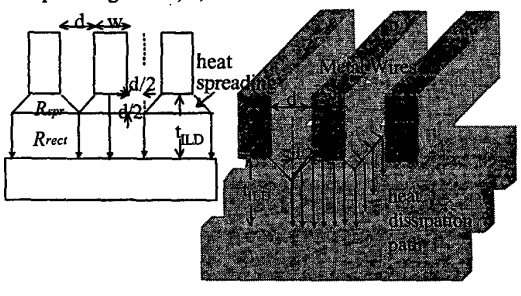

Figure 3. Geometry used for calculating R_{spr}, R_{rect} and the spreading factor s. Cross-sectional view is shown on the left hand side. Space between any two wires is shared for heat dissipation.

$$R_{spr} = \int_0^{d/2} \frac{1}{k_{ILD}} \frac{dy}{w + 2y} = \frac{1}{2k_{ILD}} \ln\left(\frac{w+d}{w}\right) \quad (10)$$

Then, the total thermal resistance of ILD, $R_{th,ILD}$, can be calculated by combining R_{spr} and R_{rect} as,

$$R_{th,ILD} = \frac{1}{2k_{ILD}} \ln\left(\frac{w+d}{d}\right) + \frac{1}{k_{ILD}} \frac{t_{ILD} - d/2}{w+d} \quad (11)$$

On the other hand, by definition, $R_{th,ILD}$ can also be expressed as

$$R_{th,ILD} = \frac{t_{ILD}}{k_{ILD} w_{effective}} = \frac{t_{ILD}}{k_{ILD} ws} \quad (12)$$

By comparing (11) and (12), s, can be obtained as

$$s = \left(\frac{w}{t_{ILD}} \frac{1}{2} \left(\frac{w+d}{w}\right) + \frac{w}{t_{ILD}} \frac{t_{ILD} - d/2}{w+d}\right)^{-1} \quad (13)$$

After the s factor is installed in (7), effect of the via separation and heat spreading on the temperature profile along a metal wire can be captured completely by (9). As can be observed from Fig. 2, the result using analytical expression shows excellent agreement with the 3-D finite element thermal simulation using ANSYS. It should be noted that, dependent on different layout and operating conditions, s could have different expression than (13). However, all the equations derived here can still be valid as long as the appropriate s is determined by either an appropriate analytical expression or extracted from simulation.

3.2 Impact of Via Separation on Effective k_{ILD}

As concluded from equation (9), significant difference in temperature profiles along the wires and in the maximum temperature rise can arise between the realistic situation of heat dissipation in the presence of vias and the overly simplified case that ignores via effect. In addition, it should be noted that as predicted from (7) and validated from Fig. 2, the thermal characteristic length, L_H, in the wire is longer if ILD has lower thermal conductivity, ($k_{polymer}$ = 0.3 W/mK v.s. k_{oxide} =1.2 W/mK). Consequently, via effect is more important for the low-insulators. By defining a via correction factor (η), the via effect can be incorporated into the effective thermal conductivity of ILD, $k_{ILD,eff}$, which can then be used in place of the nominal k_{ILD} in the conventional thermal equations. An analytical expression for $k_{ILD,eff}$ incorporating via effect is now derived here. The average temperature rise, ΔT_{ave}, in one metal layer can be expressed as,

$$\Delta T_{ave} = q\, R_{th} = j_{rms}^2 \rho \frac{H t_{ILD}}{k_{ILD,eff}\, s} \tag{14}$$

On the other hand, ΔT_{ave} can also be obtained from (9) as

$$\Delta T_{ave} = \frac{1}{L}\int_{-L/2}^{L/2} (T(x) - T_0)\, dx \tag{15}$$

$$= j_{rms}^2\, \rho \frac{H\, t_{ILD}}{k_{ILD}\, s}\left[1 - \frac{\tanh\left(\frac{L/2}{L_H}\right)}{\frac{L/2}{L_H}}\right] \tag{16}$$

Comparing equations (14) and (16), via correction factor, η, can be deduced as

$$\eta = 1 - \frac{\tanh\left(\frac{L/2}{L_H}\right)}{\frac{L/2}{L_H}}, \quad 0 \le \eta \le 1 \tag{17}$$

and

$$k_{ILD,eff} = k_{ILD} * \frac{1}{\eta} \tag{18}$$

The $k_{ILD,eff}$ is plotted against via separation in Fig. 4 for three different ILD materials. The geometries of the interconnect structure were taken from the ITRS [7] for the 100 nm technology node for global wires. It can be observed that incorporation of via effect results in increased $k_{ILD,eff}$ especially for ILD materials with lower nominal thermal conductivity. This fact can explain why the interconnect temperature is not as high as commonly assumed when low-k ILD is implemented in advanced interconnect structures.

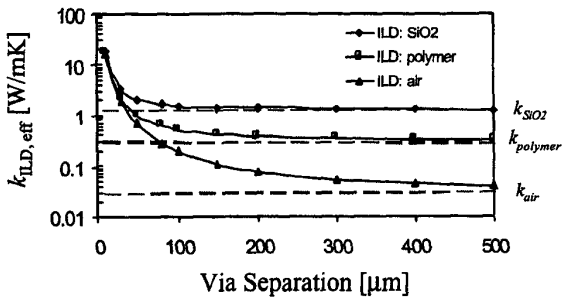

Figure 4. Effective ILD thermal conductivity increases with decreasing via separation. The lower the nominal k_{ILD}, the longer the L_H, and hence, the stronger is the via effect.

3.3 Temperature Rise in Multilevel Metal Layers

Generally, Joule heat generated in metal wires is considered to be dissipated only through the heat sink attached to the underlying Si substrate. Therefore, all the heat generated in the upper metal levels has to transfer through the lower metal levels before reaching the substrate. With $\Delta T_{i-1,\,i}$ defined as the average temperature rise between metal layers *i-1* and *i*, the temperature

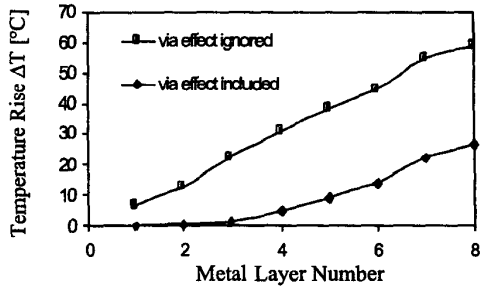

Figure 5. Distribution of temperature rise along metal layers from metal one to the top metal layer. For the case that includes the via effect, the via separations are 1, 5, 15, 30, 50, 100, 250 and 500 μm, for metal one through metal eight, respectively.

rise at the top layer for an N-level metal interconnect can be obtained as

$$\Delta T_N = T_N - T_{substrate} = \sum_{i=1}^{N} \Delta T_{i-1,i} = \sum_{i=1}^{N} q_i\, R_{th,i} \tag{19}$$

$$\cong \sum_{i=1}^{N} \frac{t_{ILD,i}}{k_{ILD,i}\, s_i} \eta_i \sum_{j=1}^{N} j_{rms,j}^2\, \rho_j\, H_j \tag{20}$$

This is a closed form analytical equation that can be used to compute the temperature rise of interconnects in a multilevel interconnect system. For the case when via effect is neglected, η_i is set to be 1. As can been seen from (20), more heat flows through lower levels since q_i represents the sum of all the heat generated from i^{th} layer to N^{th} layer. As a result, substantial temperature rise will occur in local wires if the effect of the via population, which is usually dense, is not taken into account. For the purpose of demonstration of the importance of via effect, some reasonable values of via separation were assigned to each of the 8 metal layers and a polymer was used as the ILD for the 100 nm technology node. In addition, a worst case current density, j_{rms}, of 1.4e6 A/cm^2 was assumed for all wires. It can be observed from Fig. 5 that the overall temperature rise is much lower if effect of the vias is included. Secondly, it can be observed that the temperature distribution among metal layers is quite different for these two cases. Ignoring via effect results in large temperature rise in the lower layers before leveling off. On the other hand, with via effect considered, the temperature rise in the lower levels is significantly lower even when the ILD material's nominal thermal conductivity is approximately one fourth of k_{oxide}. Most of the temperature rise is attributed to the upper metal layers with long via separation. Therefore, from the thermal design point of view, global interconnects could be more problematic [5] and the concern of increasing delay in the global wires may get worse with this additional temperature effect.

3.4 Thermal Effect on RC Performance

In this section the impact of thermal effects on RC delays are evaluated for various low-k dielectrics. Several dielectrics schemes are evaluated in Table 1, homogeneous SiO_2, polymer, air, and heterogeneous air gap, where air is used for intra-level and SiO_2 for inter-level dielectrics. The interconnect dimensions and assigned via separations were the same as in Fig. 5 except

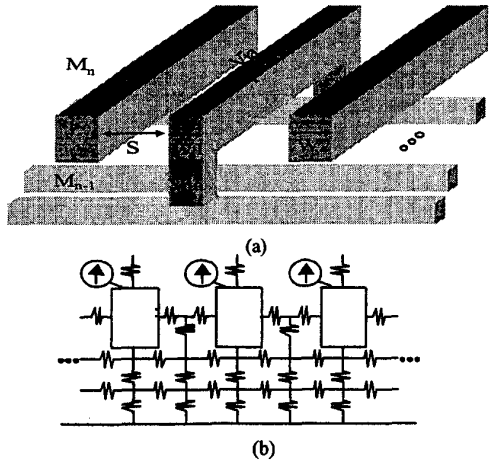

Figure 6. (a) Interconnect configuration. (b) Distributed thermal circuit.

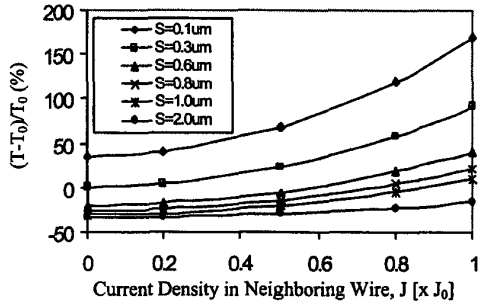

Figure 7. T is defined as the maximum temperature rise in the middle wire. Reference temperature T_o is the maximum temperature rise in the middle wire when there is no current flowing in the nearest neighboring wires and with equal line width and spacing (S). The current density in the middle wire is J_0. $1.4x10^6$ A/cm2. Line width is kept at 0.3μm throughout the simulation.

that, in the global levels (7^{th} and 8^{th} layers), four different via separations, 100 μm, 200 μm, 500 μm and 1000 μm were considered to analyze the via effect. Ignoring any fringe capacitance, the total interconnect capacitance per unit length can be simply expressed as: $C_{total}=2(C_{ILD}+C_{IMD})$, where $C_{ILD}=\varepsilon_{ILD}/2AR$ and $C_{IMD}=\varepsilon_{IMD}AR$, where AR denotes wire aspect ratio. Thickness of ILD is assumed to be the same as the height of the upper metal layer. The factor of 2 in the denominator for C_{ILD} accounts for the overlap with orthogonal wires on adjacent levels. The length of overlap is taken to be half the length of the interconnect based on the assumption that wire width is half the pitch. First, we notice that, due to the high wire AR, the intra-level (line-to-line) capacitance, C_{IMD}, is dominant. About 90% of C_{total} is contributed by C_{IMD} even if Miller effect is not considered. Temperature in the global interconnect level is estimated using (20). From Table I, it can be observed that the lower the nominal k_{ILD}, the stronger is the via effect due to longer L_H. Furthermore, as the distance between vias increases, the via effect diminishes. In the case of using homogeneous air as dielectrics, RC improvement can deviate from the expected value by as much as 60% when via separation is long. From the data, it can be seen that the heterogeneous air gap structure has the same low temperature rise as the homogeneous SiO_2, and has even better RC performance than homogeneous air dielectrics after considering thermal effects. This can be explained by observing that for the air-gap structure most of the heat is flowing downwards to the heat sink while the capacitance is reduced by the presence of air as an intra-level dielectric. Finally, it should be noted that as current density keeps increasing for future technology nodes, the RC performance expected from low-k dielectrics may deviate from its nominal value further if thermal effects are not managed properly.

3.5 Thermal Coupling Effects

To provide robust thermal analysis for deep sub-micron Cu/low-k interconnects, it is very desirable to have an efficient simulation methodology to estimate the temperature profiles in the metal wires and evaluate the thermal coupling between them. Based on the thermal-electrical analogy (Fig. 1), a 3-D distributed thermal circuit model has been developed. This thermal network can be easily implemented in the same manner as an electrical circuit network by simply employing the proper counterparts as illustrated in Fig. 6. It is important to include the lateral thermal resistance in the model to account for the heat spreading effect and, therefore, there is no data-fitting modification in the circuit model. The main advantage of this SPICE-based methodology is that once layout data is available, the thermal analysis can be done quickly. As validated in Fig. 2, the results using HSPICE show excellent agreement with those using ANSYS. It should be noted that the steeper temperature profile for the low-k dielectrics could exacerbate electromigration due to the larger temperature gradient. To account for the temperature dependence of the metal resistivity, the heat generation (q) in each piece of the wire has been modeled as a voltage (temperature) controlled current source ($q=J^2\rho(T)$).

To investigate the parallel thermal coupling effect between

Dielectric Schemes (ε_r / k [W/mK])	C_{IMD} (pF/cm)	C_{ILD} (pF/cm)	C_{total} (pF/cm)	ΔT (°C) (global wire via sep.) 100/200/500/1000 [μm]	R (kΩ/cm) (global wire via sep.) 100/200/500/1000 [μm]	RC (ns/cm²) (global wire via sep.) 100/200/500/1000 [μm]	Realistic RC Normalized to SiO_2 100/200/500/1000	Nominal RC Normalized to SiO_2
SiO_2 (4.0 / 1.2)	0.956	0.066	2.043	8.3 / 8.7 / 9.0 / 9.0	1.07/1.08/1.08/1.08	2.20/2.20/2.21/2.2	1/1/1/1	1
Polymer (2.5 / 0.3)	0.598	0.041	1.277	23 / 25 / 27 / 28	1.14/1.15/1.16/1.17	1.46/1.47/1.48/1.49	0.66/0.67/0.67/0.67	0.63
Air (1.0 / 0.03)	0.239	0.017	0.511	59 / 95 / 145 / 165	1.30/1.46/1.69/1.78	0.67/0.75/0.86/0.91	0.30/0.34/0.39/0.41	0.25
Air gap	0.239	0.017	0.609	8.3 / 8.7 / 9.0 / 9.0	1.07/1.08/1.08/1.08	0.65/0.66/0.66/0.66	0.30/0.30/0.30/0.30	0.30

Table 1. Realistic RC performance of the top level interconnect, under the impact of thermal effect, is evaluated for various dielectric schemes with different via separations. Thermal effect is not considered in the calculation of nominal RC performance.

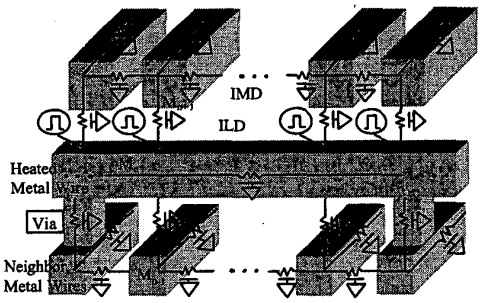

Figure 8. 3-D thermal circuit RC transmission line model for transient thermal analysis of interconnect structures.

wires, the configuration shown in Fig. 6(a) is examined and symmetrical boundary conditions applied. In Fig.7, the middle wire is carrying a current density of J_0(=1.4x10^6 A/cm2). It can be seen that both the current density of the neighboring wire and the line spacing greatly affect the temperature of the middle wire. In the case of equal line width and spacing (0.3μm), the temperature rise of the middle wire can be increased by nearly 100%. The negative values are due to the symmetric boundary condition chosen in this simulation. The coupling effect can be even more drastic when the wire is carrying a low current density, which represents a typical signal line. Consequently, The strong thermal coupling may cause resistance variations and further enhance crosstalk problem.

4. Transient Stress Analysis

4.1 Analytical Model

In general, a high-current short-pulse (J > 10MA/cm^2, and t_{pulse} < 200 ns) usually causes much higher ΔT_{max} due to more severe self-heating than under normal operating conditions and the heat diffusion is limited to the immediate materials in contact with the metal line. Again, only heat conduction is considered in this analysis. The governing heat diffusion equation of temperature rise during brief transients is

$$\frac{\partial}{\partial x}(k_M\frac{\partial T}{\partial x})+\frac{\partial}{\partial y}(k_{ILD}\frac{\partial T}{\partial y})+\frac{\partial}{\partial z}(k_{IMD}\frac{\partial T}{\partial z})+\frac{i_{rms}^2\rho(T)}{wH}=C_{eff}\frac{\partial T}{\partial t} \quad (21)$$

where $C_{eff}\cong[c_M wH+2c_{ILD}s_V w\sqrt{\alpha_{ILD}t}+2c_{IMD}s_I H\sqrt{\alpha_{IMD}t}]^{-1}$ (22)

and c_M, c_{ILD} and c_{IMD} are the heat capacity of metal, ILD and IMD materials respectively. S_v and S_l are shape factors in vertical and lateral directions. α_{ILD} and α_{IMD} are the thermal diffusion coefficients of ILD and IMD materials respectively. It should be noted that, unlike in the case of normal steady-state operating condition, the temperature dependence of $\rho(T)$ absolutely can not be ignored because of the large temperature rise. Together with the time- dependent C_{eff}, there is no easy analytical solution available for (21). Therefore, an efficient simulation methodology is desirable and will be discussed in details in Section 4.2. On the other hand, a rough estimation of temperature rise can be shown as [13],

$$\Delta T=\frac{E}{C_{eff}} \quad (23)$$

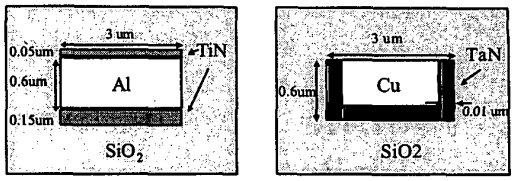

Figure 9. Schematic cross sections of Al and Cu interconnects with cladding layers used in model validation [12] and for simulations in Fig. 10.

$$\cong\frac{i_{rms}^2\rho(T)t}{wH}[c_M wH+2c_{ILD}s_V w\sqrt{\alpha_{ILD}t}+2c_{IMD}s_I H\sqrt{\alpha_{IMD}t}]^{-1} \quad (24)$$

4.2 SPICE-Based Simulation Methodology

RC transmission lines are used to model the heat diffusion (Fig.8) due to the similarity of the respective governing equations as illustrated in Fig. 1. This technique was validated by comparing with experimental data [12].

4.3 AlCu vs Cu Interconnects

As shown in Fig. 10, for the same cross section, current density, and surrounding dielectric, Cu wires would experience lower ΔT_{max} than Al wires, due to their higher thermal conductivity and thermal capacity, and most importantly, due to their lower resistivity. This along with higher melting point (~1100 ^{0}C) than that of AlCu (~660 ^{0}C) would provide more thermal margin to Cu interconnects. However, ΔT_{max} can still be high when metal dimensions are scaled down and low-k dielectrics are incorporated. Therefore, it is prudent to study the effect of vias on the thermal characteristics of Cu wires to make reliable use of them in deep submicron designs.

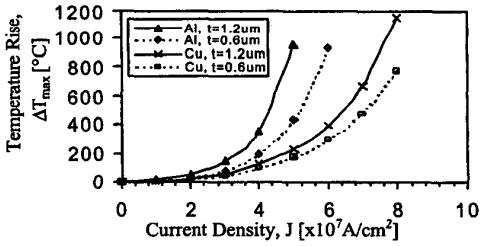

Figure 10. For the same wire cross section, shown in Fig. 9, Cu wire shows much lower temperature rise compared to Al wire under a 200 ns pulse stress. Symbols represent simulation data.

4.4 Impact of Via Separation and Low-k Dielectrics

Fig. 11 compares the normalized spatial temperature distribution along an interconnect line with a via separation of 100 μm, subjected to transient current pulses of 200 ns and 2 μs duration. It can be observed that the temperature rise profile for the 2 μs pulse is more gradual due to the increased influence of vias for longer diffusion time, which results in longer diffusion lengths. The heat diffusion length, $L_D \propto (\alpha t)^{1/2}$, where α is the thermal diffusivity of the interconnect materials, are 5 μm and 16 μm for the 200 ns and 2 μs pulse durations respectively. Thermal diffusion length L_D can be interpreted as the distance over which

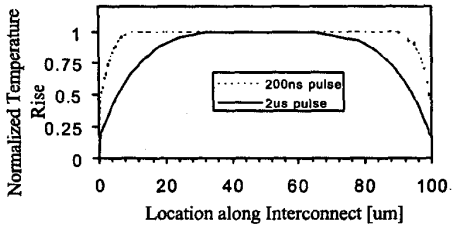

Figure 11. Simulated normalized temperature ($\Delta T/\Delta T_{max}$) profile along global Cu interconnect for two pulse durations with current density J=4x10^7 A/cm^2. Polymer is used as dielectrics in this case.

via effect is prominent. Fig. 12 plots the temperature decay after a 200 ns pulse. It can be observed that the temperature decays more rapidly with vias placed closer. This shortens the high temperature span that the interconnect would experience and thus reduces thermal problems. The maximum temperature rise, at the end of a 200 ns pulse, ΔT_{max}, is shown for global (Fig. 13) and local interconnects (Fig. 14) for different dielectrics as a function of the current density. It can be observed that while the temperature rises sharply and low-k dielectrics show worse situation for a typical global line with via separation of 100 μm, the temperature rise is significantly alleviated for local interconnects due to a smaller via separation of 1 μm. Even if air is used as both the ILD and the IMD dielectric (worst case thermal scenario), no significantly higher ΔT_{max} is observed for the local interconnects. This suggests that they are all within L_D and via effect dominates the thermal characteristics.

4.5 Impact of Dummy Thermal Vias

ΔT_{max} vs. via separation for different dielectrics is shown for high current pulse duration of 200 ns in Fig. 15. It indicates that ΔT_{max} would be reduced dramatically for smaller via separation. For larger via separation ΔT_{max} saturates since the effect of vias diminishes. Consequently, dummy thermal vias, which conduct heat but are electrically isolated, can be installed in Cu/low-k structure to lower the temperature rise. The advantage of the dummy via effect can be demonstrated by using the lowest-k dielectric, air, in ULSI interconnect structure despite its poor thermal properties. In the case of global interconnect, Fig. 15 shows that thermal vias would be required approximately every 20 μm in Cu/air and every 30 μm in Cu/polymer interconnect structures to match the temperature rise of Cu/SiO_2. For the purpose of comparison, under normal steady state operating

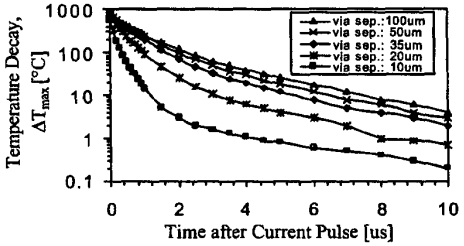

Figure 12. The temperature decay after a 200 ns current pulse, for Cu/low-k (polymer) global wires. The decay is facilitated by the presence of vias.

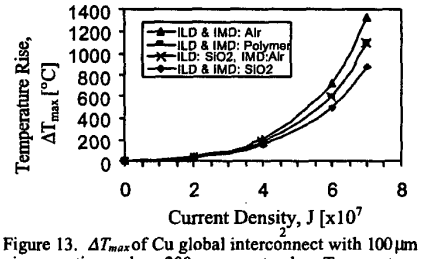

Figure 13. ΔT_{max} of Cu global interconnect with 100 μm via separation under a 200 ns current pulse. Temperature rises sharply with current density.

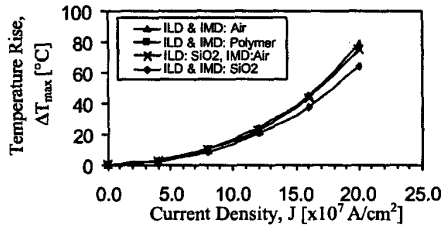

Figure 14. ΔT_{max} of Cu local interconnect with 1 μm via separation under a 200 ns current pulse. Temperature rises are much lower and nearly independent of the surrounding dielectric materials.

condition with the J_{max} specified in the ITRS, the thermal via separation can be much more relaxed based on a simple analytical evaluation. The temperature profiles for Cu/SiO_2 with via separation of 100 μm, and for Cu/air with via separation of 20 μm, experiencing the same ΔT_{max} under a 200 ns pulse are shown in Fig. 16. It can be observed that the temperature rise

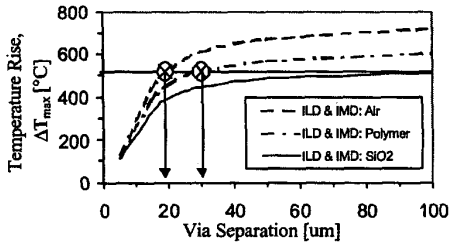

Figure 15. ΔT_{max} of Cu/air and Cu/polymer can match ΔT_{max} of Cu/oxide global interconnect if dummy thermal vias are added every 20 μm and 30 μm, respectively, with t_{pulse} = 200 ns and J=6x10^7 A/cm^2.

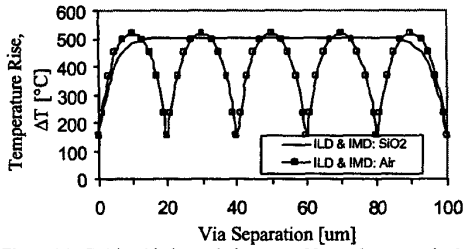

Figure 16. Cu/air with thermal vias every 20 um shows nearly the same ΔT_{max} as that of Cu/oxide global interconnect with 100 μm via separation under a 200 ns and J=6x10^7 A/cm^2 current pulse.

along the Cu/air wire varies spatially and that the average temperature is much lower than that of Cu/SiO_2 wire, resulting in reduced thermal problems and may relax the requirement for thermal via separation.

4.6 Impact of Interconnect Aspect Ratio

Finally, the effect of wire aspect ratio (AR) on the thermal characteristics is evaluated. For the same metal thickness, wires with smaller AR would suffer higher ΔT_{max} because of the smaller surface area-to-volume ratio (Fig. 17). For the same cross section area, indicating same current capability, a larger perimeter would result in lower ΔT_{max} by offering larger area for heat to diffuse out of metal wires, as shown in Fig.18. However, for embedded air gap (ILD: SiO_2 and IMD: Air), ΔT_{max} increases slightly with AR. This can be explained by the fact that with higher AR, embedded air gap interconnect structure would have increasing area contacted by air. Fig. 17 and Fig. 18 can be used to provide thermal design guidelines for interconnect.

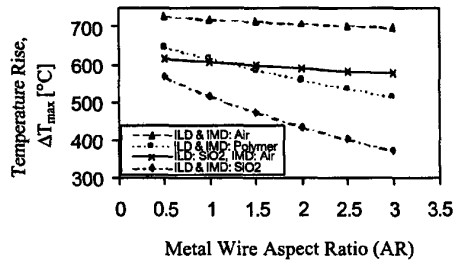

Figure 17. For the same metal thickness, global interconnects with lower AR, shows higher ΔT_{max} due to lower surface area-to-volume ratio. t_{pulse} = 200 ns and J=6x10^7 A/cm^2.

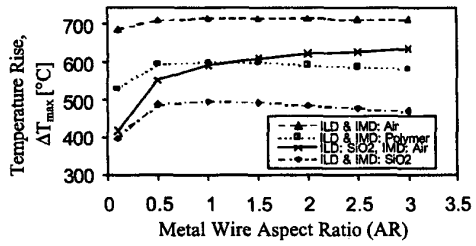

Figure 18. For the same metal wire cross section area, the impact of AR and dielectric structure strategy is shown. ΔT_{max} peaks at AR=1 due to the smallest perimeters. t_{pulse} = 200 ns and J=6x10^7 A/cm^2.

5. Conclusions

In this paper, both compact analytical models and a simple SPICE-based 3-D thermal circuit simulation methodology for steady-state and transient stress conditions are presented which allow quick evaluation of various Cu/low-k interconnect structures. The compact analytical models and the SPICE simulation results show excellent agreement with rigorous finite element simulations and can be employed for accurate reliability and performance analysis. It has been shown that, to accurately estimate the temperature rise and profile in the interconnect, the effect of via as efficient thermal paths must be considered. In fact, the effective thermal conductivity of ILDs can be significantly higher than the nominal value if via separation is comparable to the thermal characteristic length. Furthermore, it has been demonstrated that thermal coupling can be significant for wires in densely packed structure. Additionally, the impact of wire aspect ratio (AR) on the thermal characteristics has also been shown to be important for the thermal design of deep sub-micron interconnect structures. Finally, as technology keeps scaling, thermal effects should be carefully evaluated not only to address reliability concerns, but also for accurate interconnect performance analysis.

Acknowledgement

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