Carbon Nanotube Vias: A Reality Check

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Abstract

This paper presents a comprehensive electrothermal analysis of single-walled (SWCNT) and multi-walled carbon nanotube (MWCNT) vias – possibly the most imminent application of CNT-based components in VLSI chips. Accurate resistance and thermal conductivity models are provided for isolated SWCNTs and MWCNTs, as well as bundles of these, based on detailed electrical and thermal transport physics in sub-μm regime. It is found that although CNT via resistance may not be a significant concern for local interconnects, the resistance must be minimized in order to avoid significant degradation of global interconnect performance. Furthermore, detailed three dimensional electrothermal simulations show that Joule heating and the presence of thermal contact resistance between CNTs and metal, can be major bottlenecks in extracting maximum thermal performance from ballistic CNT bundle vias. From a processing perspective, we show that the applicability of MWCNT vias, which are currently being fabricated, is severely limited by their thermal and electrical resistance. For SWCNT vias, small diameter CNTs with dense packing and good thermal and electrical contacts between CNT and metal are needed.

I. Introduction

Carbon nanotubes (CNTs) have been proposed for VLSI interconnect applications due to their outstanding electrical and thermal properties. CNTs can carry three orders of magnitude larger current densities than Cu without showing signs of electromigration (EM) failure [1]. With increasing current densities, small dimension Cu vias are the structures that are most susceptible to failures. Hence several research groups have focused on developing CMOS compatible process for fabricating MWCNT vias [2]-[5].

Current efforts on the twin aspects of research in CNT based interconnects – fabrication on the one hand, and modeling/analysis-based evaluation (to guide design/process needs) on the other – are not synergistic. Till this date, while all fabrication efforts have been directed towards MWCNT vias (short, vertical interconnects where reliability is more critical than performance), almost all works analyzing the applicability of CNT interconnects in VLSI circuits [6], [7] have only addressed their electrical performance in terms of providing low-latency horizontal paths on a chip. A notable exception is the work in [8] which does point to the thermal and reliability advantages SWCNT vias can offer. However, the analysis in [8] is quite simplified as it does not consider any detailed modeling of the thermal properties of CNT vias and also ignores Joule heating in them. As will be shown through the detailed modeling and analysis in this work, even though the high values of thermal conductivity (*1750-5500 W/mK* [8]) predicted for CNT may be achievable, in the case of short vias (via height < 500 nm) this is overshadowed by the presence of thermal contact resistance as well as Joule heating at the metal-CNT contacts. To the best of our knowledge, the work presented here is the first to comprehensively evaluate CNT bundle vias (**Fig. 1**) that are already being fabricated [3], [9], and quantify their impact on performance and thermal management of the back-end.

II. Electrical Transport in CNT Vias

The resistance of a one-dimensional ballistic conductor (length less than the mean free path (*mfp*) of electrons, $L<\lambda$) considering spin degeneracy is given by $(h/2e^2)/M$, where $R_Q = h/2e^2 \approx 12.9\ k\Omega$ is the fundamental quantum resistance and M is the number of conducting channels. The effective mean free path of electrons (λ) in a CNT is the combined effect of various acoustic and optical phonon scattering lengths as shown in **Fig. 2**. This makes λ dependent on nanotube diameter, temperature, length, and bias voltage. Electrothermal analysis of CNT vias must consider the dependence of resistance on length as well as temperature because normal chip operating temperatures are well above room temperature, about 90 ºC. **Fig. 3** plots the electron mean free path of an isolated SWCNT as a function of length for different diameters and temperatures. The range of via heights in imminent technology generations is also shown (shaded regions). Although there is a significant variation in electron mean free path as these parameters vary, in the range of parameters depicted here (as applicable to CNT vias) λ is always larger than the tallest CNT vias expected as per ITRS [10]. As shown in **Fig. 2**, the acoustic and optical phonon mean free paths are directly proportional to nanotube diameter. Since MWCNTs have larger diameters than SWCNTs the effective λ in MWCNTs will be larger than those shown for SWCNTs in **Fig. 3**. Hence, for the rest of this work we assume that ballistic electrical conduction ($L<\lambda$) holds true for all CNT vias. In an SWCNT, the number of conducting channels is always 2. Hence the resistance of an isolated SWCNT is $(h/4e^2)$. In the case of MWCNTs, the number of conducting channels is dependent on its diameter as well as temperature [11], as shown in **Fig. 4**.

Fig. 5 shows the resistance of a densely packed SWCNT bundle via. It is observed that a via with 1 nm diameter SWCNTs will have resistance higher than that of Cu via of identical dimensions, even when perfect contacts are assumed between the metal and nanotubes ($R_{mc} = 0$). However, for densely packed vias with small diameter CNTs (for example *0.4 nm*) the resistance becomes competitive with that of Cu vias. In the case of MWCNT bundles, **Fig. 6** shows that for typical chip operating temperatures, the via resistance is much higher than that of an SWCNT bundle via. Finally, **Fig. 7 (a)** shows that even when via resistance is large (as is generally the case with CNT vias) the impact of this large resistance on overall interconnect delay is small for local interconnects. However, for global interconnects, a large number of vias constitute the path from the active device level (driver or load) to the topmost metal layer. Considering a typical global interconnect with repeaters inserted for optimal delay, **Fig. 7(b)** shows a large increase in global interconnect delay with increase in CNT via resistance, due to the cumulative effect of multiple vias in its path. Hence, if CNT vias are used everywhere, their resistance must be carefully engineered for optimizing the performance of global wires.

However, taking note of the fact that recent CNT via fabrication efforts have already brought electrical resistance of CNT vias down to within an order of magnitude of Cu vias [9], it is possible to achieve delay penalty of ~ 10% for global interconnect (see **Fig. 7(b)**). On the other hand, the thermal performance of vias has much greater implications on interconnect reliability [12]. Since CNT vias have larger resistance (and thus, larger Joule heating) than Cu, it becomes equally important to carefully analyze the heat generation and conduction mechanisms in CNT vias.

III. Thermal Transport in CNT Vias

Several works in the published literature express the inability to accurately predict the phonon mean free path in CNTs [13], [14]. On

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the other hand, experimental analyses have demonstrated evidence of ballistic thermal transport in CNTs. SWCNTs with *1 nm - 3 nm* diameter have shown ballistic thermal conductance even for lengths larger than *2 μm* at room temperature [13]. MWCNTs of diameter *14 nm* have also shown large phonon mean free paths (~ *500 nm*) at 320 K [15]. Hence, on the basis of these experimental observations, we can safely assume that the CNTs used in vias of height < *300 nm* will have ballistic thermal transport. In this case, the ballistic thermal conductance of a CNT (G_{CNT}) can be calculated using the model shown in **Fig. 8** [14]. Using this model, **Fig. 9** shows the dependence of equivalent thermal conductivity (K_{CNT}) of isolated CNTs on diameter, length and temperature. The large values of K_{CNT} exceeding *1000 W/mK* are shown to be achievable for isolated CNTs for lengths exceeding ~ *100 nm* and very small diameters. For ballistic CNT vias concerned in this work, similar to electrical ballistic transport, thermal resistance only occurs at the upper and lower contact due to ballistic thermal transport. Along the CNT length, there is no phonon scattering and reflection. Considering densely packed CNT bundle, **Fig. 10** shows total thermal conductance ($G_{Via} = n_{CNT} \times G_{CNT}$) of CNT vias for different diameters. It can be observed that G_{Via} of SWCNT via decreases with increasing diameter. While G_{Via} difference between MWCNT vias with different diameters remains small even if the diameter is doubled. This is because larger diameter MWCNTs contain more shells, whereas the shell number remains constant for SWCNTs. Knowing G_{Via}, the perfect thermal contact resistance (θ_0) can be calculated by $1/(2G_{Via})$. If the contact is imperfect, there is an additional thermal contact resistance θ_{mc} between CNT and metal. From the experimental data [13], θ_{mc} may range from 0 to $2\times\theta_0$. For thermal transport in the directions perpendicular to via length (*x-y* directions shown in **Fig. 12**), it is known that it is the interfacial resistance between CNT and ILD that dominates the thermal transport [16], [17]. Here, we assume the thermal resistance per unit nanotube length (in *x-y* directions) is about *2 Km/W* [16].

IV. Electrothermal Simulations of CNT Vias

Fig. 11 shows a schematic of the heat generation mechanisms in the CNT via structure. The heat generation in the CNT via only occurs at the via-ends where it contacts the metal layers while the thermal conductivity of the via varies depending on various factors shown earlier. Rigorous 3-D electrothermal FEM simulations are carried out to examine the thermal profile of CNT vias and adjacent interconnects. **Fig. 12** shows the geometry and boundary conditions for the electrothermal FEM simulations. Thermal contact resistance between CNT vias and adjacent Cu wires is taken into account along with temperature and size-dependent Cu resistivity. Temperature contour plots in **Fig. 13** show that very small diameter and densely packed SWCNT based vias have comparable thermal performance as that of Cu vias. As expected, MWCNT vias exhibit much higher temperature rise than SWCNT vias due to higher via resistance as well as lower thermal conductance. It is worth noting that there is a bottleneck at the CNT-via contact ends: thermal energy is blocked at the contact, whereas this is not the case with Cu vias. It can be expected that metal-CNT contact plays a critical role in CNT via thermal transportation. In **Fig. 13**, contact conditions (both thermal and electrical aspects) are assumed to be perfect, which is the ideal case. However, in reality, there are imperfect thermal and electrical resistances at the metal-CNT contacts. **Fig. 14** shows the impact of thermal resistance (θ_{mc}) as well as electrical resistance (R_{mc}) on the thermal performance. It can be observed that both thermal and electrical contact resistances have significant impact on thermal performance, especially for larger diameter SWCNT or MWCNT vias. Another imperfection factor is that the CNT bundle may not be densely packed. In fact, decreasing density of CNT bundle implies smaller number of CNTs per unit area, which directly increases thermal resistance as well as electrical resistance of CNT via. As expected, **Fig. 15** shows that the density of CNT bundles impacts the thermal performance significantly.

For ballistic transportation, both thermal and electrical resistances remain constant as long as the CNT is shorter than the mean free path. This advantage of CNT property can be utilized if it is applied to tall vias. **Fig. 16** compares the maximum interconnect temperature rise with CNT vias to that with Cu vias for increasing via height. An important point to note is that, as the via height is increased, the maximum temperature increases monotonically in case of Cu vias but remains relatively unchanged for CNT vias. It can be observed that small diameter SWCNT vias can achieve better thermal performance than Cu vias, even after considering the imperfect θ_{mc} and R_{mc} (for via height > 200 *nm*). However, Cu via exhibits much better performance than MWCNT vias even at 300 *nm* height. Hence, the small diameter SWCNT vias with good electrical and thermal contact could be employed as tall vias.

V. Conclusion

This work shows for the first time that thermal and self-heating effects constitute a greater concern for CNT vias than their electrical performance. Taking note of the fact that fabrication efforts have already brought electrical resistance of CNT vias down to within an order of magnitude of Cu vias [9], this work points to the immediate need for careful thermal characterization of CNT vias which has not been done so far. This work also provides insight into the intrinsic properties of CNTs and those of CNT-metal interfaces that must be carefully engineered to derive maximum benefit from CNT vias. It is shown that MWCNT vias, which are currently being fabricated, cannot match the electrical and thermal performance of Cu or SWCNT vias for nanometer geometries. Dense SWCNT bundles with small diameter and good contact (both thermal and electrical) between CNT and metal are needed for via applications.

Acknowledgment

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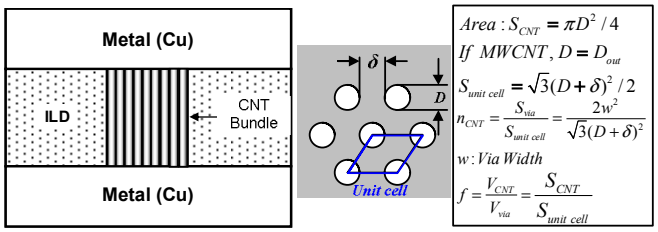


Fig. 1. Schematic and cross-sectional view of CNT vias integrated into Cu/ILD interconnect structure. The number of individual CNTs in a via (n) and volume fraction of CNTs (f) are calculated from the hexagonal unit cell, where D is the SWCNT diameter (MWCNTs have outermost shell diameter D_{out} and innermost shell diameter D_{in}), δ is the interval of CNTs. For densely packed CNT-bundle vias, δ is equal to the Van der Waal's gap ($0.34\ nm$).

$$\lambda_{eff} = \left(1/\lambda_{ac} + 1/\lambda_{op,abs} + 1/\lambda_{op,ems}^{fld} + 1/\lambda_{op,ems}^{abs}\right)^{-1},\ \lambda_{ac} = 400.46\times10^3\frac{D}{T}$$

$$\lambda_{op,abs} = \lambda_{op}\frac{N_{op}(300)+1}{N_{op}(T)} \approx \lambda_{op}\frac{1}{N_{op}(T)},\ \lambda_{op} = 56.4D,\ N_{op} = \left(\exp\left(\frac{\hbar\omega_{op}}{K_BT}\right)-1\right)^{-1}$$

$$\lambda_{op,ems}^{fld} = \frac{(\hbar\omega_{op}-K_BT)}{qV/L} + \frac{N_{op}(300)+1}{N_{op}(T)+1}\lambda_{op} \approx \frac{(\hbar\omega_{op}-K_BT)}{qV/L} + \lambda_{op}$$

$$\lambda_{op,ems}^{abs} = \lambda_{op,abs} + \frac{N_{op}(300)+1}{N_{op}(T)+1}\lambda_{op} \approx \lambda_{op,abs} + \lambda_{op},\ N_{op}(300) \sim 9.47\text{e-}4$$

Fig. 2. Determination of total effective electron mean free path (λ_{eff}) for a CNT, which depends on temperature, diameter, voltage bias as well as length [17], [18]. λ_{ac} and $\lambda_{op,\ abs}$ are *mfp* of scattering by acoustic phonon and optical phonon (OP) absorption, respectively. $\lambda_{op,ems}^{fld}$ and $\lambda_{op,ems}^{abs}$ are the *mfp* of scattering by OP emission, which would occur if electrons gain sufficient energy either from electrical field ($\lambda_{op,ems}^{fld}$) or after an OP absorption ($\lambda_{op,ems}^{abs}$). N_{op} is the OP occupation. The OP emission threshold energy $\hbar\omega \sim 0.18\ eV$.

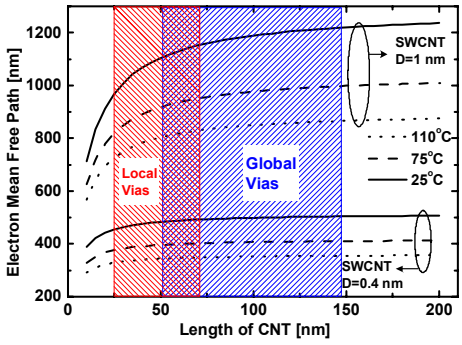


Fig. 3. Electron mean free path of an individual SWCNT at low-bias ($1\ mV$) as a function of CNT length. Shaded regions show the range of CNT lengths corresponding to local and global via heights, respectively. For MWCNT, each shell has larger diameter and would have even larger *mfp*.

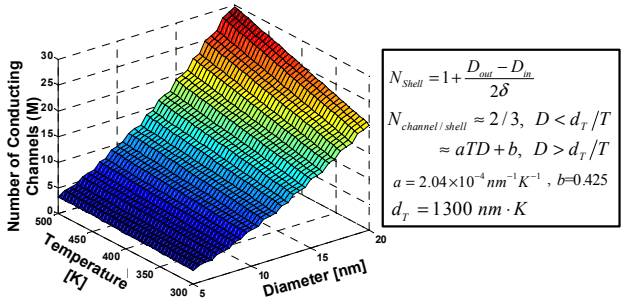


Fig. 4. Number of conducting channels (M) in an MWCNT as a function of diameter and temperature. The equations alongside show the model [11] used to calculate number of conducting channels per shell ($N_{channel/shell}$) and number of shells per MWCNT (N_{shell}).

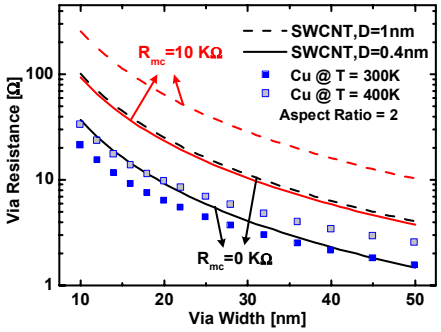


Fig. 5. Via resistance as a function of via width (square cross-section) using SWCNT bundles for different CNT diameters and metal-nanotube contact resistances. Square symbols show equivalent Cu via resistance (including size effects) at $300\ K$ (solid) and $400\ K$ (hollow). Note that CNT resistance is independent of via height due to ballistic transportation.

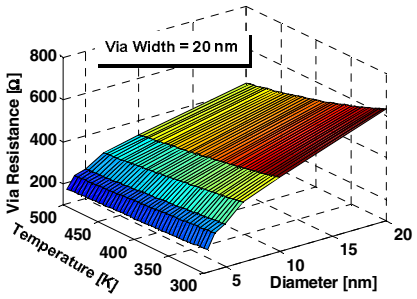


Fig. 6. MWCNT via resistance as a function of temperature and diameter (square via of width $20\ nm$). Resistance is independent of via height since these CNTs are of ballistic length.

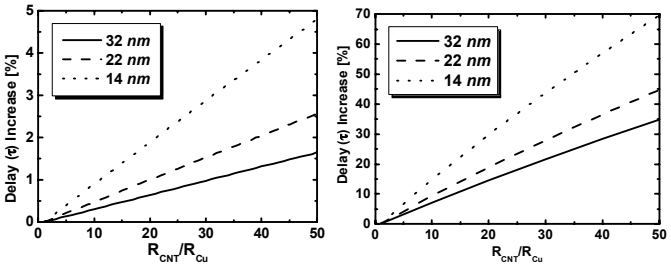


Fig. 7. % increase in interconnect delay (τ) with increase in via resistance (expressed as a multiple of Cu via resistance) for **(a)** local interconnects (Metal 1): minimum sized drivers with fanout of 4, and **(b)** global interconnect (6 times minimum global-wire width and spacing) with repeaters inserted for optimal delay. Interconnect and gate parameters follow ITRS [10] predictions at each technology node.

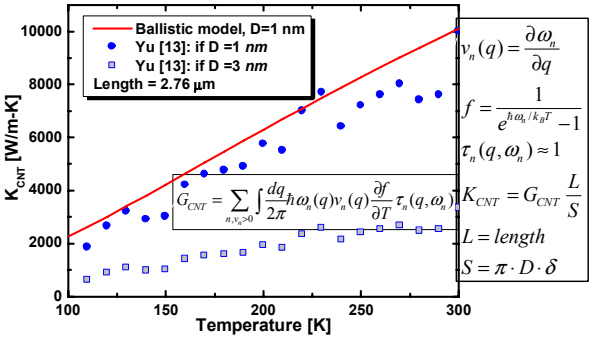
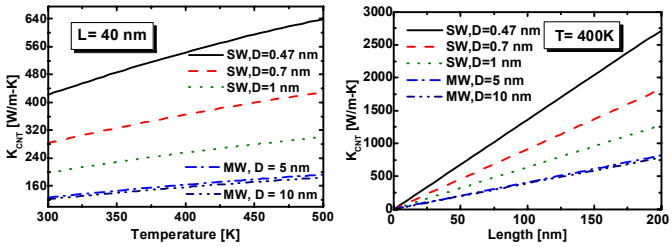


Fig. 8. Ballistic thermal conductivity (K_{CNT}) for an isolated CNT [14]. Here $\omega_n(q)$ is the phonon dispersion which is calculated following the methodology in [19]. Calculated K_{CNT} of ballistic SWCNT shows good agreement with measured data from [13].



(a) (b)

Fig. 9. Equivalent thermal conductivity (K_{CNT}) for isolated metallic CNTs of different diameters as a function of **(a)** temperature and **(b)** length (L). For calculating K_{CNT}, the area S is calculated as per equations shown in **Fig. 1**.

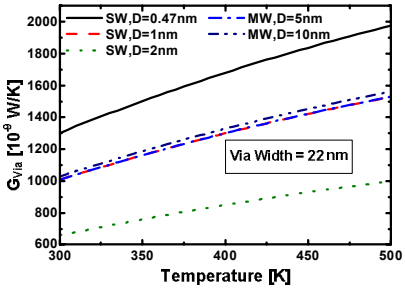


Fig. 10. Thermal conductance (G_{Via}) for densely packed metallic CNT bundles (square via of width = *22 nm*) for different values of D (individual CNT diameter), as a function of temperature. The G_{Via} value for D =*1 nm* SWCNT almost equals that for D = *5 nm* MWCNT. Note that G_{Via} is independent of via height due to ballistic transportation.

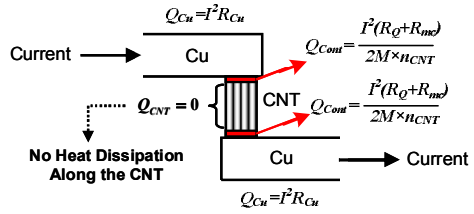


Fig. 11. Heat generation mechanisms for a CNT bundle via connected to two metal (Cu) leads, where individual CNTs are ballistic conductors. Here, I is the current through R_{mc} are the quantum contact resistance between metal and CNTs and M is the number of conducting channels in each CNT. Q represents heat generation in various segments.

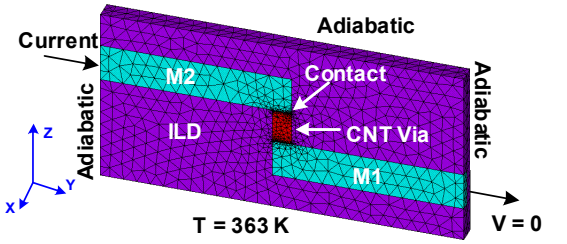


Fig. 12. Front view of interconnect structure used for 3-D finite-element electrothermal simulations, along with electrical and thermal boundary conditions. All parameters are based on ITRS [10] predictions for *22 nm* node. Metal lengths are *220 nm* for M1 and M2, via width and height are *22 nm* and *40 nm*, respectively. K_{ILD} = *0.12 W/m-K* [20] and current is *0.142 mA* [20]. Thin plates with thickness *1 nm* are inserted between the metal and CNT via to represent contacts (densely meshed regions). This simulation structure is used in **Figs. 13-15**.

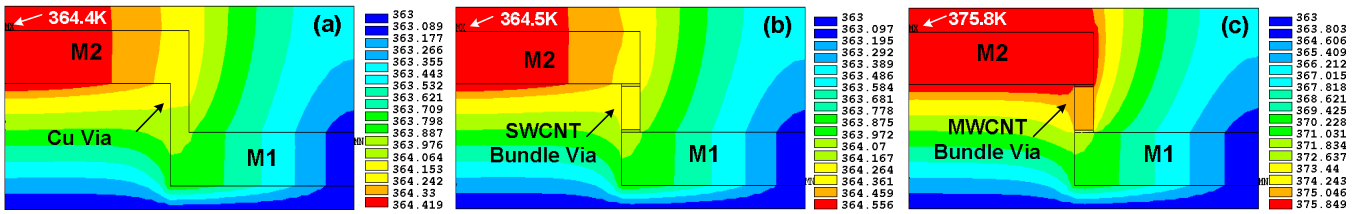
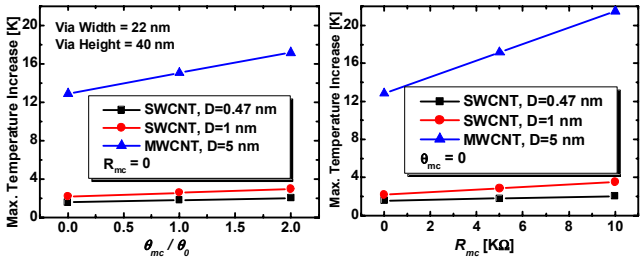


Fig. 13. Temperature contour plots from 3-D electrothermal FEM simulations for **(a)** Cu **(b)** densely packed SWCNT bundle and **(c)** densely packed MWCNT bundle vias. For SWCNT bundle, D = *0.47 nm* (diameter of (6,0) metallic SWCNTs). For MWCNT bundle, D_{out} = *5 nm*. Here, the metal-CNT contacts are assumed to be perfect (both θ_{mc} and R_{mc} are 0). The maximum temperature for each case is also indicated.



(a) (b)

Fig. 14. The maximum temperature rise as a function of **(a)** thermal contact resistance θ_{mc} **(b)** electrical contact resistance R_{mc}, between CNT via and metal (M1/M2). θ_0 is the ballistic thermal resistance of CNT, which varies with different CNT diameter. From the fabrication and measurement work [13], θ_{mc} may range from 0 to $2\times\theta_0$.

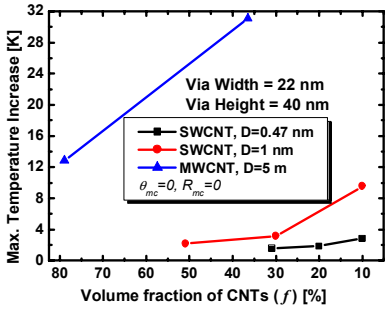


Fig. 15. The maximum temperature rise with decreasing volume fraction of CNTs in via (f), which can be regarded as the density of CNT bundle. f is calculated using equation shown in **Fig. 1**. The highest f of SWCNT bundles reduces as diameter approaches to the Van der Waal's gap.

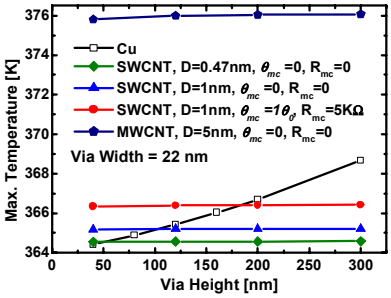


Fig. 16. The maximum temperature rise with increasing via height (with via width = 22 *nm*) for densely packed CNT vias (for different diameters, θ_{mc} and R_{mc} values) and Cu via. For Cu via, the temperature rises with increasing via height, whereas the temperature of CNT via stays nearly constant.