The Effect of Interconnect Scaling and Low-k Dielectric on the Thermal Characteristics of the IC Metal

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Abstract

The effect of interconnect scaling and low-k dielectric on the thermal characteristics of interconnect structures has been characterized for the first time under DC and pulsed current conditions. It is shown that under DC conditions the thermal impedance of metal lines increases by about 10% when the low-k dielectric is used as the gap fill. The critical current density for the low-k structures under pulsed condition is shown to be about 10-30% lower than that of standard dielectric structures depending on metal and pulse widths.

Introduction

Aggressive scaling of Si based IC devices motivated by the desire for faster circuit speed and higher packing density has increased the functional complexity of VLSI circuits. This has in turn, reduced the interconnect metal pitch and increased the number of metallization levels. Reduction in metal pitch however degrades interconnect RC delay which tends to curtail the benefits of interconnect scaling [1]. Low dielectric constant (Low-k) materials have been introduced [2] as an alternative intra-level insulator to reduce interconnect capacitance (therefore delay) and cross-talk noise to enhance circuit performance. Recently it has been demonstrated that thermal effects, instead of electromigration itself, will start to dominate interconnect design guidelines for advanced high performance interconnects [3,4]. Further, metal lines have been reported to thermally breakdown under high pulsed current stress conditions such as during ESD events [5]. We have recently presented a model for interconnect heating and failure under ESD conditions [6]. Characterization of the effect of interconnect scaling and low-k dielectric material on the thermal behavior of the IC metal is desirable to provide thermal design guidelines in the near future. The purpose of this paper is to comprehend the implications of interconnect scaling using low-k dielectric structures.

Experimental

Two types of different intra-level dielectric were used in this study. Both had a double level metallization process. The standard dielectric process had SiO_2 (k~4) as the insulating material everywhere, while for the low-k process, a dielectric with k~3 was used as the gap fill insulator [7] for the level 1 metallization only. The metal system was multilayered with the stacking sequence of TiN/AlCu/TiN. All the metal lines were standard NIST recommended 1000μm long test structures with varying line width (3μm, 1.5μm and 0.75μm). A standard transmission line pulsing technique [8] was used to generate high constant current pulses of varying widths (Δt=100ns, 200ns and 500ns) and magnitudes. The voltage, and hence the resistance of the metal lines increased linearly with time during all the pulsing events.

Thermal Characterization

Initially the DC joule heating was measured for all the structures. Fig. 1 shows the effect of interconnect scaling on the self heating of metal 1 lines. The self heating gets more severe for smaller line widths for a given input power. This result is due to the fact that under DC conditions most of the joule heat generated is dissipated through the underlying oxide layer to the Si substrate which acts like a heat sink. Scaling reduces the effective surface area in contact with this underlying oxide. Fig. 2 shows the same effect with low-k dielectric. Apart from the increase in self heating with decreasing line width the temperature rise (ΔT) is higher for all input powers (P). These results indicate that the thermal impedance (θ_j) defined by

$$\Delta T = P \cdot \theta_j \qquad (1)$$

increases as line width decreases and that interconnect structures with low-k materials have even higher thermal impedance that gets worse with scaling as shown in Fig. 3. Fig. 4 shows the self heating of 3μm metal lines for a 100 ns pulse for the standard dielectric process. It is observed that the metal lines are heated well beyond their melting point. The open circuit failure occurs at a ΔT of 1000 °C [6]. Similar heating behavior is observed for other pulse widths. At the point of open circuit failure the thermal stress generated by the molten metal exceeds the fracture strength (~1GPa) of the passivating layers. Also, ΔT is identical for both metal 1 and 2. This shows that the underlying oxide thickness has no impact on the ΔT (contrary to what is generally observed under DC conditions) and that the lines have identical thermal capacities. Such behavior arises due to the fact that the pulse widths are much smaller than the thermal time constants (~2μs) of the interconnect structures. As a result, the total underlying oxide thickness doesn't influence the self heating of metal lines under these short time current pulses. Fig. 5 demonstrates this effect, where the input pulse energy (E) defined by

$$E = \int_0^{\Delta t} I \cdot V dt \approx \frac{1}{2} I^2 \Delta t [R_f + R_i] \qquad (2)$$

is plotted against ΔT. Here, I is the current, V is the voltage across the line, R_f and R_i are the final and initial resistance during the pulsing event. Since the inverse of the slope of this

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line gives the thermal capacity (C_{th}) of the metal system, defined by

$$E = C_{th} \cdot \Delta T \quad (3)$$

we can see that thermal capacities of metal 1 and 2 are identical. The minimum energy required to melt the given volume of the 3μm wide AlCu line was calculated to be 8μJ, including the latent heat of fusion. However, it can be observed from Fig. 5 that the energy dissipation capability of the interconnect structure is much larger. This suggested that a thin sheath of surrounding insulator was also getting heated up during the current pulse and the failure temperature is higher than the melting temperature. Fig. 6 shows similar self heating effect for the low-k dielectric process. Contrary to the standard dielectric process it can be observed that metal 1 heats up and fails more quickly than metal 2. To comprehend this observation the ΔT is plotted as a function of pulse energy in Fig. 7. It is observed that metal 1 requires less energy to heat up to a given temperature. This is due to the dissipation of a smaller fraction of heat energy into the surrounding dielectric. The different thermal response of the low-k interconnect structure is explained below.

The thermal capacity of metal 1 as extracted from Fig. 7 is smaller than the thermal capacity of metal 2. This is expected since the low-k material has a lower thermal conductivity and therefore the thermal diffusion length into the low-k material is shorter. Due to this smaller thermal capacity effect in the low-k dielectric structures the fraction of the pulse energy that goes into the dielectric is lower and thus the metal fails at a lower current density. This was observed for all the other pulse widths as well and the results are summarized in Fig. 8. Note that the critical current densities decrease with increasing pulse widths. It should also be noted that the open circuit failure temperature is nearly constant (1000 °C) for all the pulse widths and for both processes in agreement with earlier work [6]. Further, the effect of the low-k dielectric gets stronger for longer pulse widths. This is due to the fact that as heat diffusion time increases, the effect of the lower thermal conductivity of the low-k material becomes more prominent. Fig. 9 shows this effect of thermal capacity increase with increasing pulse width for a 3μm line. This is due to the increasing thermal diffusion length (l_d) into the surrounding dielectric with time. This is expected, since from heat diffusion theory we expect the thickness of the insulator sheath to be proportional to $(\Delta t)^{1/2}$.

$$l_d \propto \sqrt{\frac{\kappa \cdot \Delta t}{\rho \cdot c}} \quad (4)$$

Where κ is the thermal conductivity, ρ is the density and c is the specific heat of the material. Therefore, the thickness of the heated insulator sheath increases with increasing pulse width and the results for both the standard dielectric and the low-k structures is shown in Fig. 10. This explains why the standard dielectric provides a larger sheath thickness, and therefore a bigger extra thermal capacity. As a result of the smaller thermal capacities of the low-k process the critical current densities for failure are also relatively smaller for all pulse widths as shown in Fig. 11. The $J_{critical}$ values are ~10% lower for the low-k structures and gets further reduced for longer pulses which carry more energy.

The effect of interconnect scaling on the heating of metal lines with short duration pulsed current is shown in Fig. 12. It is observed that the wider metal lead (3μm) heats up more quickly as compared to the narrower lines. This is due to the smaller surface area to volume ratio for the wider lead. Hence smaller J is needed to reach the same ΔT. Similar effects were observed for the other pulse widths. This result can be better explained using principles of thermal physics. As shown in Fig. 13 the thermal capacities decrease with narrower line widths as expected and the low-k structures have even smaller thermal capacities as discussed earlier. When the ratio of the experimental thermal capacity to the theoretical thermal capacity is plotted against various line widths (Fig. 14), it is observed that this ratio increases with scaling. This explains the results of Fig. 12. Finally, in Fig. 15, the effect of interconnect scaling using low-k dielectric is illustrated. The $J_{critical}$ values are ~10-30% lower for the low-k structures and show a tendency to be getting even lower for sub-micron lines with longer pulse widths.

Conclusions

A low-k dielectric process, which uses the low-k dielectric for metal 1 gap fill only, raises the DC thermal impedance of metal 1 by about 10%. The thermal impedance under short current pulse increases even more and the critical failure current density is reduced by 10 to 30% depending on line and pulse widths. These thermal characteristics will have significant implications on the design of future deep sub-micron VLSI interconnects that employ low-k dielectrics and must be considered while developing electromigration, ESD/EOS and I/O buffer interconnect design rules.

Acknowledgments

The authors would like to acknowledge W. Hunter and R. Havemann of TI for their support and encouragement during various phases of this work. They would also like to thank the SRC (IJ-148), and the MICRO program for their continued support.

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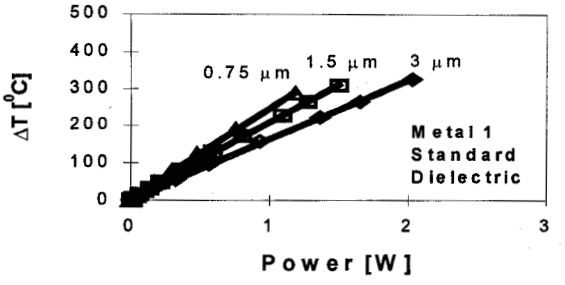

Figure 1. Effect of interconnect scaling on the DC self heating of metal 1 lines with the standard dielectric.

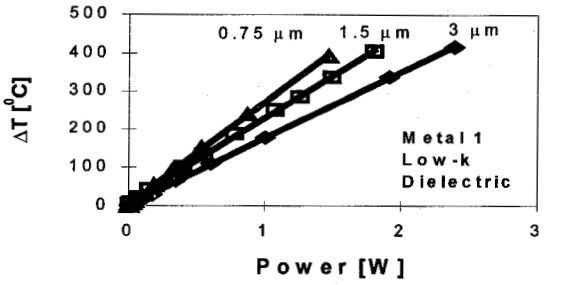

Figure 2. DC self heating effect of metal 1 lines with the low-k dielectric is more severe.

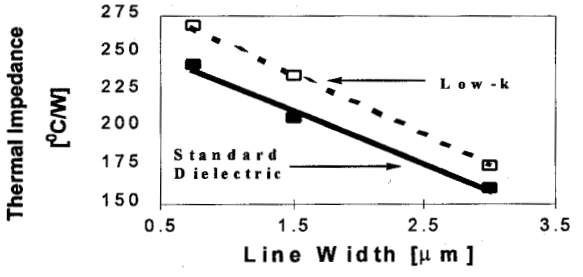

Figure 3. Thermal impedance of metal 1 is higher for the low-k dielectric and increases further as line width decreases.

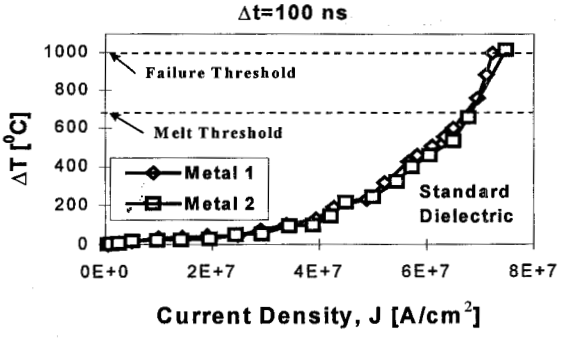

Figure 4. Self heating and failure for 3 μm X 1000 μm metal lines for a 100 ns pulse shown for the standard dielectric process.

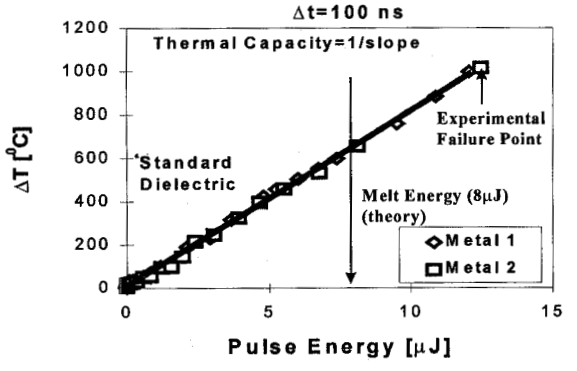

Figure 5. The thermal capacity of (3μm) metal 1 and metal 2 is identical in case of the standard dielectric process in agreement with Fig. 4.

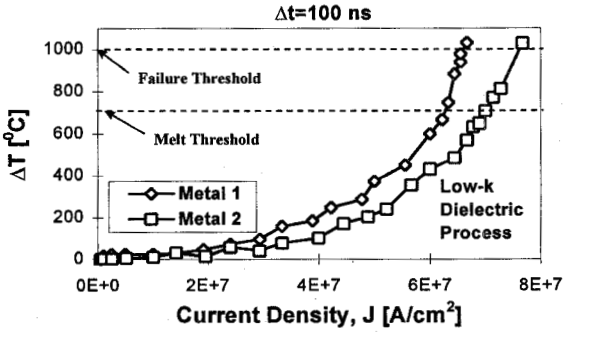

Figure 6. Self heating and failure for 3 μm X 1000 μm metal lines for a 100 ns pulse with metal 1 embedded in low-k along the sides (gap fill).

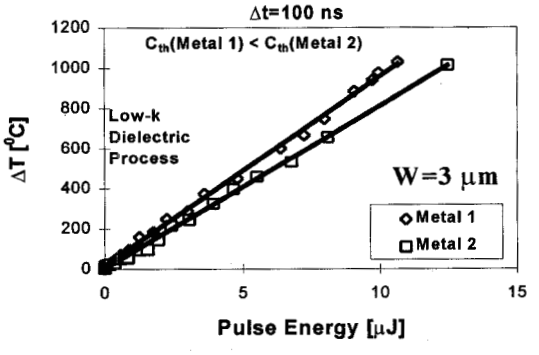

Figure 7. Thermal capacity (Cth=1/slope) of metal 1 is less than that of metal 2. Metal 1 with low-k requires ~7μJ and metal 2 without low-k requires ~9μJ to reach the melt temperature of ~660 °C.

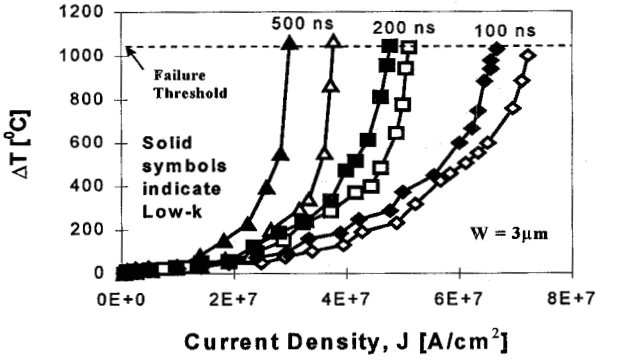

Figure 8. Effect of low-k dielectric on the critical current density in 3μm X 1000μm metal 1 leads summarized for various pulse widths.

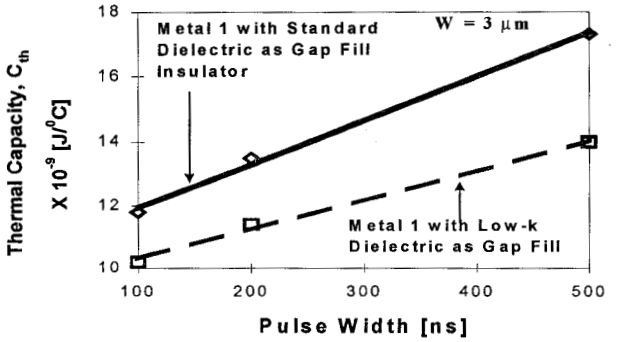

Figure 9. Thermal capacity increases with pulse width and is relatively lower for the low-k embedded metal.

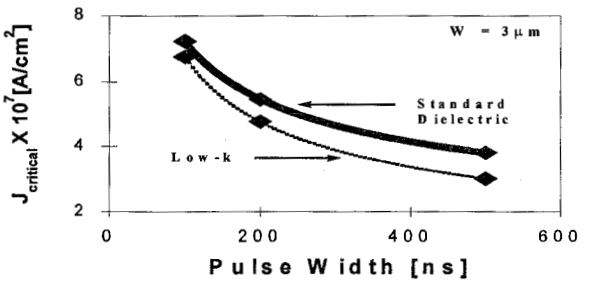

Figure 11. Critical current density of metal 1 leads decreases with increasing pulse width. For the low-k structures, $J_{critical}$ is further lowered by about 10%.

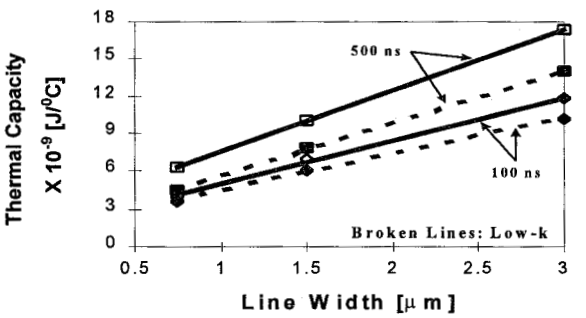

Figure 13. Thermal capacity variation with interconnect scaling and the effect of low-k dielectric for various pulse widths. The relative effect of low-k on the thermal capacities is larger for narrower metal leads and wider pulse widths.

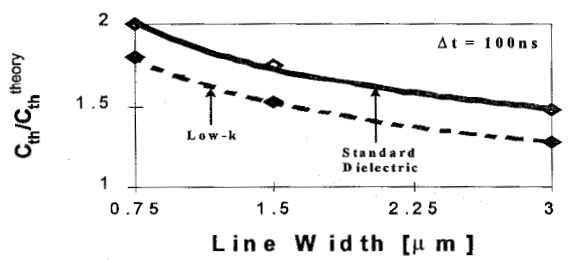

Figure 14. Ratio of experimental and theoretical thermal capacities increases with scaling due to increasing heat conduction into the oxide sheath.

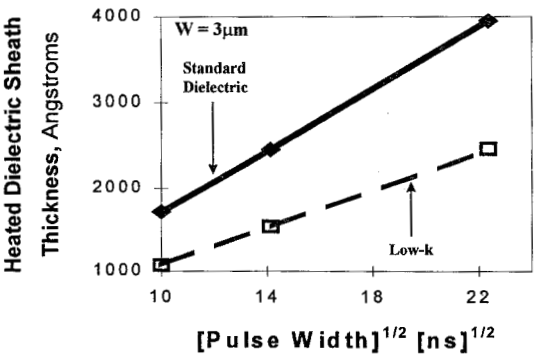

Figure 10. Thickness of the heated dielectric sheath is lower for the low-k material, which results in their lower thermal capacities as shown in Figure 9.

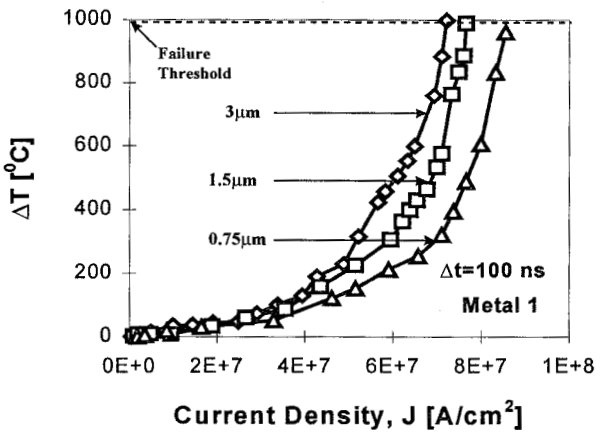

Figure 12. Effect of line width reduction on metal heating. The wider lines heat up more rapidly owing to their smaller surface area to volume ratio (for metal 1 standard dielectric process).

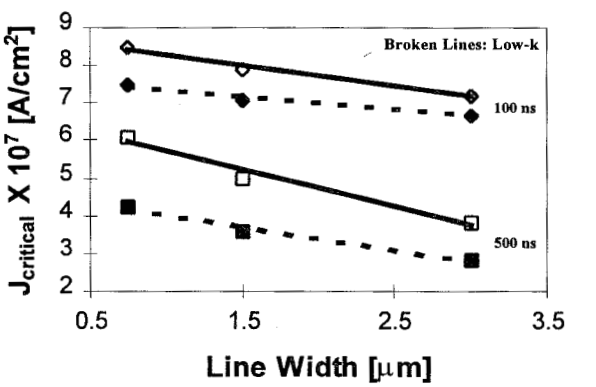

Figure 15. Effect of interconnect scaling and low-k dielectric on the critical current density for metal 1 leads stressed by current pulses of varying widths. $J_{critical}$ increases for decreasing line width as shown in Fig.12. The effect of low-k lowers the critical values further. As line widths gets smaller and pulse widths get larger the effect of low-k gets even worse.