Temperature and Current Effects on Small-Geometry-Contact Resistance

Kaustav Banerjee, Ajith Amerasekera*, Girish Dixit*, and Chenming Hu

Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720

**Semiconductor Process and Device Center, Texas Instruments Inc., 13570 N. Central Expressway, M/S 3702, Dallas, TX 75243*

Abstract–The effects of temperature and current on the resistance of small geometry silicided contact structures have been characterized and modeled for the first time. Both, temperature and high current induced self heating have been shown to cause contact resistance lowering which can be significant in the performance of advanced ICs. It is demonstrated that contact-resistance sensitivity to temperature and current is controlled by the silicide thickness which influences the interface doping concentration, N. Behavior of W-plug and force-fill (FF) Al plug contacts have been investigated in detail. A simple model has been formulated which directly correlates contact resistance to temperature and N. Furthermore, thermal impedance of these contact structures have been extracted and a critical failure temperature demonstrated that can be used to design robust contact structures.

I. Introduction

Contact resistance (R_c) between the silicide and doped Si source/drain regions of advanced MOSFETs constitutes a significant fraction of the parasitic series resistance in the path of the drain current, thereby contributing to a loss in circuit performance. Modulation of this contact resistance at high current levels is known to affect the MOS linear region I-V characteristics [1]. Aggressive scaling of IC devices has resulted in smaller contact sizes and higher current densities. Recently it has been demonstrated that thermal effects, instead of electromigration will become more important in the design of advanced high performance interconnects [2]. Electrical characterization of temperature and current effects on the behavior of small-geometry-contact resistance is therefore necessary to comprehend the full impact of their parasitic behavior on transistor and circuit performance. The purpose of this work is twofold, first to understand the effects of temperature and current on small-geometry-contact resistance and develop a physical model of their behavior, second to extract thermal parameters and a conservative upper limit of temperature above which the contact structures exhibit degradation.

II. Temperature & Low Current Effects on R_c

The different contact technologies that were studied are listed in Table 1. Fig. 1 shows a schematic cross section along with a TEM micrograph of a W-contact structure. In all the measurements n+ Si was negatively biased relative to TiSi2 and p+ Si was positively biased relative to TiSi2. Fig. 2a shows that the contacts display good ohmic behavior.

Contact Plug Material	Contact Size	Substrate	TiN liner Thickness	TiSi2 Thickness
CVD-W	0.30 μm	n+/p+ Si	20 nm	35 nm
CVD-W	0.30 μm	n+/p+ Si	20 nm	9.0 nm
FF-Al	0.30 μm	n+/p+ Si	20 nm	9.0 nm

Table 1. Contact technologies evaluated in this study. The contact plug processes are chemical vapor deposited (CVD) W and force-fill (FF) Al. Silicide was formed from physical vapor deposited (PVD) Ti in all cases.

However, it can be observed that the contacts to p+ Si have higher resistance and greater nonlinearity in the I-V characteristics. Fig. 2b clearly shows that the resistance of contact to p+ Si is more sensitive to current and temperature.

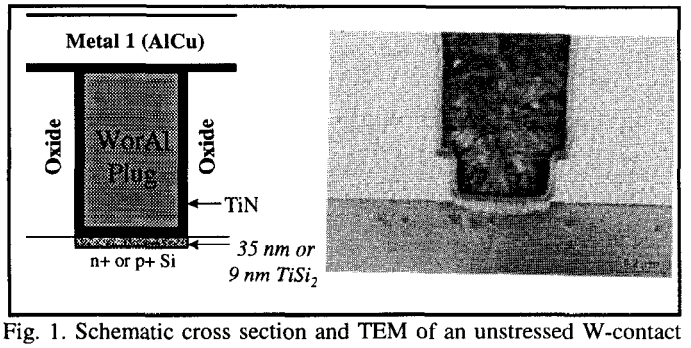
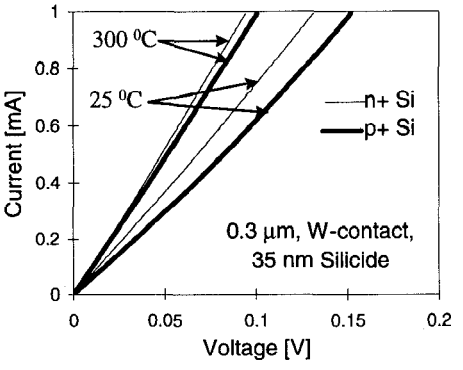
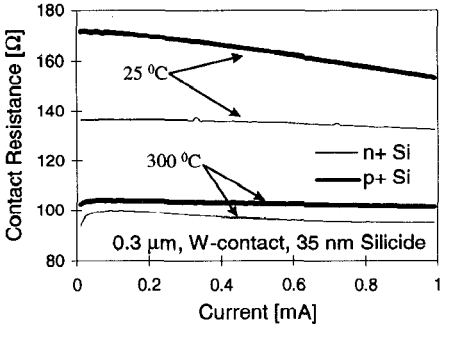


Fig. 1. Schematic cross section and TEM of an unstressed W-contact with silicide and TiN barriers.



a)



b)

Fig. 2. a) I-V characteristics of W-contact structures with 35 nm silicide. b) Contact resistance sensitivity with current (low current regime) at two different temperatures for W-contacts to n+ and p+ Si.

0-7803-4100-7/97/$10.00

Fig. 3 depicts the behavior of the contact resistance with ambient temperature for the W-contact with thick silicide. Kelvin structures were used for the contact resistance measurements. A small current corresponding to a voltage < 0.02 V was used for these measurements. Also, since the resistance of a 0.3 μm W or Al plug is known to be only ~3-4 Ω [3], most of the contact resistance comes from that of the TiSi2/Si barrier. Thus R_c values are independent of the contact plug material.

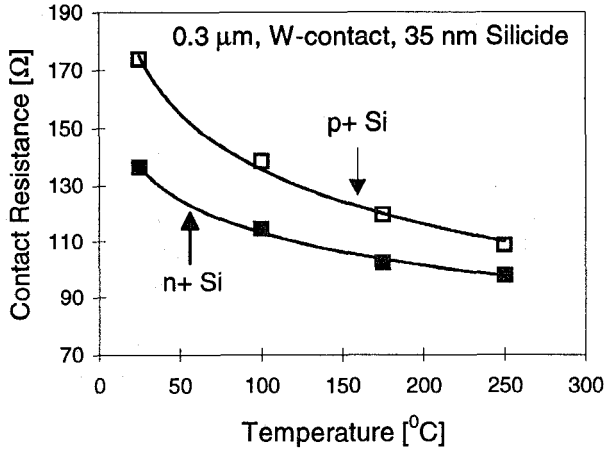


Fig. 3. Contact resistance decrease with temperature for n+ and p+ W-contacts. The p+ contact shows larger temperature sensitivity.

Under such small current (voltage) conditions the contact resistance values were found to be weakly dependent on the polarity of the bias. Therefore, all the contact resistance measurements were carried out under a single polarity condition as stated earlier. It can be observed from Fig. 3 that contact resistance decreases with temperature and that contact to p+ Si shows a bigger temperature sensitivity. This explains the larger current sensitivity of the contact to p+ in Fig. 2b. Being more sensitive to temperature, it is more sensitive to self -heating and therefore more sensitive to current.

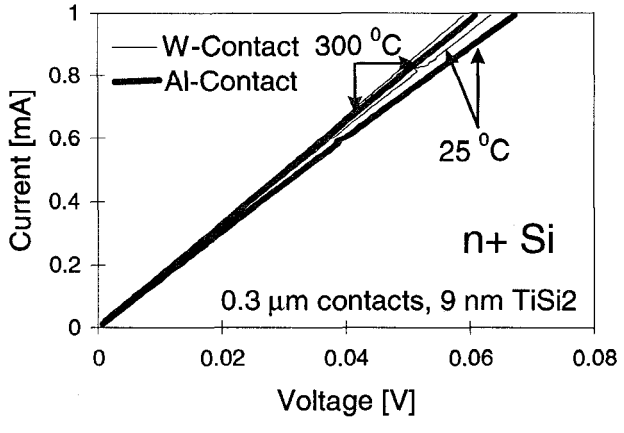


Fig. 4. I-V characteristics of W and Al plug contacts to n+ Si with 9 nm silicide gives nearly equal contact resistance and are only slightly temperature sensitive.

Fig. 4 shows the I-V characteristics of both W and Al plug contacts to n+ Si where the silicide thickness is only ~ 9 nm. It is observed that unlike the W-contact with the thicker silicide, these contacts are more ohmic in character and shows very little sensitivity to temperature, and therefore to current.

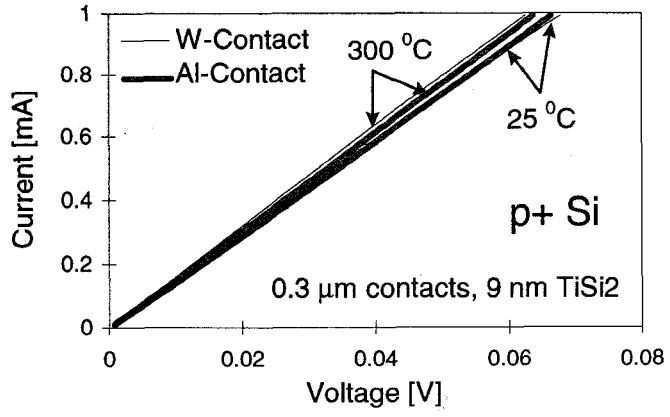


Fig. 5. I-V characteristics of W and Al plug contacts to p+ Si with 9 nm silicide gives nearly identical contact resistance values as compared to those of n+ Si and are also only slightly temperature sensitive.

As the silicide thickness increases more dopants may segregate into the silicide and the interface moves down into the Si where the doping concentration may be lower. Thinner silicide therefore results in a silicide-Si interface with a higher impurity doping concentration. Higher doping concentration with thin silicide results in a narrower depletion region (smaller barrier width), enhanced tunneling, and lower contact resistance. Fig. 5 shows similar results for contacts with thin silicide to p+ Si. It can also be noticed from Fig. 4 and Fig. 5 that for the thin silicide case the contact resistance to n+ and p+ Si is nearly identical unlike the thick silicide case. All these differences will be explained with a model presented in the next section.

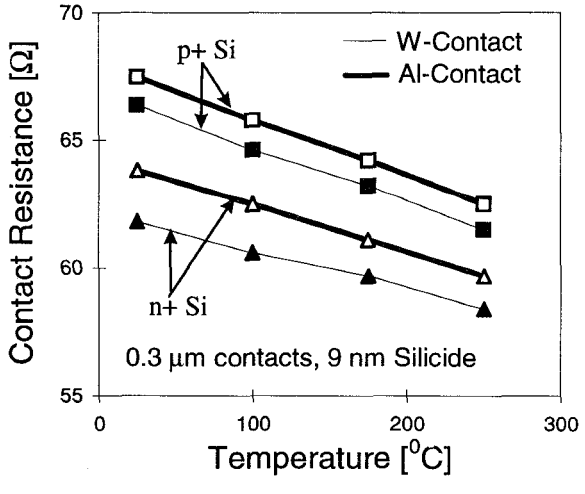


Fig. 6. Temperature sensitivity of the contact resistance of W and Al plug contacts with 9 nm silicide.

Fig. 6 shows the temperature sensitivity of the contacts to n+ and p+ Si for both the W-plug and the Al plug processes with 9 nm thick silicide. It is observed that these contacts have smaller contact resistance, and decrease very slowly with temperature.

III. Contact Resistance Model

For contacts to heavily doped ($N > 10^{17}$ cm^{-3}) n and p type Si, tunneling is the dominant carrier transport mechanism [4-5] and the contact resistance is known to vary exponentially with the factor ($B/\sqrt{N}$) [6], where B is dependent on the barrier height ϕ_b, and the tunneling effective mass, and N is the impurity doping concentration at the metal-semiconductor interface. The temperature and dopant concentration dependent contact resistance to n+ and p+ Si can be expressed as

$$R_c^n(T) = H\exp\left[\frac{B_n(T)}{\sqrt{N_n}}\right] \quad (1)$$

and

$$R_c^p(T) = H\exp\left[\frac{B_p(T)}{\sqrt{N_p}}\right] \quad (2)$$

respectively. Here H is a constant. Indices n and p are used to distinguish between n+ and p+ Si. Using equation 1 and 2 and the temperature dependent contact resistance values in Fig. 3 and Fig. 6, values of H, $B_n(T)$, $B_p(T)$, N_n and N_p have been determined that can be used to calculate the doping concentration from a knowledge of the contact resistance and results are shown in Table 2. Fig. 7 gives the temperature dependence of the parameter B for n and p type Si.

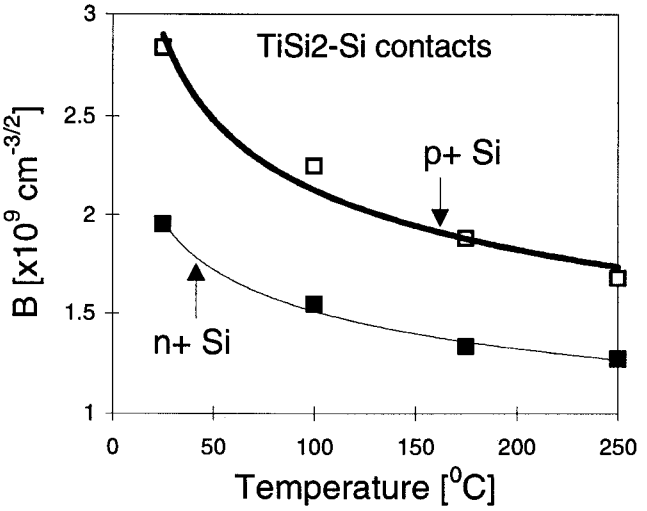


Fig. 7. Temperature dependence of B for n and p type Si.

H = 55.845 Ω

TiSi2 Thickness		Measured R_c [Ω] T=25 °C	T=175 °C	B(T) x10⁹ cm⁻³/² T=25 °C	T=175 °C	Doping Concentration N(SIMS)	N(Model)	Calculated R_c [Ω] T=25 °C	T=175 °C
35 nm	n+:	136.5	102.5	1.954	1.334	4.68x10¹⁸ cm⁻³	4.78x10¹⁸ cm⁻³	136.5	102.79
	p+:	173.77	119.6	2.836	1.881	6.24x10¹⁸ cm⁻³	6.54x10¹⁸ cm⁻³	171.07	116.53
9 nm	n+:	61.8	59.7	1.954	1.334	3.28x10²⁰ cm⁻³	3.28x10²⁰ cm⁻³	62.20	60.11
	p+:	66.4	63.2	2.836	1.881	3.74x10²⁰ cm⁻³	3.74x10²⁰ cm⁻³	64.67	61.55

Table 2. Comparison of measured and calculated contact resistance values using the model. Here, only the doping concentration for 9 nm TiSi2 contact was provided by the SIMS data. All other parameters like B, H and N (for 35 nm TiSi2) were extracted from contact resistance data.

IV. High Current Effects on R_c

Fig. 8 shows the high current (DC) behavior of the contact structures (under positive bias) with 35 nm silicide. It can be observed that resistance decreases with increasing current. This is simply due to self heating as explained earlier. Fig. 8 is used along with Fig. 3 to plot the input power, P vs. temperature rise, ΔT in Fig. 9. It can be observed that the thermal impedance for both the n+ and p+ structures are nearly identical as expected. The slope of the best fit line gives the thermal impedance θ_j of the contact system defined by,

$$\Delta T = P \cdot \theta_j \quad (3)$$

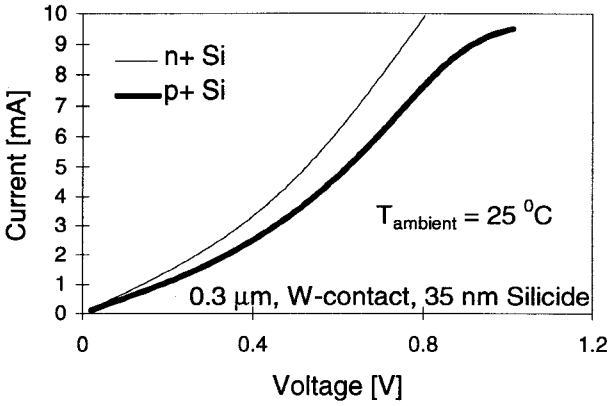


Fig. 8. I-V characteristics of n+ and p+ contacts in the high current regime becomes non linear due to severe self heating.

and is extracted to be ~ $7.5x10^4$ °C/W. The self heating at the current design rule (~ 1 mA) for contacts is shown to be ~ 10 °C. The thermal impedance extracted from Fig. 9 is used to estimate the critical temperature for the contacts to fail.

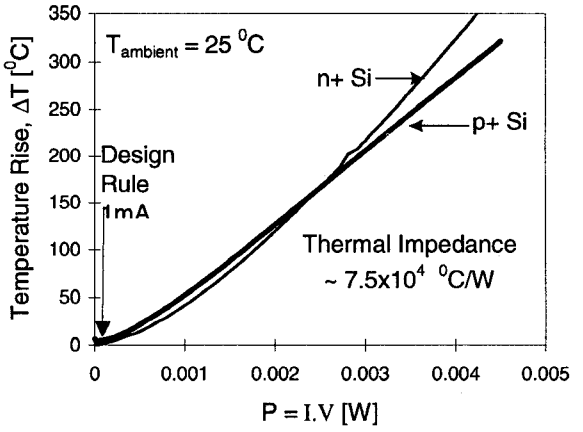


Fig. 9. Thermal impedance of n+ and p+ contacts extracted from Fig. 3 and Fig. 8 at an ambient temperature of 25 °C are equal.

The critical temperature is shown to be ~ 1400 °C in Fig. 10. This suggests that the silicon near the interface reaches melt temperature and the TiSi2 gets dissolved in it forming some polycrystalline Si rich compound. Also the failure current was found to be independent of

the TiSi2 thickness and the contact plug material. The actual failure site is difficult to capture under DC stress, since the contact is usually completely destroyed. Since, the barrier resistance dominates the net contact resistance, maximum heat dissipation also takes place near the interface. In order to capture the degradation front, a pulse Kelvin set up [3] was employed and the contacts were stressed in small increments of current by a single 500 ns pulse. Fig 11 shows a TEM micrograph of a contact stressed just into degradation showing failure location.

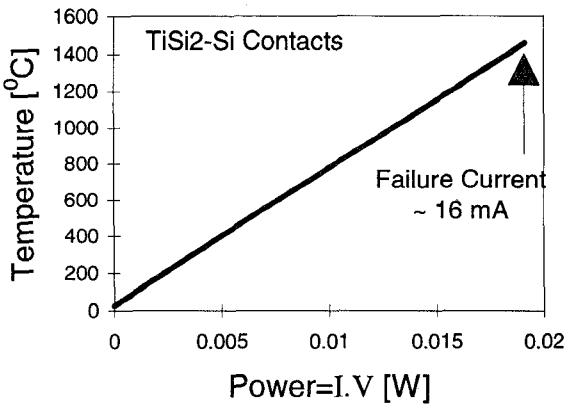


Fig. 10. Temperature rise at the point of failure under high current conditions is determined from the thermal impedance in Fig. 9.

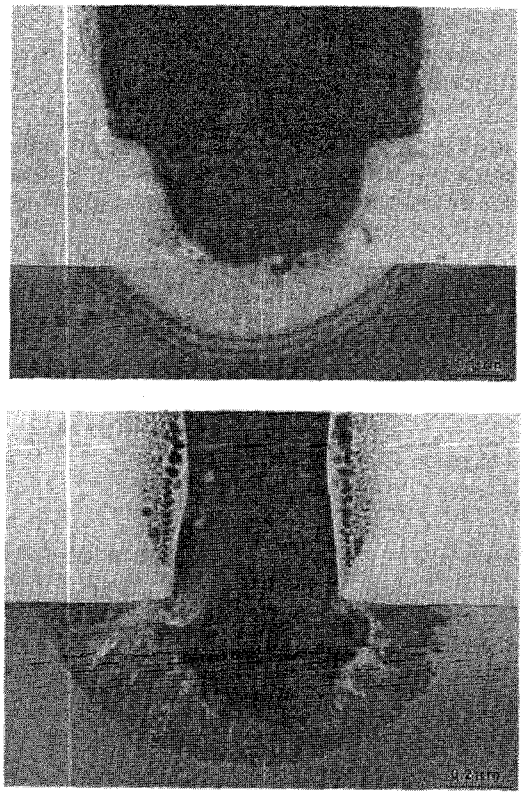


Fig. 11. TEM micrographs of 0.3 μm W-contacts showing progression of failure at the silicide-Si interface. The TEM on top shows initiation of the failure and the one on the bottom shows a contact that has undergone severe degradation.

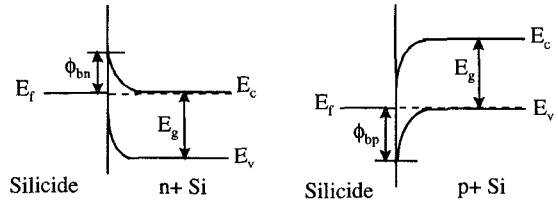


Fig. 12. Silicide-Si band diagram illustrating Fermi level pinning.

V. Discussion & Conclusions

The negative temperature dependence of the parameter B used in equation 1 and 2 is believed to be mainly due to the temperature dependence of the barrier height because the tunneling effective mass is expected to give a weak positive temperature dependence of B. Therefore both ϕ_{bn} and ϕ_{bp} (shown in Fig. 12) must decrease with increasing temperature. The temperature dependence of B for n+ and p+ Si indicates that the Fermi level E_f is not pinned at the same point in n+ and p+ semiconductor. Note that the band gap E_g decreases by only 0.043 eV between 25 ^{0}C and 175 ^{0}C, which in itself cannot explain the decrease in R_c with temperature.

In conclusion, a model for temperature and current effects on the resistance of small-geometry TiSi2/Si contact has been presented. The pre exponential term H is found to be independent of temperature and the barrier height ϕ_b is found to be temperature dependent. One can now predict the effect of temperature and doping concentration on the TiSi2/Si contact resistance. It is shown that temperature and current induced self heating can change contact resistance and that the silicide thickness can be adjusted to design robust, low resistance contact structures. Further, a critical temperature for contact failure has been estimated and the failure mechanism has been identified.

Acknowledgment

This work was funded by Texas Instruments, MICRO, and the SRC (96-IJ-148A). The authors would also like to thank W. Hunter and R. Havemann of SPDC, Texas Instruments for their support and encouragement, and T. Breedijk (SPDC, TI) for the SIMS data.

References

[1] D. B. Scott et al, "Titanium disilicide contact resistivity and its impact on 1-μm CMOS circuit performance", *IEEE Trans. Electron Devices*, Vol., ED-34, No. 3, pp. 562-574, 1987.

[2] W. R. Hunter, "The implications of self-consistent current density design guidelines comprehending electromigration and joule heating for interconnect technology evolution", *Tech. Dig. IEDM*, pp. 483-486, 1995.

[3] K. Banerjee et al, "Characterization of contact and via failure under short duration high pulsed current stress", *Proc. IRPS*, pp. 216-220, 1997.

[4] F. A. Padovani and R. Stratton, "Field and thermionic-field emission in Schottky barriers", *Solid State Electronics*, Vol. 9., pp. 695-707, 1966.

[5] C. Y. Chang and S. M. Sze, " Carrier transport across metal-semiconductor barriers", *Solid State Electronics*, Vol. 13., pp. 727-740, 1970.

[6] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, pp. 305, 1981.