Gate Bias Induced Heating Effect and Implications for the Design of Deep Submicron ESD Protection

Kwang-Hoon Oh, Charvaka Duvvury*, Kaustav Banerjee, and Robert W. Dutton

Center for Integrated Systems, Stanford University, CA 94305
*Silicon Technology Development, Texas Instruments, Dallas, TX 75243
Phone: 650-723-9484; Fax: 650-725-7731; e-mail: okhoon@gloworm.stanford.edu

Abstract

This paper presents a detailed investigation of the degradation of ESD strength with gate bias for various deep submicron ESD protection designs. It has been shown for the first time that gate bias induced heating is the primary cause of this degradation. It has also been established that substrate biasing can help eliminate the negative impact of the gate bias effect, which has significant implications for the design of ESD protection circuits in deep submicron technologies.

Introduction

For multi-finger NMOS protection, it has been recognized that the gate coupling technique is efficient by ensuring uniform triggering of the lateral NPN [1, 2], although its effectiveness is dubious in silicided processes [3]. However, it is also well known that excess gate coupling degrades the second breakdown triggering current (I_{t2}) of NMOS devices and thus design techniques have been used to limit the gate *coupling [4]*. Even with controlled gate coupling on the protection device, under ESD stress, high gate coupling on the output NMOS transistor (see Figs. 1 to 3) causes HBM/CDM failures and places some restrictions in the design of ESD protection. Hence, the early failure of the NMOS transistor caused by gate coupling should be clearly characterized and modeled for the optimum design of ESD protection. The physical mechanism for this I_{t2} degradation with gate bias and its dependence on the finger width for advanced NMOS transistors has not been reported. This work establishes the root cause of I_{t2} degradation with gate bias by modeling the channel heating phenomenon. For advanced technologies, the severity of this effect has been shown to be dependent on the finger width and the extent of lateral uniformity of ESD current conduction. This work also establishes that the substrate bias enhanced triggering can have an impact on gate bias effect, and hence on the ESD protection as well.

Output NMOS Failure

The typical output buffer protection scheme with different protection device options is shown in Fig. 1. In ESD protection circuits, the gate grounded NMOS (GGNMOS) or the gate coupled NMOS transistors (GCNMOS) are widely used as protection devices that can provide a discharging current path during ESD events. More recently, the substrate pump NMOS structure has been introduced to ensure uniform lateral bipolar current conduction *[5, 6]*. Under ESD stress from I/O pad to the ground, the high ESD current is shared by the different competing current paths, mostly through the NMOS protection structure, and partially through the lateral V_{dd} diode and the output NMOS transistor itself. During such conditions, the potential of the I/O pad reaches the triggering voltage of the lateral NPN (V_{t1}) for the protection NMOS, and snaps back to the holding voltage (V_h). The ESD current through the lateral diode to V_{dd} node charges up the V_{dd} capacitance up to V_h - 0.7V. As a result, this voltage (at V_{dd}) can be fed into the gate of the output NMOS transistor through internal circuit blocks, which can influence the effectiveness of the ESD protection design. As shown in Fig. 2, the early failure of the output NMOS transistor has been seen for HBM due to the degradation of I_{t2}, regardless of the ESD strength of the protection device itself. The same failure mode has also been observed for the charged device model (CDM). By using HSPICE simulation, 2KV HBM test mode was reproduced as shown in Fig. 3. Initially, all the nodes are floating, and then voltages at the I/O pad and V_{dd} start to increase with the injection of HBM current. The gate voltage of the output NMOS transistor is determined depending on the condition of the pre-drive circuits to the output devices. If gn_1, gn_2, gp_1 and gp_2 nodes are at ground (Fig. 3 (b)), the gate voltage (V_{gn}) of the output NMOS transistor follows the voltage of V_{dd} node with a slight delay, and finally goes higher than that of the protection NMOS device (V_g), which leads to a reduction in the ESD strength relative to the protection device. On the other hand, in the condition that gn_1 and gn_2 are at ground and gp_1 and gp_2 are at V_{dd}, the gate potential of the output NMOS stays around 0.5V (Fig. 3 (c)). For the simulation, the gate voltage of the output NMOS transistor ranges from 0.5V to V_{dd} (~ 4.8V). Similar effects take place for any V_{dd}. Therefore, the gate bias effect for the output NMOS is important.

Experiments and Analysis

In this study, 1.5V (L_{poly}= 0.175 μm and t_{ox}= 27 Å) and 3.3V (L_{poly}= 0.5 μm and t_{ox} = 70 Å) single finger ESD NMOS transistors, manufactured using a silicided 0.13 μm technology, have been investigated. In order to identify underlying failure mechanism of the output transistors with gate coupling, involving various gate bias conditions, the second breakdown triggering current (I_{t2}) was measured with the transmission line pulsing (TLP) method using a current pulse width of 200ns. As shown in Fig. 4, the I_{t2} of the NMOS transistors is strongly dependent on the applied gate bias and the technology node. For the 0.35 μm technology node, the degradation of I_{t2} was observed with gate bias. However, the I_{t2} dependence on the gate bias is no longer consistent for the W=20 μm and W=40 μm devices of the 0.13 μm technology node (Fig. 4 (b) and (c)).

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Unlike the dependence observed in the 0.35 μm technology node, contradictory trends appear depending on the gate finger width of the NMOS transistor. This implies that the gate bias can result in two different physical mechanisms depending on the finger width for a given structure. As shown in Fig.5 (a), the I_{t2} values of the advanced silicided transistors are severely degraded with increasing finger widths. The ESD current distribution is uniform within the very narrow finger width such as $W < 5$ μm for the low voltage (1.5V) transistors and $W \leq 10$ μm for the high voltage (3.3V) transistors. In addition, the emission microscopy images of the ESD current distribution shows that only a small part of the finger width is effective for the ESD current conduction in the silicided NMOS devices (Fig. 5 (b)). This strong width dependence of I_{t2} for advanced technologies is attributed to the localized (non-uniform) bipolar conduction. As discussed in [6], this non-uniform bipolar conduction becomes more serious for devices with low resistance substrates and silicided diffusions. According to the results in Fig. 4 and Fig. 5, it can be inferred that gate bias can improve I_{t2} of the wide finger devices (W=20 μm and W=40 μm) where the ESD currents are non-uniform. On the other hand, I_{t2} of the narrow finger device (W=5 μm for the 1.5V NMOS and W=5 μm and 10 μm for 3.3V NMOS) where ESD current is known to conduct almost uniformly, is degraded with gate bias. This reduction in I_{t2} with increasing gate bias is also observed for the 20 μm wide device in the 0.35 μm technology where the bipolar current conduction is also known to be very uniform.

Simulations and Discussion

As is well known, boosting substrate current with gate bias can minimize the current localization under ESD conditions. This mechanism seems to work for the wide finger 1.5V NMOS devices (see Fig.4 (b)) with considerable improvement of I_{t2}, while the improvement of I_{t2} for the 3.3V devices is less apparent (Fig. 4 (c)). However, the severe reduction in I_{t2} with gate bias for the narrow transistors is insensitive to the efficiency of the lateral NPN structure. To comprehend the underlying physical mechanism that leads to early ESD failure, electro-thermal simulations (MEDICI) have been performed for the structure devised using TSUPREM4. The simulations in Fig. 6 (a) show that the current density within the source/drain extension junction depth is strongly modulated by gate bias. This implies that the distribution of the local temperature in the drain extension and the channel area (indicated by the rectangle in Fig. 6 (a)) can also be influenced by the applied gate bias. At a drain current of 5mA/ μm, the local temperature values in the box are shown in Fig. 6 (b). The simulation results show that the distribution of the local temperature near the channel area (within the box) increases as gate bias increases. In addition, it can be clearly noticed from Fig. 7 that the location of the peak temperature resides in the drain extension and it moves closer to the surface with gate bias. Hence this heating effect induced by the gate bias can lead to I_{t2} degradation in devices where the lateral ESD currents flow uniformly. As shown in Fig. 8, the location of the maximum temperature has been simulated with gate bias. For the negative gate bias, the location of the peak temperature doesn't change at all. This simulation result suggests that I_{t2} remains the same with the negative gate bias. This observation agrees well with the measured data in Fig. 4. However, the surface heating becomes stronger with the gate bias since the location of the peak temperature approaches the Si/SiO_2 interface. This means that more heat can be accumulated near the surface with gate bias, and the device tends to be more vulnerable to thermal failures at the surface. To verify this heating effect, I_{t2} was also measured with both the gate and the substrate bias as shown in Fig 9. It was observed that the reduction in I_{t2} disappeared with substrate bias, since the lateral ESD currents conduct more deeply into the silicon substrate with the substrate bias leading to reduced heating near the surface. Hence it can be concluded that gate bias induced heating effect primarily accounts for the reduction in I_{t2} for devices with uniform lateral ESD current conduction. Based on the I_{t2} data for the high voltage transistor (Fig. 9), and considering the impact of the gate bias and the substrate bias, a design window can be established for a given technology as illustrated in Fig. 10. For the substrate trigger protection [5, 6], I_{t2} roll-off with gate bias is not important. In fact, protection can be designed with the gate grounded as long as substrate bias is supplied for an efficient multi-finger NPN. For the output transistor, since the substrate bias is not available and the gate coupling is unpredictable, the buffer size should be designed based on the failure current component that it can handle which depends on its gate coupling level. This design can be done with high current ESD simulations [7]. On the other hand, for the design of the gate coupled ESD protection devices without substrate bias, the protection device gate should be designed with R and C (see Fig. 1 (b)) to maintain the gate bias below the level above which I_{t2} begins to roll-off with the gate bias.

Conclusions

In conclusion, an extensive investigation into the degradation of ESD strength with gate bias for advanced ESD protection designs provides new insight into the gate bias effect. It has been shown that gate bias induced heating is the primary cause of this degradation. It has also been established that substrate biasing can help eliminate the negative impact of the gate bias effect. Results from this work can be used to generate design windows for efficient and robust ESD protection design, including compatible output buffer design, to overcome ESD failures in advanced deep submicron technologies.

- This work was supported by Texas Instruments through a customized SRC task 751.001.

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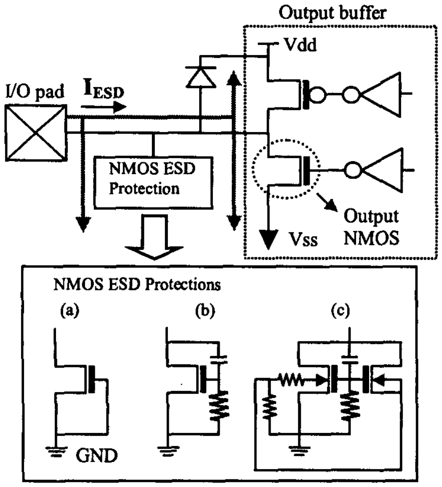

Figure 1. Simplified output buffer protection scheme with various protection NMOS transistor options. Irrespective of protection transistor options, under ESD conditions, high ESD voltage can be fed into the gate of the output NMOS transistor, which can lead to early failures. (The gray arrows indicate the ESD current paths.) (a) GGNMOS, (b) GCNMOS, and (c) substrate pump NMOS

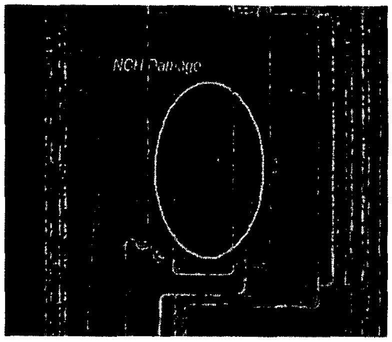

Figure 2. Failure image of the output NMOS transistor in HBM test mode. Since increased gate voltage of the device lowers its ESD strength, the device fails earlier than the protection devices.

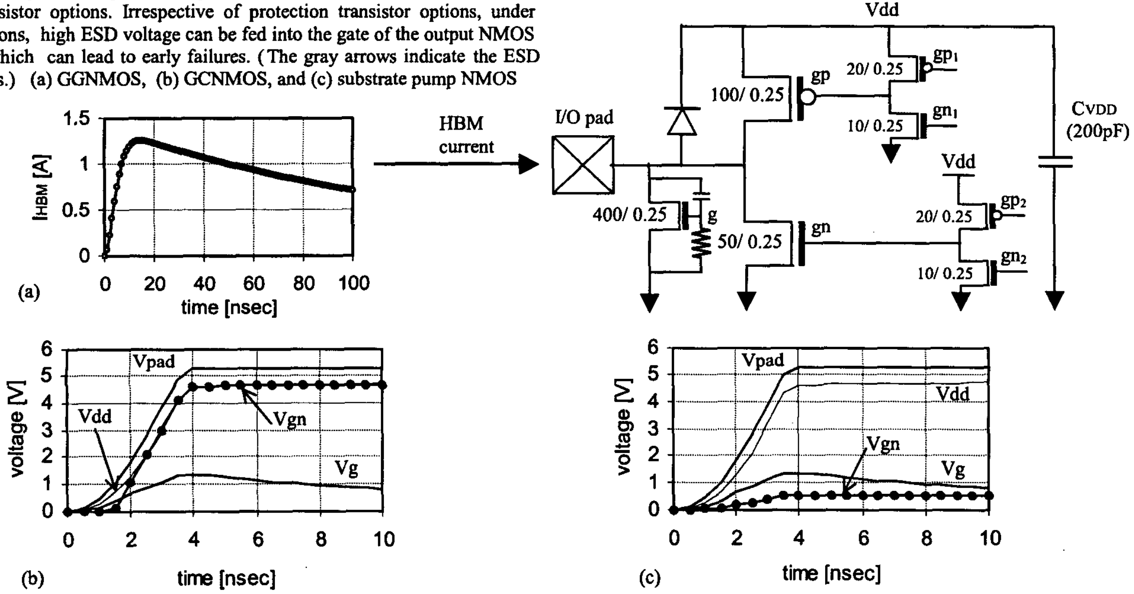

Figure 3. Voltage waveforms of each node in the output buffer protection under 2KV HBM test simulation with the two different pre-drive circuit conditions. (a) circuit schematic in the HSPICE simulation with the HBM current waveform (tr = 10ns) (b) voltage waveforms with the gn_1, gn_2, gp_1, and gp_2 grounded, and (c) voltage waveforms with the gn_1 and gn_2 grounded, and the gp_1 and gp_2 tied to V_{dd}.

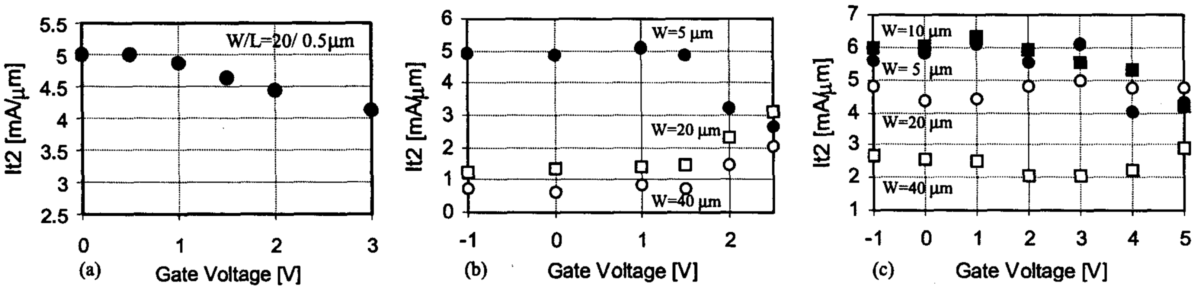

Figure 4. Second breakdown triggering current (I_{t2}) with gate bias for the two different technology nodes. (a) 0.35 μm technology, (b) 0.13 μm technology (1.5V NMOS with L_{poly}= 0.175 μm), and (c) 0.13 μm technology nodes (3.3V NMOS with L_{poly}= 0.5 μm). Both (b) and (c) have different finger widths.

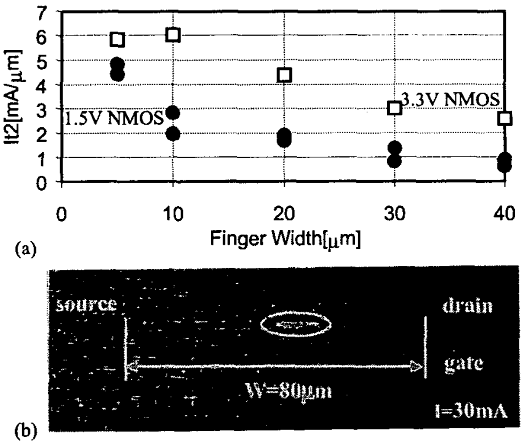

Figure 5. (a) I_{t2} for the output NMOS transistors (both of 1.5V and 3.3V transistors) with Vgs = 0V for different finger widths, and (b) EMMI image of the spatial distribution of ESD current for the 3.3V NMOS transistor. The both show that strong non-uniform conduction occurs for the 0.13 µm technology.

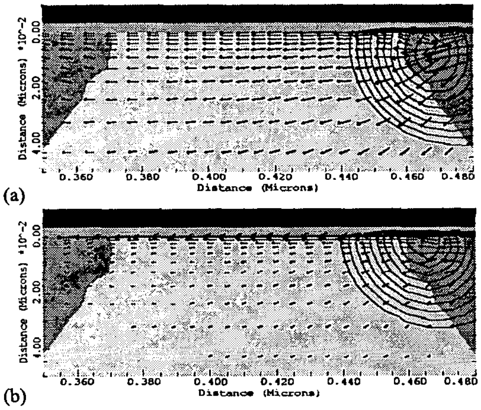

Figure 7. Current vector and temperature distribution contours in the rectangular box (in Fig. 6 (a)). Outer most contour corresponds to 500K and the location of peak temperature becomes shallower with gate bias.
(a) Vgs = 0V, and (b) Vgs = 1.5V

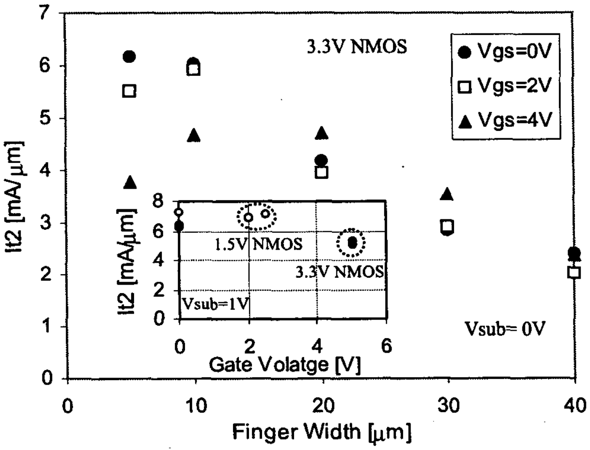

Figure 9. I_{t2} of the high voltage transistor with finger widths for the various gate voltages, and the effect of the external substrate bias on the I_{t2} degradation (inner figure).

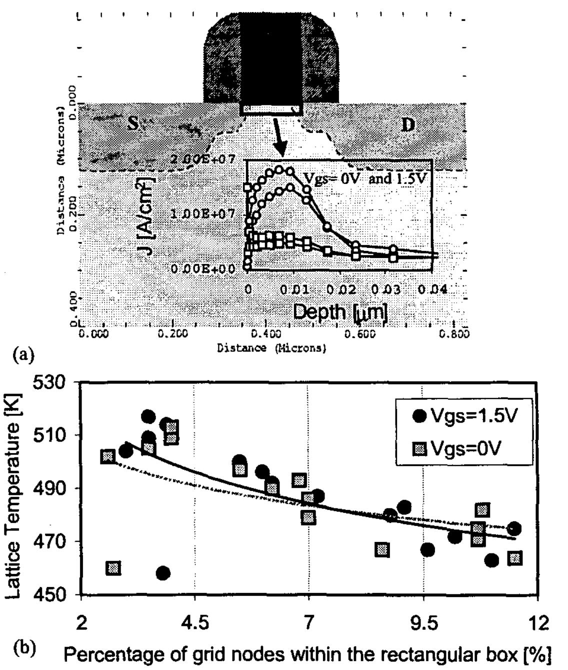

Figure 6. (a) The simulation structure and the current density at the drain current of 5mA/ µm in the rectangular box (below the gate) where the current density is strongly modulated by the gate bias (circles: at the drain end and squares: at the source end), and (b) Overall temperature distribution within the box is shifted to higher temperature with increase in the gate bias.

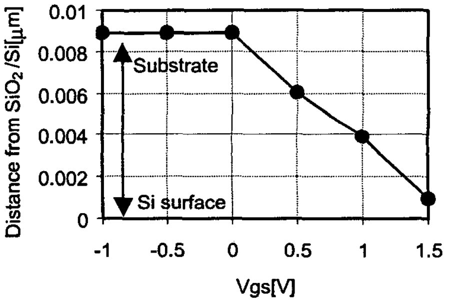

Figure 8. Simulation results showing the location of peak temperature with gate bias.

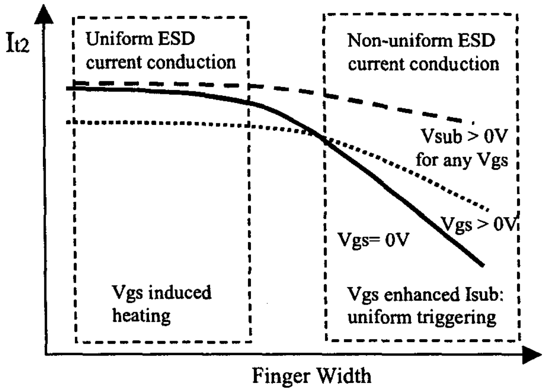

Figure 10. Design window for optimizing the performance of deep submicron ESD protection and output buffers.