Modelling and Analysis of Power Dissipation in Single Electron Logic

Santanu Mahapatra, Adrian M. Ionescu, Kaustav Banerjee* and Michel J. Declercq

Electronics Laboratory (LEG), Institute of Microelectronics and Microsystems (IMM),
Swiss Federal Institute of Technology Lausanne (EPFL), CH-1015 Lausanne, Switzerland
*Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA

Abstract

A new analytical model for Single Electron Transistors (SETs) that can be used for co-simulation with CMOS is developed and validated with Monte Carlo simulation. The model includes temperature dependence, device asymmetry and background charge effects. A detailed physical parameter extraction procedure for asymmetric SETs is reported. An analytical approach is subsequently developed to investigate and accurately predict the power dissipation of SET inverters. *Static* power, as main mechanism of SET logic power dissipation, and contributions of *dynamic* and temperature-dependent *leakage* power are derived and critically discussed. It is shown that SET asymmetry can be exploited to significantly reduce SET logic power dissipation with negligible impact on propagation delay.

Introduction

Historically, power scaling has been a key factor in IC evolution and, nowadays is still a major concern for nanometer scale CMOS. Various new evolutionary and revolutionary device architectures [1-3] have been recently proposed at nano-scale, with an increasing interest in Single Electron Transistors (SETs) as promising candidates for future *ultra-low power* ULSI [1]. This papers reports for the first time detailed investigations and calculations of power dissipation associated with Single Electron Logic, using a comprehensive physical SET model.

Development of New Analytical Model and Associated Parameter Extraction

An improved SET analytical model, with better compaction and physical formulation compared to our recent SET model (MIB) [4], is proposed. The new model includes the temperature dependence of the tunneling rates in drain and source tunneling currents (in contrast with [4], where an equivalent temperature-dependent leakage current is used), which is more physical. The drain current, I_{DS}, is calculated as *half of the harmonic mean* of drain and source tunneling components: $I_{DS}=I_D I_S/(I_D+I_S)$, where I_D and I_S are deduced with the computing subroutine, $\mathcal{F}(V_{GS}, V_{GS2}, V_{DS})$ reported in **Fig. 1**. The model also includes background charge effect (critical for SET logic) and can be used for both asymmetric and symmetric SETs, with one- or two-gate architectures. It is worth noting that all the model parameters are physical: i) drain and source tunneling capacitances, C_{TD} and C_{TS}; ii) capacitances of the first and second gate, C_G and C_{G2}, and iii) drain and source tunnel-junction resistances, R_D and R_S. The new model is able to describe both static and dynamic SET characteristics with high accuracy, as validated by comparison with Monte Carlo (MC) simulator SIMON [5]. The various plots depicted in **Fig. 2(a)** at different V_{DS} demonstrate the accuracy of the proposed model, which is further validated in terms of SET transconductance, g_m (= dI_{DS}/dV_{GS}), as shown in **Fig. 2(b)**. Also, for the first time, we report on the *subthreshold slope*, *S*, of SET as performance factor; using $log(I_{DS})$-V_{GS} characteristics **[Fig. 2(c)]** of realistic devices. **Figure 2(d)** reports the effect of temperature on S for two different SET technological nodes (island diameter: 18nm and 1.8nm) suggesting that SET can provide *S* values of 1-20mV/decade at low temperatures (<20K), significantly competitive with MOSFETs (with ideal limit of 60mV/decade at room temperature, which in practice, can reach about 20mV/decade near 10K, being limited by interface state capacitance behavior dependent on temperature [6]). However, caution should be paid to possible non-identified practical limitations of these values in fabricated SETs. In fact, any SET has two associated subthreshold slopes, $S_1>0$ and $S_2<0$, that reduce with the temperature and can be tuned by making SET *resistively asymmetrical* [**Fig. 2(c)**]. Our analytical model has the advantage that can be used to extract its parameters from real measured data. If I_{peak} is the peak current (at $V_{GS} = V_{peak}$), and V_m (or V_n) is the minimum positive value of V_{GS} at which SET starts to exhibit positive g_m [**Fig. 3(a)**], for a certain value of V_{DS}, then it follows:

$$V_{peak}=e/(2C_G)+(C_\Sigma/C_G)\{\sqrt{R_S}/(\sqrt{R_S}+\sqrt{R_D})-C_{TD}/C_\Sigma\}V_{DS}$$
$$\text{and } I_{peak}=V_{DS}/(\sqrt{R_S}+\sqrt{R_D})^2 \quad (1)$$

$$V_m=e/(2C_G)-(C_{TD}/C_G)V_{DS} \text{ or } V_n=e/(2C_G)-(C_{TS}/C_G)V_{SD} \quad (2)$$

Eq. (1) suggests that the plot of V_{peak} versus V_{DS} is a straight line [**Fig. 3(b)**], and the intercept with the vertical axis can be used to extract C_G. Again, Eq. (2) proposes that the plot of V_m versus V_{DS} is also a straight line [**Fig. 3(c)**], the slope of which can be used to extract C_{TD}. It should be noted that as V_m is sensitive to the temperature, T [**Fig. 3(a)**], the extractions should be conducted at low temperatures. Finally, if I_{DS}-V_{GS} characteristics are recorded with *exchanged* drain and source terminals, the slope of V_n versus V_{SD} plot [**Fig. 3(d)**] can be used to extract C_{TS}. With the device capacitances extracted, the SET resistances are evaluated from the slope of the V_{DS} versus V_{peak} plot and from the peak value of I_{DS}. This original yet simple extraction procedure has been extensively validated by a self-consistent procedure based on data provided by MC simulation.

Analysis of Power Dissipation of SET Inverters

In the following, we show *for the first time* how to take advantage of the proposed analytical SET model for the investigation of power dissipation of C-SET inverter, as basic logic cell. Typical static characteristics of C-SET inverter simulated with our model (and validated by SIMON) are shown in **Fig. 4(a) and (b)**: they validate that SET inverter gain, $G=dV_{out}/dV_{in}$, is pretty low and essentially mirrors the C_G/C_T ratio. However, it should be noted that the SET inverter gain is *weakly sensitive* to T and the transition points (defined similar to CMOS, at G = -1) are nearly independent of T [3], which is remarkably good news. The effect of background charge on inverter characteristics is presented in **Fig. 5(a) and (b)**: it is found that C-SET inverter is tolerant to background charge up to around $0.1e$. The detailed analysis of the inverter static currents, I_{static}, is depicted in **Fig. 6** at $T = 0K$. From

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this figure, it can be seen that when the inverter is in Zone 1 or 4 (i.e., output is either logic *High* or *Low*) both transistors are *ON*, which is in total contrast with CMOS inverter, and therefore there is a static current path, I_{static}, from V_{DD} to V_{SS}, which leads to static power dissipation (similar to short circuit power of CMOS). However, when the inverter is in logic-transition region (Zone 2 and 3) one of the SETs is always *OFF* (Coulomb Blockade) and that leads to zero static current (again contrary to CMOS). When the output, V_{out}, of SET inverter is in logic *High* (Zone 1), then at T = 0K and for a *symmetric* SET, the following analytical formulation holds:

$$V_{out}^3 + A_2 V_{out}^2 + A_1 V_{out} + A_0 = 0 \quad (3)$$

where $A_0 = \{4C_G V_{DD}(e + 2C_G V_{in})V_{DD}\}/\{8C_T (C_G + C_T)\}$, $A_1 = -\{8 (C_T^2 + C_T C_G + C_G^2) V_{DD}^2 + 2e^2 + 8C_G V_{in} (e + C_G V_{in})\}/\{8C_T (C_G+C_T)\}$ and $A_2 = \{4C_G (2C_G V_{in} + e)\}/\{8C_T (C_G + C_T)\}$. For simplicity, assuming $V_{out}^3 << (A_2 V_{out}^2 + A_1 V_{out} + A_0)$, which corresponds to many practical cases, we have approximated Eq. (3) with a 2nd order expression. **Figs. 7(a) and (b)** show that such approximation could be acceptable for quick hand calculation of ouput voltage V_{out} and corresponding static power dissipation of SET inverter. It follows that the static power dissipation (P_{static}) of the SET inverter can be analytically calculated as:

$$P_{static} = I_{static}(V_{DD} - V_{SS}) = [\{2C_G V_{in} - 2C_T V_{DD} - 2(C_G + C_T)V_{out} + e\}\{2C_G V_{in} + 2(C_T + C_G)V_{DD} + 2C_T V_{out} + e\}/\{4C_\Sigma^2(-V_{DD} - V_{out})R_S\}](V_{DD} - V_{SS}) \quad (4)$$

Fig. 7(b) shows the static power dissipation of SET inverter using Eq. (4) with V_{out} calculated numerically from Eq. (3) and analytically from 2nd order approximation. It should be noted that, as the inverter characteristics is symmetrical against the V_{in} = 0 axis, therefore the power dissipation in Zone 4 will be similar to that in Zone 1, which results in P_{static} of the order of 90pW at $|V_{in}|$~10mV. It is also found that P_{static} is a weak function of T because the SET inverter characteristics do not change significantly in Zones 1 and 4 with T. With the dynamic power dissipation of SET inverter described by: $P_{dynamic} = (E_{H\to L} + E_{L\to H})f$, where $E_{H\to L}$ and $E_{L\to H}$ are energy dissipation when output switches from high to low and low to high respectively (which is actually the difference between energy taken from the power supply and the energy stored in the load capacitor) and given by:

$$E_{H\to L} = -V_{SS}\int_0^{3\tau} i_{bottom}\,dt - \frac{1}{2}C_L V_{out}^2\Big|_{t=3\tau}$$

$$\text{and } E_{L\to H} = V_{DD}\int_0^{3\tau} i_{top}\,dt - \frac{1}{2}C_L V_{out}^2\Big|_{t=3\tau} \quad (5)$$

where, f is the operating frequency and τ is the inverter time constant. **Fig. 8** depicts the $P_{dynamic}$ and $P_{dynamic}/P_{static}$ ratio for a SET inverter as a function of frequency. An original finding is that *static power dissipation* (that appears to dominate SET operation) *can be significantly reduced by making the SET resistively asymmetric*: i.e., instead of making $R_S = R_D = R_T$ with designed $R_D = 4R_T/(1+\sqrt{x})^2$ and $R_S = xR_D$, where $x > 1$, the static power dissipation can be reduced by tens of % (by reducing I_{static}, **Fig.6**) while *dynamic power dissipation and propagation delay are almost unaffected* (**Fig. 8**). On the other hand, when *background charge* changes (however in a limited manner, preserving inverter functionality in near the same voltage window), I_{static} increases in Zone 1 (or Zone 4) and, simultaneously, decreases by the same amount in Zone 4 (or Zone 1). Hence, it can be concluded tha *background charge effect is almost negligible on power dissipation.* In addition to the static and dynamic power dissipation there is another specific source of power dissipation in SET logic circuits: the *temperature induced (leakage current dependent) leakage power dissipation* ($P_{leakage}$). At higher temperatures, in Zone 2 and 3, both the SETs conduct current instead of being in OFF state, which offers a temperature induced current path between V_{DD} to V_{SS}. As seen from **Fig. 9**, in the logic transition region, the V_{DD}-to-V_{SS} current is highly dependent on temperature and this temperature-induced leakage current gives rise to leakage power dissipation mainly during logic level transition. It is found that $P_{leakage}$ is also a function of the rise time of the input signal. We demonstrate that, for realistic parameters of SET, the contribution of $P_{leakage}$ can be up to about 10% of P_{static}. Finally, it should be noted that, compared to nanometer scale CMOS inverters where leakage power is dominant [7], static power (as defined above) is expected to dominate SET logic operation, and its order of magnitude is around 100 pW per gate (which is about 4-5 decades lower than that of CMOS), being quasi-independent of temperature. However, caution should be paid to the fact that this apparently outstanding power reduction with SET logic gate does not reduce the *power density* commensurately. This is mainly due to SET dimensions (in the range of few nm, compared to 50 nm SOI CMOS [1]), which only reduces the power density by a factor of 10-100 (in the best case). Hence, accurate estimations of SET based logic power density and its dependence on device parameters is necessary for realistic comparisons with CMOS based logic.

Conclusion

Analytical models have been formulated to investigate and predict the I-V characteristics of Single Electron Transistors and the power dissipation of SET inverters. The static power (of the order of 100pW/inverter) is identified as the main mechanism of SET logic power dissipation and found to be weakly dependent on the operation temperature. Contributions of other power components, such as dynamic and temperature-dependent leakage power, are also critically discussed. New design solutions at device level, such as asymmetric SET architectures, are proposed and demonstrated to reduce SET inverter static power dissipation, without significant impact on their dynamic performances.

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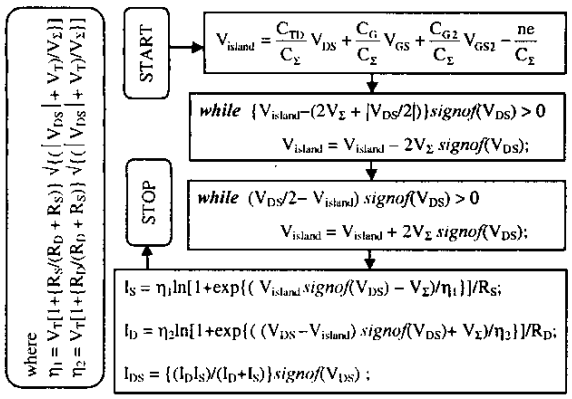
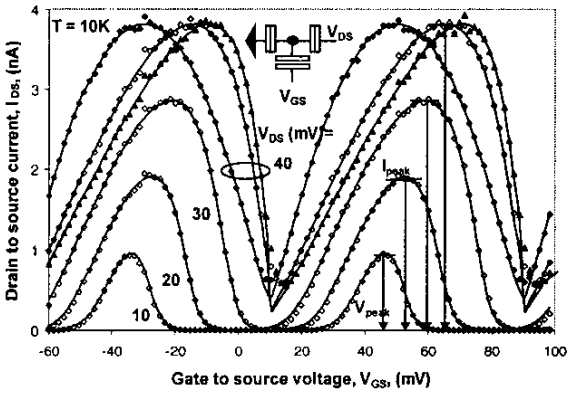
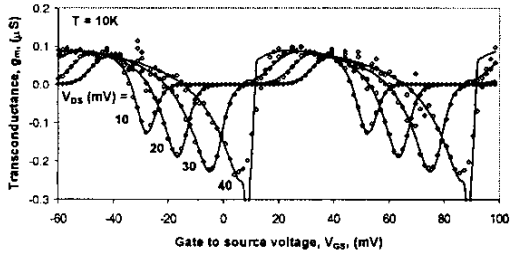


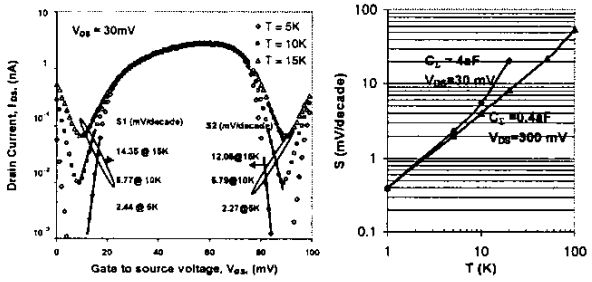
Fig.1 Simplified flowchart of the computing subroutine, $\mathscr{F}$, for SET drain current I_{DS}. Here V_T is the thermal voltage, e is the elementary charge, $V_\Sigma = e/(2C_\Sigma)$ and $C_\Sigma = C_{TD} + C_{TS} + C_G + C_{G2}$. The *signof*($V_{DS}$) function holds the sign of V_{DS} and *ne* is the background charge.



(2a)



(2b)



(2c) (2d)

Fig.2 Validation of new MIB model (solid line) for asymmetric SET device (C_G = 2aF, C_{TD} = 1.5aF, C_{TS} = 0.5aF, R_D = 1MΩ and R_S = 5MΩ) with widely accepted MC simulator SIMON (symbol). (a) I_{DS}-V_{GS} characteristics, where: "▲" R_D = 0.6MΩ and R_S = 6MΩ, "♦": R_D = R_S = 2.6MΩ (b) g_m-V_{GS} characteristics derived by numerical derivation of Fig.(a) for R_D: R_S =1:5; (c) subthreshold slope (S) calculation for R_D = 1MΩ and R_S = 5MΩ and (d) S as a function of T for different technology.

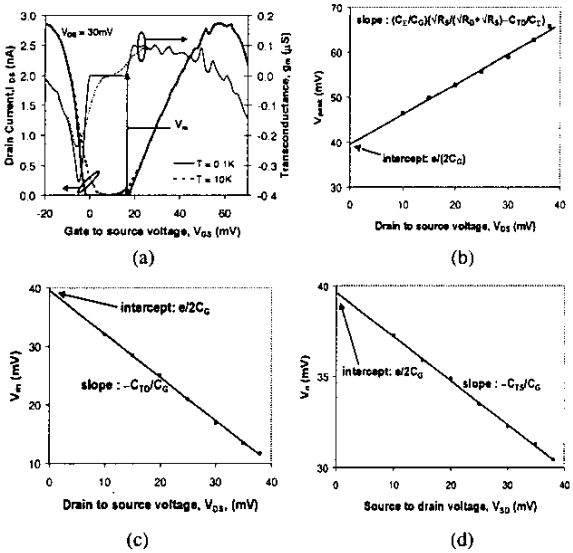


Fig. 3 Parameter extraction procedure by self-consistent method [4] using the characteristics given in Fig.2.

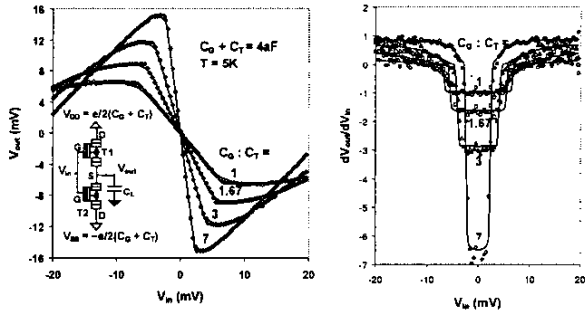


Fig. 4 (a) SET-inverter static characteristics for different values of C_G/C_T (solid line = MIB and symbol = SIMON). T1 and T2 are identical with R_D = R_S = 1MΩ, C_T = C_{TD} = C_{TS} and load capacitance C_L = 1fF (b) corresponding gain characteristics.

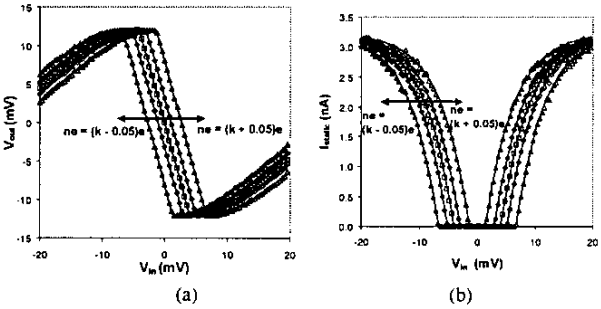


Fig.5 Effect of background charge on inverter characteristics for the C_G:C_T =3 at T = 0K, where the background charge is ne=(k-α)e, where k is an integer and α is a fraction.

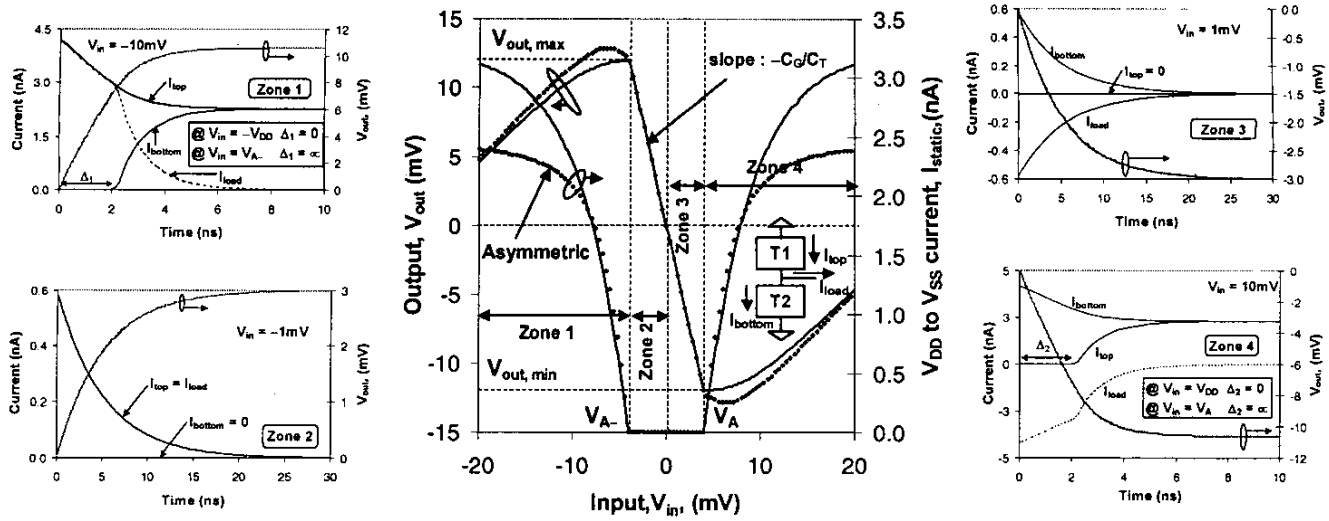
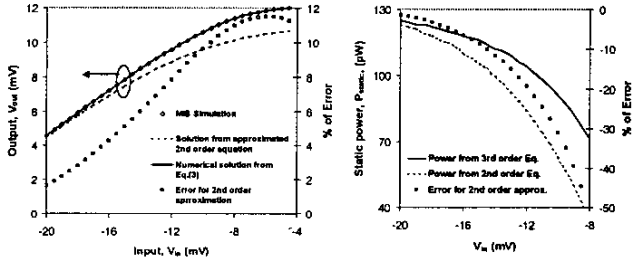
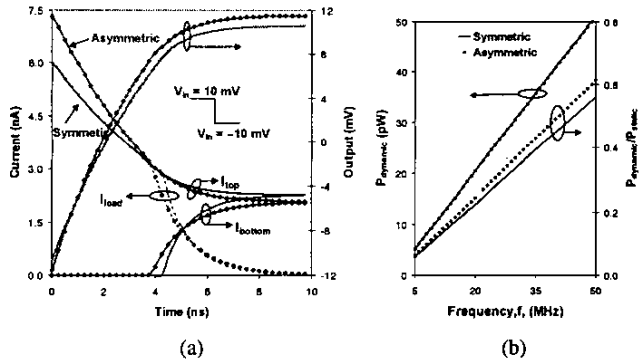


Fig. 6 SET inverter characteristics at T=0K predicted by MIB with the device parameters of Fig.5. It should be noted that Zone1 and Zone 4 represents the regimes where the output of the inverter is logic HIGH and LOW respectively. Here $V_{out,max} = |V_{out,min}| = (C_G/C_\Sigma)V_{DD}$ and at $|V_{in}| = |V_{A-}| = V_A = (C_T/C_\Sigma)V_{DD}$, $dV_{out}/dV_{in} = -1$. Now, when the inverter is in Zone1 or 4, at steady state, both T1 and T2 are ON and therefore offer a static current I_{static} from V_{DD} to V_{SS}. It should be noted that, in Zone 1 & 4, Δ is the "waiting time", i.e, when one SET is conducting but the other is OFF. However, in the transition regime (Zone 2 and 3) one SET is always OFF (i.e., Δ is infinity) and at the steady state both T1 and T2 are in OFF state, which results in $I_{static} = 0$. The characteristics with symbols in the central figure represents a resistively asymmetric inverter with $R_S = 1.5M\Omega$ and $R_D = 0.6\ M\Omega$.



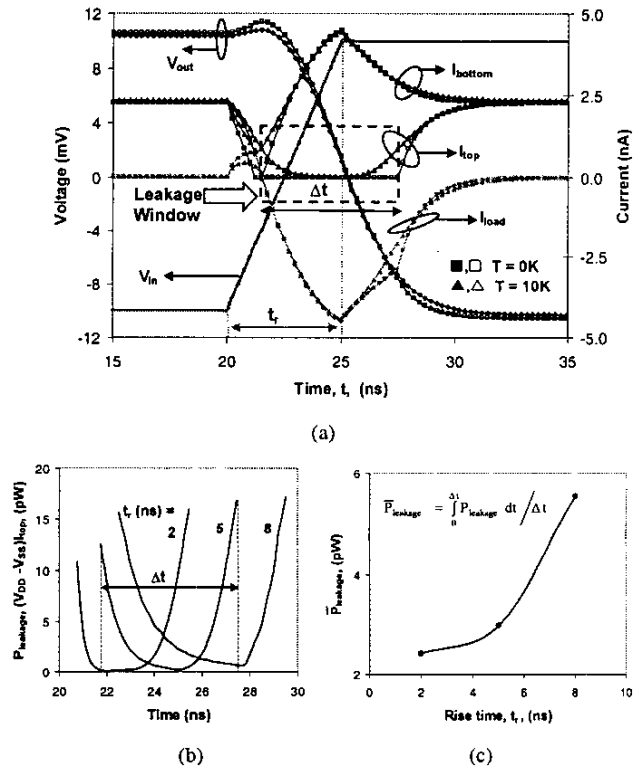
(a) (b)

Fig.7 (a) Static output voltage versus input voltage of SET inverter (Zone 1, for the same parameters as Fig.5 and (b) corresponding static power calculated with the proposed models, at T = 0K.



(a) (b)

Fig. 8 Dynamic power dissipation for SET inverter predicted by MIB simulation with the same device parameters of Fig.5. It is assumed that the input signal is switching between ±10 mV. Fig. 8(a) shows the transient response for symmetric and asymmetric SET when input is changing from *High* to *Low*. Fig.8(b) demonstrates the effect of device asymmetry (R_S = 1.5MΩ, R_D = 0.6MΩ), denoted by dotted line, on the power dissipation.



(a) (b) (c)

Fig. 9. Effect of T on $P_{leakage}$. Fig.(a) shows how I_{top} changes with temperature and offers a nonzero V_{DD} to V_{SS} current in the logic transition regime that leads to the T dependant $P_{leakage}$. Fig.(b): an estimation of $P_{leakage}$ in the 'Leakage Window' for different value of rise time (t_r) at a temperature of 10K. Fig.(c): the average value of $P_{leakage}$ for different t_r.