# Via Design and Scaling Strategy for Nanometer Scale Interconnect Technologies

Sungjun Im, Kaustav Banerjee*, and Kenneth E. Goodson**

Department of Materials Science and Engineering, Stanford University, Stanford, CA 94305, USA
*Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA
**Department of Mechanical Engineering, Stanford University, Stanford, CA 94305, USA
Phone: (650) 736-0044, Fax: (650) 723-7657, E-mail: sjim@stanford.edu

**Abstract**

Via design and scaling is a critical issue for all nanometer scale interconnect technologies. This paper presents a comprehensive investigation into the robustness and accuracy of ITRS [1] specified design guidelines for vias in nanometer scale technologies. Using rigorous thermal Finite Element simulations of 3-D via/line structures embedded in a chip, and material/geometrical data based on the ITRS, it is shown that design of vias based on ITRS specified maximum allowable currents for various technology nodes can severely compromise their reliability by underestimating chip-level thermal effects and current flow continuity in pitch matched vias, especially at the local interconnect tier. A more robust via design optimization strategy is proposed which will be useful to process designers.

**Introduction**

In advanced ULSI interconnect systems, via design and scaling rules are critical for the robustness and reliable operation of the IC component. Via design also has strong impact on the required wiring area and on the routability of neighborhood wires due to the via blockage effect. Additionally, interconnect scaling trend has yielded increasing current densities and associated thermal effects [2, 3]. Furthermore, low dielectric constant (low-$\kappa$) materials are being introduced as alternative insulators to silicon dioxide to reduce interconnect delay and cross-talk noise to enhance circuit performance. These materials can exacerbate thermal effects owing to their low thermal conductivity (Fig. 1). Also, the increased metal resistivity due to electron surface scattering [4] and finite barrier layer thickness is an emerging concern as wire sizes scale down, which will further aggravate thermal problems due to increased interconnect Joule heating. Hence, it is important to carefully consider various effects including via resistance, via self-heating that determines effective via temperature, and electromigration (EM) reliability, while formulating via design rules for nanometer scale interconnect technologies.

**Via Current-Density Scaling**

The most recent edition (2001) of the ITRS provides a *single* maximum allowable current value through the vias assuming a chip temperature of 105 $^0$C at various technology nodes (Fig. 2). Also, it does not provide any quantitative justification and, as a result, the proposed numbers seem somewhat speculative. Additionally, for high-performance technologies local vias are mostly pitch matched, and hence the currents flowing through the local wires and vias must be identical. Hence, continuity of current flow must be taken into account, especially for the local wires and vias. It has been recently reported that local vias can be a reliability concern even for signal nets where the currents are bipolar [5]. In this study we have performed a rigorous analysis that takes various effects outlined above into consideration for robust via design and scaling methodology for power and ground lines, which effectively carry dc currents.

Since the interconnect temperature rise is directly affected by the chip junction temperature, accurate scaling analysis must reflect junction temperature variations. The junction temperatures at each node are estimated by using one-dimensional heat flow equation (Fourier's law), the maximum power dissipation as per ITRS, and a package thermal resistance of (0.5 K/W) based on present technology (150 nm) (Fig. 3). The ITRS provides the requirement of the maximum current ($I_{max}$) for vias and the maximum current density ($J_{max}$) for wires without specifying their tiers (Fig. 2). Therefore, the $I_{max}$ values for local, semi-global, and global tier wires can be significantly different from the $I_{max}$ values for vias if they are calculated from ITRS proposed $J_{max}$ values and wire cross sections corresponding to each tier (Fig. 4). Furthermore, if the current continuity for pitch matched vias is taken into account, it follows that the $I_{max}$ value for the vias should be determined by the $I_{max}$ value in the adjoining wires. This is especially true for local tier vias [5]. As technology scales down, the calculated $I_{max}$ values decrease independent of tiers. This is due to the fact that the decrease in wire size is larger than the increase in $J_{max}$. It is shown that the $I_{max}$ values, even for local wires, are 12 – 47 % larger than that for the vias given by ITRS. In this work, four different $I_{max}$ values shown in Fig. 4 were used as current stress inputs for the purpose of evaluating ITRS proposed $I_{max}$ values for vias and for providing via design guidelines.

**Methodology**

The three-dimensional Finite Element (FE) electro-thermal simulation tool (ANSYS), has been employed to account for Joule heating of complex interconnect and via

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structures. The simulations at various technology nodes were based on parameters (Table 1), which have been determined from the ITRS data. The effective resistivity incorporating the interface scattering and barrier layer effects is used along with the reduced thermal coefficient of resistivity ($\alpha$) due to the scattering effect [5]. The orthogonal interconnect arrays at the local tier (*M1* and *M2*) and vias connecting *M1* and *M2* are considered in this analysis (Fig. 5). The widths of *M1* and *M2* ($W_1$ and $W_2$) are assumed to be the same for a given technology node. The via separation (from their centers) and via area are assumed to be $4\times W_1$ and $W_1\times W_1$ respectively. The FE simulation encompasses thermal coupling between adjacent wires, non-uniform Joule heating due to current crowding, and the temperature dependent metal resistivity, $\rho(T)$. Assuming a periodic array of vias with a constant separation, temperature fields are obtained for the unit cell defined by symmetry (Fig. 6). It can be observed that the temperature fields in the vias attain around 197 $^0$C for the 45 nm technology node shown in this example.

## Results and Discussion

Figure 7 plots the simulation results of the average temperature of a via connecting *M1* and *M2* subject to four different $I_{max}$ values calculated in Fig. 4. For the three cases where small $I_{max}$ values are used, the via temperature is mostly governed by the chip junction temperature, and the temperature rise with respect to the junction temperature is less than 5 $^0$C. However, if a local via is forced to carry the same $I_{max}$ as global wires (possible for pitch matched local vias, especially in stacked via structures), the via temperature rise can reach up to 56.5 $^0$C. Based on these via temperatures and Black's equation for dc currents, self-consistent current densities (which comprehend both EM and interconnect Joule heating) are calculated, which satisfy the same time-to-failure (TTF) for the ITRS reference temperature (105 $^0$C) and ITRS specified via current density (= ITRS $I_{max}$ / via cross sectional area). The via current density can be modified by changing either via cross sectional areas or $I_{max}$ values flowing into the via. Since current scaling is difficult due to circuit performance requirement, via area scaling is explored first. In order to meet the thermal reliability constraints, the area of the via at the local tier should be much larger than the areas of minimum sized vias at the local tier as per the ITRS (Fig. 8). If the ITRS specified $I_{max}$ (via) values are used, the via area at the local tier should be 1.1 – 4.1 times larger than the ITRS specified minimum via size depending on the technology node. If the local vias carry the same $I_{max}$ as global wires, 8.5 – 48.7 times larger local via areas are required. An alternative via design strategy is to increase the number of local vias using the ITRS specified minimum via size. Figure 9 plots the number of ITRS specified minimum sized local vias required to satisfy the same EM reliability criterion as allowed for the single pitch matched vias in Fig. 8. It is shown that the required number of vias can increase up to 5 for the 22 nm node even if ITRS specified $I_{max}$ values are used, due to via Joule heating and scattering effects discussed earlier.

The requirement of decreased via current density can also be achieved by reducing $I_{max}$ values. Figure 10 compares the $I_{max}$ values for the via based on ITRS and this analysis, which shows that the percent decrease in allowable $I_{max}$ with respect to the $I_{max}$ from ITRS continues to increase from 9.8 % to 75.8 %. The $J_{max}$ values for wires proposed by the ITRS and from this analysis are evaluated in Fig. 11. The $J_{max}$ values based on this analysis for each tier are obtained by dividing the modified self-consistent $I_{max}$ values by the wire cross section at that tier assuming fixed local via dimensions and current flow continuity. It can be observed that the $J_{max}$ values provided by ITRS are too conservative for the local and semi-global wires, and too aggressive for the global wires. Furthermore, Fig. 12 illustrates that lower effective junction-to-ambient thermal resistance, $\theta_J$, will be required to safely use ITRS proposed $I_{max}$ (via) at 105 $^0$C and via dimensions without violating self-consistent EM reliability criterion. Therefore, innovative chip cooling solutions can be exploited for providing more flexible via designs. Finally, the design space illustrated in Figs. 8 – 10 can be used for designing and scaling vias in nanometer scale interconnect technologies.

## Conclusions

Using rigorous thermal Finite Element simulations of 3-D via/line structures embedded in a chip and self-consistent electromigration analysis, it is shown that design of vias based on the ITRS specified via size and maximum allowable currents can severely compromise their reliability. It is recommended that various nanometer-scale and thermal effects in pitch matched local vias be taken into account for robust via design.

## References


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[3] K. Banerjee et al., *Design Automation Conference*, 1999, pp. 885-891.
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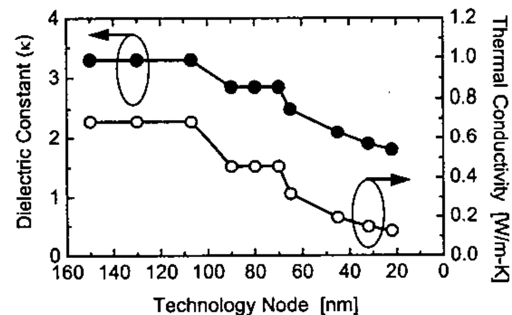


**Fig. 1.** Effective dielectric constant ($\kappa$) and thermal conductivity ($K$) of inter-layer dielectric (ILD) materials as a function of technology node.

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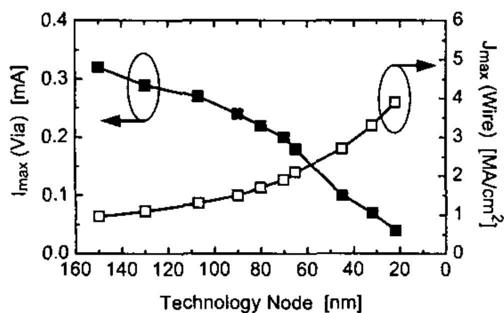


**Fig. 2.** ITRS proposed $I_{max}$ for all vias and $J_{max}$ for all wires at 105 °C.

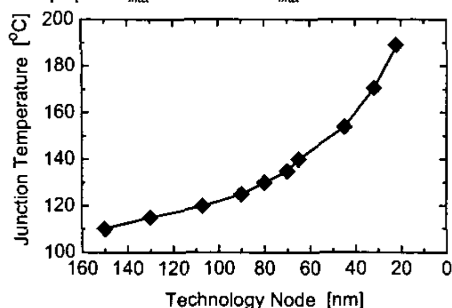


**Fig. 3.** Chip junction temperature ($T_J$) variations calculated from the maximum chip power ($P_{max}$) and ambient temperature ($T_{amb}$= 45 °C) based on ITRS. The effective junction-to-ambient package thermal resistance ($\theta_J$=0.5 K/W) is calculated for the current technology node (150 nm) using $\Delta T=T_J-T_{amb}=P_{max}\times\theta_J$, and used for other technology nodes. $T_J$=110 °C is assumed for 150 nm node.

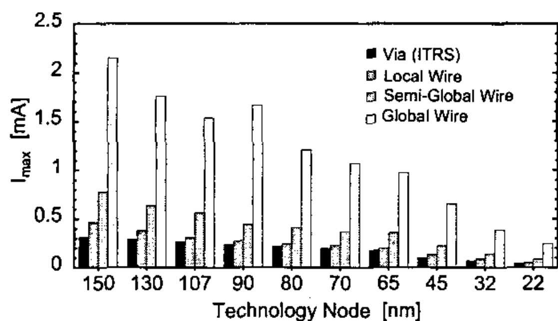


**Fig. 4.** The $I_{max}$ values for local, semi-global and global wires calculated from $J_{max}$ values and metal cross-sectional areas at each tier based on ITRS. These values are compared to the ITRS proposed $I_{max}$ values for vias.

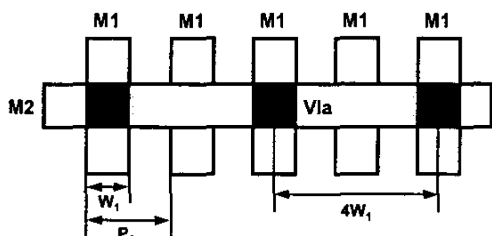


**Fig. 5.** Schematic of local wires (*M1* and *M2*) and vias. It is assumed that interconnect pitch, $P_1=2\times W_1$. Note that only one of the *M2* lines is shown here for simplicity. Contacts to the substrate are ignored in this analysis.

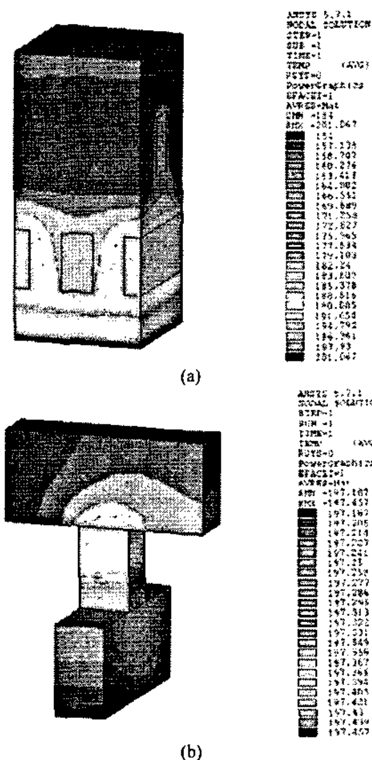


**Fig. 6.** Temperature contour plots from FE simulations at 45 nm node. (a) Local wires (*M1* and *M2*) embedded in a dielectric medium ($K_{ILD}$=0.2 W/m-K) where a via connecting *M1* and *M2* is hidden. (b) A via connecting *M1* and *M2* where current flows from the left of *M2* to the back of *M1*. Note that the color scale is different from (a). All simulation parameters are based on ITRS, and $I_{max}$ value for global wires (0.65 mA) is applied to all wires in this case as a worst-case simulation.

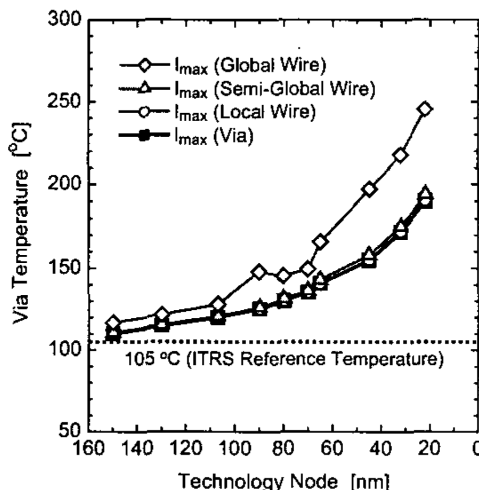


**Fig. 7.** Average temperature of local vias connecting *M1* and *M2* as a function of technology node with varying $I_{max}$. The reference temperature (105 °C) where ITRS estimates $I_{max}$ for all vias and $J_{max}$ for all wires is also indicated.

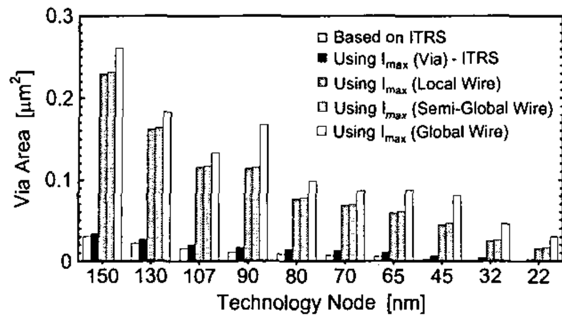


**Fig. 8.** Required local via areas to satisfy the self-consistent EM reliability criterion for various $I_{max}$ values.

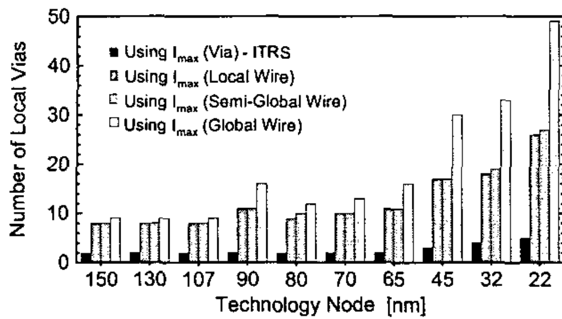


**Fig. 9.** Required number of local vias to satisfy the self-consistent EM reliability criterion for various $I_{max}$ values.

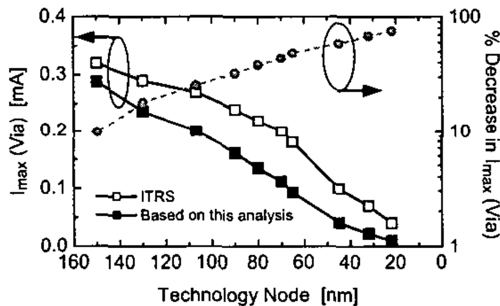


**Fig. 10.** EM reliability and Joule heating aware $I_{max}$ values for vias with fixed local via dimensions. The percentage decrease in $I_{max}$ with respect to the ITRS values is also plotted.

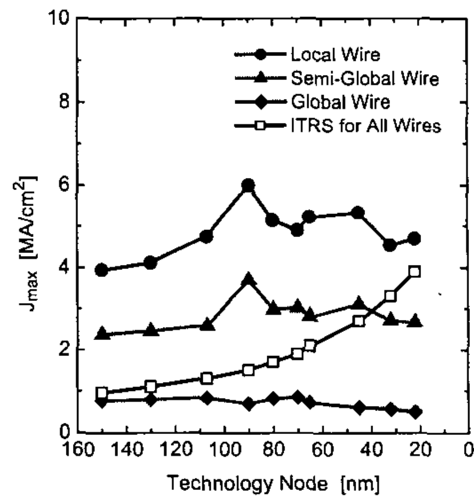


**Fig. 11.** EM reliability and Joule heating aware $J_{max}$ values for local, semi-global, and global wires assuming fixed local via dimensions and current flow continuity, which are compared to the single $J_{max}$ value from ITRS.

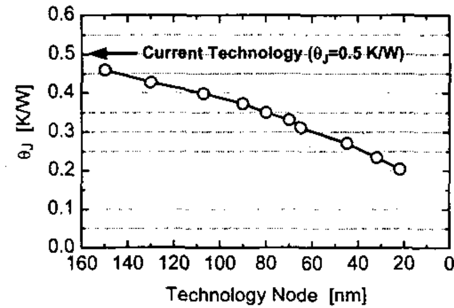


**Fig. 12.** The effective junction-to-ambient thermal resistance, $\theta_J$, required to safely use ITRS proposed $I_{max}$ (via) and via dimensions without violating self-consistent EM reliability criteria. According to ITRS, the ambient temperature is 45 °C for all technology nodes.

**Table I.** ITRS based interconnect parameters and material properties used in this study. The ratios of $\rho / \rho_o$ (thin-film) and $\alpha / \alpha_o$ are calculated by using [5], and the ratio of $\rho / \rho_o$ (barrier) is calculated by assuming conformal barrier layer. The ratio of $\rho / \rho_o$ (effective) is then obtained by multiplying [$\rho / \rho_o$ (thin-film)] by [$\rho / \rho_o$ (barrier)]. $\rho_o$=2.7×10$^{-6}$ Ω-cm and $\alpha_o$=6.8×10$^{-3}$ /K at $T_{ref}$=120 °C are used for calculating $\rho(T)$, and $Q$=0.5 eV is used for EM TTF calculations.

| Tech. Node [nm] | Maximum Power [W] | Wire Width (Local Tier) [nm] | Wire Height (Local Tier) [nm] | Wire Aspect Ratio (Local Tier) | Barrier Thickness [nm] | $\rho / \rho_o$ (thin-film) | $\rho / \rho_o$ (barrier) | $\rho / \rho_o$ (effective) | $\alpha / \alpha_o$ | $\kappa$ | $K_{ILD}$ [W/m-K] | $I_{max}$ – via (at 105 °C) [mA] | $J_{max}$ – wire (at 105 °C) [MA/cm²] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 150 | 130 | 175 | 280 | 1.6 | 16 | 1.0502 | 1.2979 | 1.3630 | 0.9501 | 3.3 | 0.69 | 0.32 | 0.96 |
| 130 | 140 | 147.5 | 236 | 1.6 | 14 | 1.0600 | 1.3121 | 1.3909 | 0.9407 | 3.3 | 0.69 | 0.29 | 1.1 |
| 107 | 150 | 122.5 | 196 | 1.6 | 12 | 1.0729 | 1.3248 | 1.4213 | 0.9287 | 3.3 | 0.69 | 0.27 | 1.3 |
| 90 | 160 | 105 | 178.5 | 1.7 | 10 | 1.0857 | 1.3086 | 1.4207 | 0.9172 | 2.85 | 0.46 | 0.24 | 1.5 |
| 80 | 170 | 92.5 | 157.25 | 1.7 | 9 | 1.0979 | 1.3170 | 1.4459 | 0.9067 | 2.85 | 0.46 | 0.22 | 1.7 |
| 70 | 180 | 85 | 144.5 | 1.7 | 8 | 1.1069 | 1.3041 | 1.4435 | 0.8991 | 2.85 | 0.46 | 0.20 | 1.9 |
| 65 | 190 | 75 | 127.5 | 1.7 | 7 | 1.1218 | 1.3009 | 1.4594 | 0.8871 | 2.5 | 0.32 | 0.18 | 2.1 |
| 45 | 218 | 52.5 | 94.5 | 1.8 | 5 | 1.1759 | 1.3043 | 1.5337 | 0.8476 | 2.1 | 0.20 | 0.10 | 2.7 |
| 32 | 251 | 37.5 | 71.25 | 1.9 | 3.5 | 1.2467 | 1.2930 | 1.6121 | 0.8037 | 1.9 | 0.15 | 0.07 | 3.3 |
| 22 | 288 | 25 | 50 | 2.0 | 2.5 | 1.3662 | 1.3158 | 1.7976 | 0.7439 | 1.8 | 0.13 | 0.04 | 3.9 |