Effect of Via Separation and Low-k Dielectric Materials on the Thermal Characteristics of Cu Interconnects

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ABSTRACT

This paper reports the impact of vias on the spatial distribution of temperature rise in metal lines and shows that the temperature is highly dependent on the via separation. A 3-D electro-thermal simulation methodology using a short-pulse stress is presented to evaluate interconnect design options from a thermal point of view. The simulation methodology has also been applied to quantify the use of *dummy thermal* vias as additional heat sinking paths to alleviate the temperature rise in the metal wires for the first time. Finally, the impact of metal wire aspect ratio and low-k dielectrics on interconnect thermal characteristics is discussed.

INTRODUCTION

In advanced ULSI technology, a variety of novel insulating materials, including organic and inorganic films, as well as the use of porosity and air-gaps, have been introduced to reduce the RC delay, dynamic power consumption and crosstalk noise [1-5]. However, these dielectrics invariably have poor thermal properties that can cause substantial interconnect temperature rise [6]. The increasing thermal challenge in ULSI interconnects will play an important role in advanced technology nodes and hence require urgent attention. Not only will thermal effects be a major reliability concern, but also the increase of resistivity with temperature can degrade the speed performance expected at these technology nodes. Recent publications have addressed the issue of poor thermal conductivity of low-k dielectrics and their impact on interconnect reliability and performance [7, 8]. Furthermore, self-heating in via structures has been measured and modeled [9]. However, the effect of these vias, which have much higher thermal conductivity than the dielectrics, on the thermal characteristics of the metal wires has not been investigated thoroughly. Additionally, the thermal advantage gained by using dummy thermal vias in advanced Cu/low-k interconnect structures has not been quantified. These dummy vias can effectively lower the temperature rise in low-k based interconnect structures by providing lower thermal resistance paths. In this paper, the impact of via separation on the temperature rise in deep submicron interconnect lines with different low-k dielectrics has been analyzed in detail using a 3-D RC transmission line simulation methodology.

3-D ELECTRO-THERMAL SIMULATION METHODOLOGY

In order to provide robust thermal design guidelines for deep submicron Cu/low-k interconnects, it is very desirable to have a simple simulation methodology to estimate the temperature profiles in the metal wires and evaluate the impact of via separation. Based on the thermal-electrical analogy (Fig. 1), a 3-D RC thermal circuit model has been developed, as shown in Fig. 2. To account for the temperature dependence of the metal resistivity, the heat generation (q) in each piece of the wire has been modeled as a voltage (temperature) controlled current source ($q=J^2\rho(T)$). RC transmission lines are used to model the heat diffusion due to the similarity of the governing equations as illustrated in Fig. 1. HSPICE was used for 3-D simulations of the distributed thermal RC circuits. This technique was first validated by comparing with experimental data from [10] as shown in Fig. 4. All the work presented here after is based on simulation results for Cu interconnects for the 0.1-μm technology node, adopted from [7], which are based on the National Technology Roadmap for Semiconductors (NTRS '97) [11].

In this work, electro-thermal simulations under high-current short-pulse stress conditions are used to account for worst case thermal scenarios. Since a high-current short-pulse ($J > 10\text{MA/cm}^2$, and $t_{pulse} < 200$ ns) usually causes much higher ΔT_{max} due to more severe self-heating than under normal operating conditions and the heat diffusion is limited to the immediate materials in contact with the metal line [10], this condition will define the most stringent via separation requirement for lowering the temperature of the metal wires. It should be noted that the simulation methodology developed here is quite general, and can be easily extended to study steady-state stress conditions by using longer pulses.

THERMAL SIMULATION RESULTS

AlCu vs Cu Interconnects

As shown in Fig. 5, for the same cross section, current density, and surrounding dielectric, Cu wires would experience lower ΔT_{max} than Al wires, due to their higher thermal conductivity and thermal capacity, and most importantly, due to their lower resistivity. This along with higher melting point (~1100 ^{0}C) than that of AlCu (~660 ^{0}C) would provide more thermal margin to Cu interconnects. However, ΔT_{max} can still be prohibitively high when metal dimensions are scaled down and low-k dielectrics are incorporated. Therefore, it is prudent to study the effect of vias on the thermal characteristics of Cu wires to make use of them in deep submicron designs.

Impact of Via Separation and Low-k Dielectrics

Fig. 6 compares the normalized spatial temperature distribution along an interconnect line with a via separation of 100 μm, subjected to transient current pulses of 200 ns and 2 μs duration. It can be observed that the temperature rise profile for the 2 μs pulse is more gradual due to the increased influence of vias for longer diffusion time, which results in longer diffusion lengths. The heat diffusion length, $L_D = (\alpha t)^{1/2}$, where α is the thermal diffusivity of the interconnect materials, are 5 μm and

16 μm for the 200 ns and 2 μs pulse duration respectively. Fig. 7 plots the temperature decay after a 200 ns pulse. It can be observed that the temperature decays more rapidly with vias placed closer. This shortens the high temperature span that the interconnect would experience and thus reduces thermal problems. ΔT_{max} vs. via separation for different dielectrics is shown for high current pulse duration of 200 ns in Fig. 8 and 100 ns in Fig. 9. ΔT_{max} is higher for the 2 μs pulse due to higher pulse energy, which results in greater Joule heating. However, both Fig. 8 and Fig. 9 indicate that ΔT_{max} would be reduced dramatically for smaller via separation. For larger via separation ΔT_{max} saturates since the effect of vias diminishes. This is dictated by thermal diffusion length (L_D), which can be interpreted as the distance over which heat generated in the wire flows through the via. The heat generated beyond L_D diffuses through the dielectric. It can also be observed in Fig. 9 that for shorter pulse duration the differences between ΔT_{max} for various dielectrics is much smaller. This is due to the fact that heat does not have sufficient time to diffuse through the surrounding dielectric. Additionally

ΔT_{max} vs. current density for different dielectrics is shown for global (Fig. 10) and local interconnects (Fig. 11). It can be observed that while the temperature rises sharply and low-k dielectrics show worse situation for a typical global line with via separation of 100 μm, the temperature rise is significantly alleviated for local interconnects due to a smaller via separation of 1 μm. Even if air is used as both the ILD and the IMD dielectric (worst case thermal scenario), no significantly higher ΔT_{max} is observed for the local interconnects. This observation is further validated in Fig. 12, which shows that the spatial temperature distributions for various dielectrics are similar and ΔT_{max} is nearly independent of the dielectric material. This suggests that they are all within L_D and via effect dominates the thermal characteristics.

Impact of Dummy Thermal Vias

Dummy thermal vias, which conduct heat but are electrically isolated, can be installed in Cu/low-k structure to lower the temperature rise. The advantage of the dummy via effect can be demonstrated by using the lowest-k dielectric, air, in ULSI interconnect structure despite its poor thermal properties. In the case of global interconnect, Fig. 13 shows that thermal vias would be required approximately every 20 μm in Cu/air and every 30 μm in Cu/polymer interconnect structures to match the temperature rise of Cu/SiO_2. For the purpose of comparison, under normal steady state operating condition with the J_{max} specified in the SIA roadmap, the thermal via separation can be much more relaxed based on a simple analytical evaluation. The temperature profiles for Cu/SiO_2 with via separation of 100 μm, and for Cu/air with via separation of 20 μm, experiencing the same ΔT_{max} under a 200 ns pulse are shown in Fig. 14. It can be observed that the temperature rise along the Cu/air wire varies spatially and that the average temperature is much lower than that of Cu/SiO_2 wire, resulting in reduced thermal problems and may relax the requirement of thermal via separation.

Impact of Interconnect Aspect Ratio

Finally, the effect of wire aspect ratio (AR) on the thermal characteristics is evaluated. For the same metal thickness, wires with smaller AR would suffer higher ΔT_{max} because of the smaller surface area-to-volume ratio (Fig. 15). For the same cross section area, indicating same current capability, a larger perimeter would result in lower ΔT_{max} by offering larger area for heat to diffuse out of metal wires, as shown in Fig.16. However, for embedded air gap (ILD: SiO_2 and IMD: Air), ΔT_{max} increases slightly with AR. This can be explained by the fact that with higher AR, embedded air gap interconnect structure would have increasing area contacted by air. Fig. 15 and Fig. 16 can be used to provide thermal design guidelines for interconnects.

SUMMARY

In conclusion, a simple 3D RC thermal circuit model is presented which allows quick evaluation of various Cu/low-k interconnect structures. It is demonstrated that via density strongly affects the spatial temperature distribution as well as the maximum temperature rise in interconnects and should be considered in interconnect design. However, if the via separation is much longer than thermal diffusion length, via effect will diminish. Furthermore, the impact of dummy thermal vias on the thermal characteristics of interconnects has been presented. It is shown that by optimal spacing of dummy thermal vias the Cu/low-k structures can have the same thermal capability as Cu/SiO_2. Additionally, the impact of wire aspect ratio (AR) on the thermal characteristics has also been shown to be important for the thermal design of deep submicron interconnect structures.

ACKNOWLEDGMENTS

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Thermal		Electrical
Temperature T [K]	⟺	Voltage V [V]
Heat q' [J]	⟺	Charge Q [C]
Heat flux q [W]	⟺	Current i [A]
Thermal resistance R_T [K/W]	⟺	Electrical resistance R[V/A]
Thermal capacitance C_T [J/K]	⟺	Electrical capacitance C[C/V]

Governing equations

Heat diffusion: $\nabla^2 T = R_T C_T \frac{\partial T}{\partial t}$ ⟺ RC transmission line: $\nabla^2 V = R C \frac{\partial V}{\partial t}$

Figure 1. Thermal-Electrical analogous quantities.

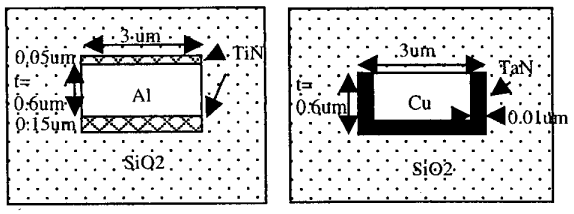

Figure 3. Schematic cross section of Al and Cu interconnects with cladding layers used in model validation Fig. 4 and for simulations in Fig. 5.

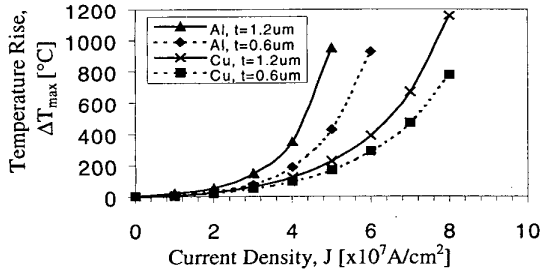

Figure 5. For the same wire cross section, shown in Fig. 3, Cu wire shows much lower temperature rise compared to Al wire under a 200 ns pulse stress. Symbols represent simulation points.

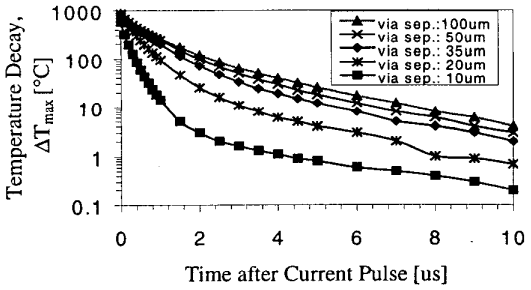

Figure 7. The temperature decay after a 200 ns current pulse, for Cu/low-k (polymer) global wires. The decay is facilitated by the presence of vias.

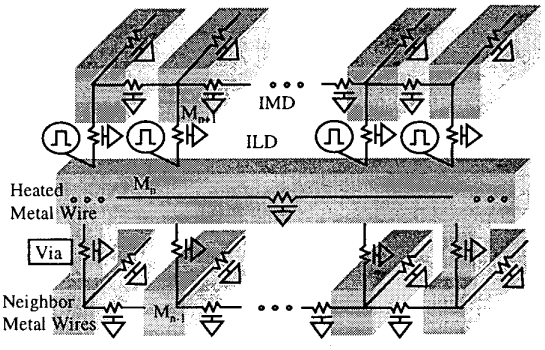

Figure 2. 3-D thermal circuit RC transmission line model for transient thermal analysis of interconnect structures.

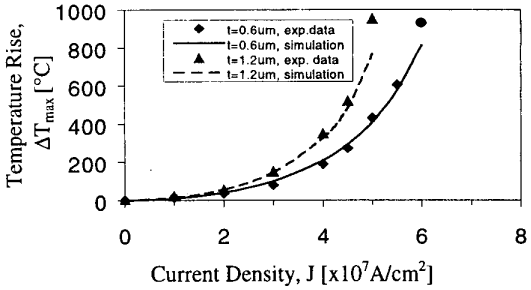

Figure 4. Validation of HSPICE thermal simulation with experimental data from [10]. Al interconnect test structure shown in Fig. 3 is used.

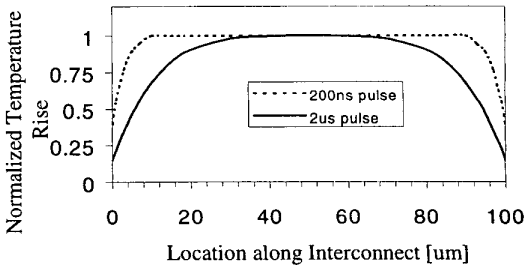

Figure 6. Simulated normalized temperature ($\Delta T/\Delta T_{max}$) profile along global Cu interconnect for two pulse durations with current density J=4x10^7 A/cm^2.

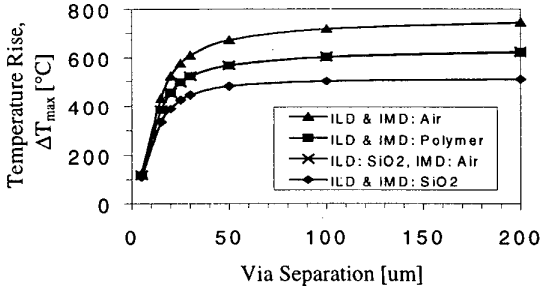

Figure 8. ΔT_{max} of global interconnects for a 200 ns current pulse with J=6x10^7 A/cm^2. ΔT_{max} increases with via separation and saturates when via effect has diminished.

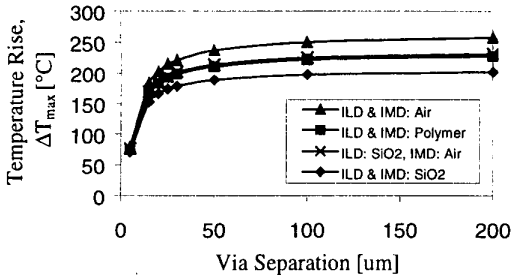

Figure 9. For a short pulse of 100 ns, with the same current density as in Fig. 8, ΔT_{max} of the global Cu interconnect is much less dependent on the dielectric materials.

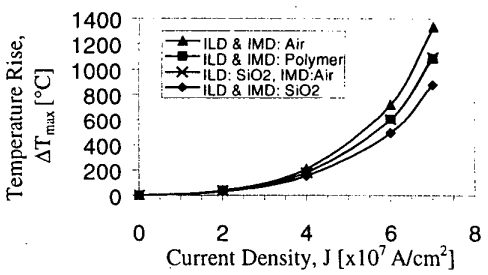

Figure 10. ΔT_{max} of Cu global interconnect with 100 μm via separation under a 200 ns current pulse. Temperature rises sharply with current density.

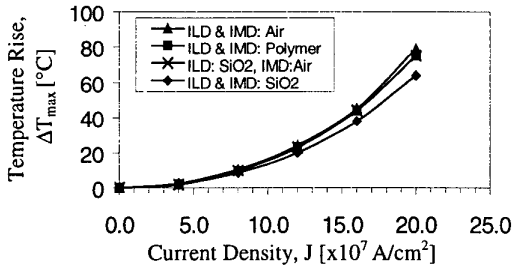

Figure 11. ΔT_{max} of Cu local interconnect with 1 μm via separation under a 200 ns current pulse. Temperature rises are much lower and nearly independent of the surrounding dielectric materials.

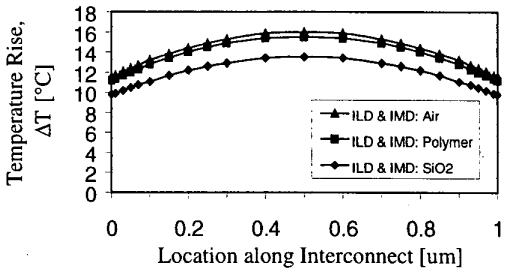

Figure 12. Temperature profiles along local Cu interconnect under a 200 ns pulse are gradual for all the dielectric materials and ΔT_{max} are about the same with J=1x10^8 A/cm^2.

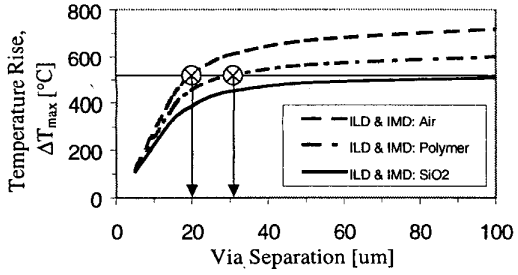

Figure 13. ΔT_{max} of Cu/air and Cu/polymer can match ΔT_{max} of Cu/oxide global interconnect if dummy thermal vias are added every 20 μm and 30 μm, respectively, with t_{pulse} = 200 ns and J=6x10^7 A/cm^2.

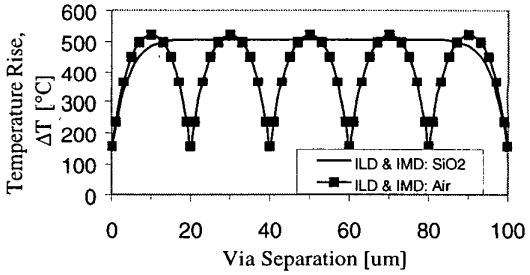

Figure 14. Cu/air with thermal vias every 20 um shows nearly the same ΔT_{max} as that of Cu/oxide global interconnect with 100 μm via separation under a 200 ns and J=6x10^7 A/cm^2 current pulse.

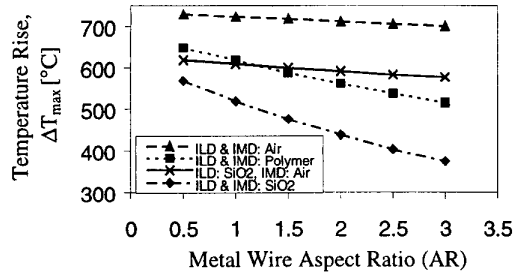

Figure 15. For the same metal thickness (2.5 μm), global interconnects with lower AR, shows higher ΔT_{max} due to lower surface area-to-volume ratio. t_{pulse} = 200 ns and J=6x10^7 A/cm^2.

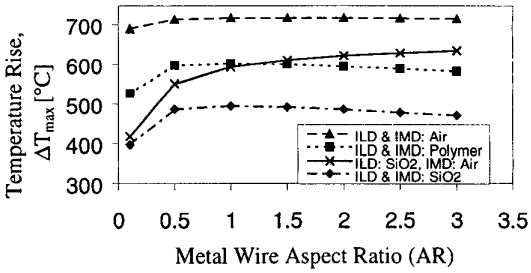

Figure 16. For the same metal wire cross section area (5 μm^2), the impact of AR and dielectric structure strategy is shown. ΔT_{max} peaks at AR=1 due to the smallest perimeters. t_{pulse} = 200 ns and J=6x10^7 A/cm^2.