Carbon Nanomaterials: The Ideal Interconnect Technology for Next-Generation ICs

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Editor's note:
Carbon nanotubes and graphene nanoribbons are two promising next-generation interconnect technologies. Electrical modeling and performance analysis have demonstrated the superiority of these emerging technologies compared to conventional copper interconnects, as this article explains.
—Sriram Vangal, Intel

THE SEMICONDUCTOR INDUSTRY is confronting an acute problem in the interconnect area as IC feature sizes continually scale below 32 nm. When the cross-sectional dimension of copper wires approach their mean free path (about 40 nm at room temperature), they suffer significant size effects because of increasing surface scattering, grain boundary scattering, and the presence of a highly resistive diffusion barrier layer, resulting in a sharp rise in copper resistivity. According to the 2008 *International Technology Roadmap for Semiconductors* (http://public.itrs.net), copper's resistivity could be more than three times higher than its bulk value at the 22-nm technology node. This steep rise in resistivity will adversely impact both performance and reliability in terms of circuit delay, chip temperature, and current-carrying capacity. This limitation of copper interconnects is driving research for alternative interconnect materials and technologies for next-generation ICs. In this research, carbon nanomaterials, with their many attractive properties, are emerging as the frontrunners to potentially replace copper for interconnects and passive devices in ICs, including vias and through-silicon vias (TSVs), horizontal wires (local, intermediate, and global levels) and off-chip interconnects.

In this article, we discuss various carbon nanomaterials, along with their prospects for next-generation interconnects and passive devices. We also provide a comparative analysis of these nanomaterials vis-à-vis optical and RF interconnects, and we illustrate why carbon nanomaterials constitute the ideal interconnect technology choice for next-generation ICs.

Unique properties of carbon nanomaterials

Low-dimensional allotropes of carbon, known as carbon nanomaterials, have extraordinary physical properties because of their unique structure. In particular, researchers have extensively investigated their 1D forms, carbon nanotubes (CNTs) and graphene nanoribbons (GNRs), because of their exciting prospects in various applications, including interconnects and passive devices in the nanoelectronics area.[1]

Atomic structure and properties

To understand the physics of CNTs and GNRs, we need to study their atomic structure. Both CNTs and GNRs can be formed from a single-layer graphene sheet. The carbon atoms in a graphene sheet are arranged in a 2D honeycomb lattice structure. A GNR can be formed by cutting a ribbon out of graphene following an edge shape (either *armchair* or *zigzag*). A CNT can be formed by rolling up a ribbon along circumferential vector $\vec{C}$ (see Figure 1a).

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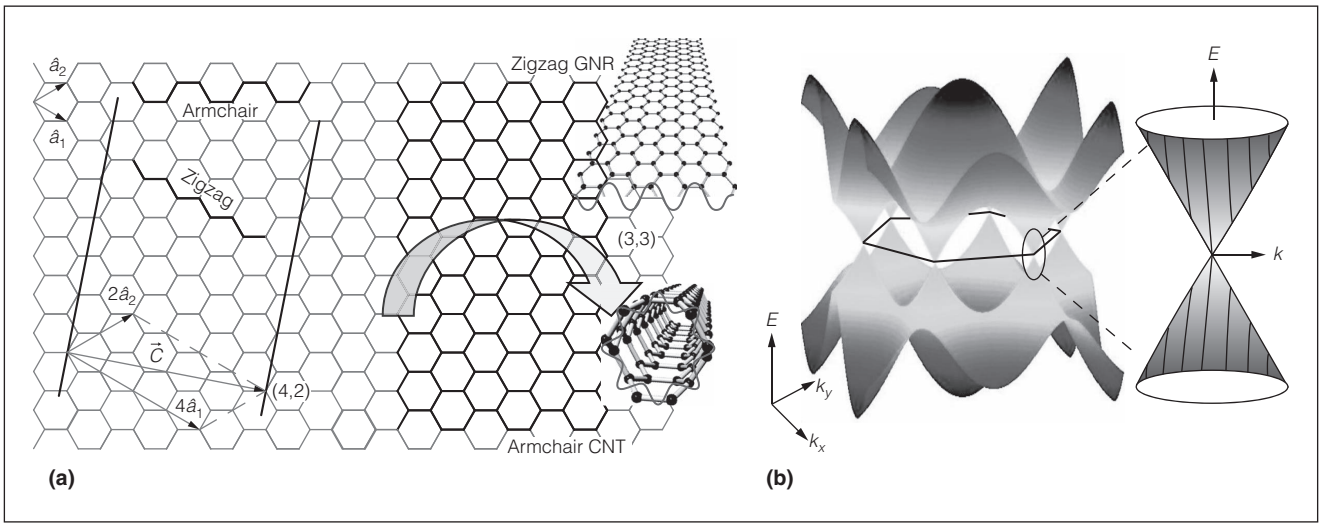

Figure 1. The atomic structure of CNT and GNR derived from a graphene sheet (a), and the band structure of graphene, where the conduction band and valence band meet at the six conical vertices (Dirac points) (b). The left side of (a) shows the chirality definition in terms of lattice vectors $\hat{a}_1$ and $\hat{a}_2$; the (4, 2) vector is shown as an example. The right side of (a) shows a zigzag-GNR and a (3, 3) armchair CNT based on the same ribbon, along with the schematic view of their wave function quantization. The zoomed-in conical shape on the right side of (b) shows a linear *E-k* relationship, where *E* is the energy and *k* is the wave vector. The wave function quantization leads to the formation of a set of slice cuts on the graphene band structure (the vertical lines on the right conical). If a slice cuts at one conical intersection point, there is no band gap (metallic); otherwise, there is a band gap (semiconducting). The band gap is inversely proportional to the GNR width or the CNT diameter.

The CNT's chirality is defined using $\vec{C}$ (the roll-up direction), which is a combination of lattice vectors $\hat{a}_1$ and $\hat{a}_2$:

$$\vec{C} = n \cdot \hat{a}_1 + m \cdot \hat{a}_2$$

where n and m are a pair of integers known as the chiral indices. Depending on the circumferential edge shape, a CNT can be *armchair* ($n = m$), *zigzag* ($n = 0$ or $m = 0$), as shown in Figure 1a, or *chiral* (other shapes). On the other hand, a GNR's chirality is defined by the edge shape, which is opposite to that of a CNT. Thus, starting from the same graphene strip, the CNT shown in Figure 1a is armchair, whereas the GNR is zigzag. The diameter D of the CNTs is also determined by the chiral indices:

$$D = \left|\vec{C}\right| / \pi = \frac{a}{\pi}\sqrt{n^2 + m^2 + mn}$$

where a is the lattice constant of graphene (0.246 nm).

Depending on the number of concentrically rolled-up shells, CNTs can be classified as single-walled CNTs (SWCNTs), double-walled CNTs (DWCNTs), or multi-walled CNTs (MWCNTs). Similarly, GNRs can be classified as monolayer, bilayer, or multilayer. The ideal interval distance between different shells in DWCNTs and MWCNTs, or between adjacent layers in multilayer GNRs is the Van der Waal's gap (about 0.34 nm).

The unique properties of CNTs and GNRs are largely due to the unique band structure of graphene, in which the *E-k (energy vs. wave vector)* relation is linear for the low energies near the six corners of the 2D hexagonal Brillouin zone (as shown in Figure 1b), leading to zero effective mass for electrons and holes.[1] Because of this linear dispersion relation at low energies, electrons and holes near these six points behave like relativistic particles described by the Dirac equation for spin-1/2 particles. Hence, the electrons and holes are called *massless Dirac fermions*, and the six corners of the Brillouin zone are called the *Dirac points*. Moreover, the sp^2 bonding in these materials (where *s* and *p* are the atomic orbitals), which is stronger than the sp^3 bonds in diamond, makes graphene the strongest material ever measured. CNTs and GNRs also have very high current-carrying capability (at least two orders of magnitude higher than that of copper). In addition, CNTs and GNRs have long mean free paths (MFPs) at low

Table 1. Properties of carbon nanomaterials relevant to VLSI interconnects and passive applications.

Property	W	Cu	SWCNT	MWCNT	Graphene or GNR
Maximum current density (A/cm^2)	10^8	10^7	$>10^9$	$>10^9$	$>10^8$
Melting point (K)	3695	1357		3800 (graphite)	
Density (g/cm^3)	19.25	8.94	1.3–1.4	1.75–2.1	2.09–2.33 (graphite)
Tensile strength (GPa)	1.51	0.22	22.2 ± 2.2	11 to 63	
Thermal conductivity ($\times 10^3$ W/m·K)	0.173	0.385	1.75 to 5.8	3	3 to 5
Temperature coefficient of resistance ($\times 10^{-3}$/K)	4.5	4	<1.1	-1.37	-1.47
Mean free path (*nm*) at room temperature	33	40	$>10^3$	2.5×10^4	1×10^3

* CNT: carbon nanotube; Cu: copper; GNR: graphene nanoribbon; MWCNT: multiwalled CNT; SWCNT: single-walled CNT; W: tungsten.
** All the references for these values reported in this table are listed in Li et al.[1] But these values are valid only for certain CNTs or graphene cases, because they depend on many other parameters, such as CNT diameter and GNR width, or even on different fabrication processes.

bias because of weak acoustic phonon scattering and suppressed optical phonon scattering at room temperature.

Table 1 summarizes the key electrical, thermal, and mechanical properties of carbon nanomaterials relevant to their interconnect and passive applications.[1]

Metallicity of CNTs and GNRs

For interconnect applications, the metallicity of CNTs and GNRs is the main concern. It's important to understand their electronic structure, which again originates from graphene's band structure, as shown in Figure 1b. The band structure of CNTs and GNRs can be studied from that of graphene by considering their structural confinement.

The difference in the confinement conditions between CNTs and GNRs is that the wave function along the CNT circumference is periodic, whereas the wave function along the GNR width vanishes at the two edges (Figure 1a). These confinements can be reflected into the band structure as slice cuts (Figure 1b), each representing one subband. Depending on the position of the slice cuts due to chirality and diameter, the resulting band structure could be without band gap (metallic) or with band gap (semiconducting).

Li et al. have explained that the condition for achieving a metallic CNT can be expressed as $n - m = 3i$, where i is an integer.[1] Hence, armchair CNTs are always metallic (see Figure 1a), whereas zigzag CNTs could be metallic or semiconducting, depending on the chiral indices (n, m). Statistically, a natural mix of CNTs will have one-third metallic and two-thirds semiconducting chirality. On the other hand, zigzag GNRs are always metallic (a small band gap will be induced in zigzag GNRs once electron spin is considered, because of the staggered sublattice potential from magnetic ordering[1]). Armchair GNRs can be either metallic or semiconducting, depending on the number (N) of atoms across the width: metallic when $N = 3i - 1$, and semiconducting when $N = 3i$ or $3i + 1$.

Modeling and performance analysis

As interest in carbon-nanomaterial-based interconnects gains momentum, a realistic analysis of these interconnects is necessary to evaluate their performance and identify the domains of on-chip interconnections (local, intermediate, and global interconnects or vias) where this novel interconnect technology has the potential to replace copper. Here, we introduce circuit models for various types of CNTs and GNRs, and analyze their performance in various applications.

RLC model

Figure 2 shows the proposed RLC-equivalent circuit models for SWCNTs and GNRs. For DWCNT and MWCNT interconnects, a more complicated equivalent circuit is employed. (Li et al. presented a detailed model for MWCNT interconnects, which is also valid for DWCNT interconnects. They also provided a detailed discussion about other CNT and GNR modeling work.[1]) We can derive the conductance of CNTs and GNRs using the linear-response Landauer formula,[1] which takes into account the large quantum contact resistance R_Q (about 12.9 kΩ per conducting channel) between 1D conductors and 3D materials. Although both CNTs and GNRs are considered 1D

materials, a significant difference between them is the existence of edge scattering in GNRs. CNTs are seamless tubular structures, which allow electrons to travel around. GNRs, however, have abrupt edges and induce scattering because of edge roughness.

Figure 3a compares the resistances of various CNTs (SWCNTs, DWCNTs, and MWCNTs) and GNRs (monolayer GNRs, neutral multilayer GNRs, and doped multilayer GNRs). For short lengths, due to large quantum contact resistance, the resistance per unit length of CNTs and GNRs are large but decrease with increasing length, and they become stable after 10 μm. For longer lengths, all types of CNTs could offer lower resistance than copper, whereas only AsF_5 (arsenic pentafluoride) intercalation-doped multilayer GNRs with high specularity (or very smooth edges) can provide lower resistance than that of copper. (Intercalation involves inserting a dopant layer between adjacent graphene layers.)

Besides quantum contact resistance R_Q, the RLC model in Figure 2 has two other new circuit elements: quantum capacitance C_Q and kinetic inductance L_K. Both of these arise mainly because CNTs and GNRs are low-dimensional materials with low density of states near the Fermi level. In materials with low density of states, adding charges to the system not only requires certain electrostatic energy, but also requires nonnegligible additional energy to occupy the higher energy states. This additional energy can be modeled as the quantum capacitance C_Q (about 193 aF/μm per channel) in series with electrostatic capacitance C_E.

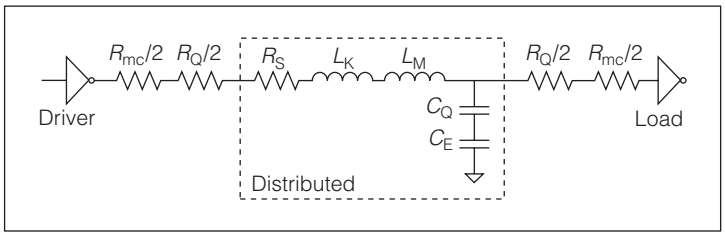

Figure 2. The equivalent distributed RLC circuit model of an SWCNT or GNR interconnect. R_{mc} is the imperfect contact resistance between the CNT and the metal; R_Q is the quantum contact resistance associated with the contact from the 1D conductor to the 3D conductor; R_S is the scattering-induced resistance, depending on mean free path; L_K is the kinetic inductance; L_M is the magnetic inductance associated with the CNTs or GNRs; and C_Q and C_E are the quantum and electrostatic capacitances.

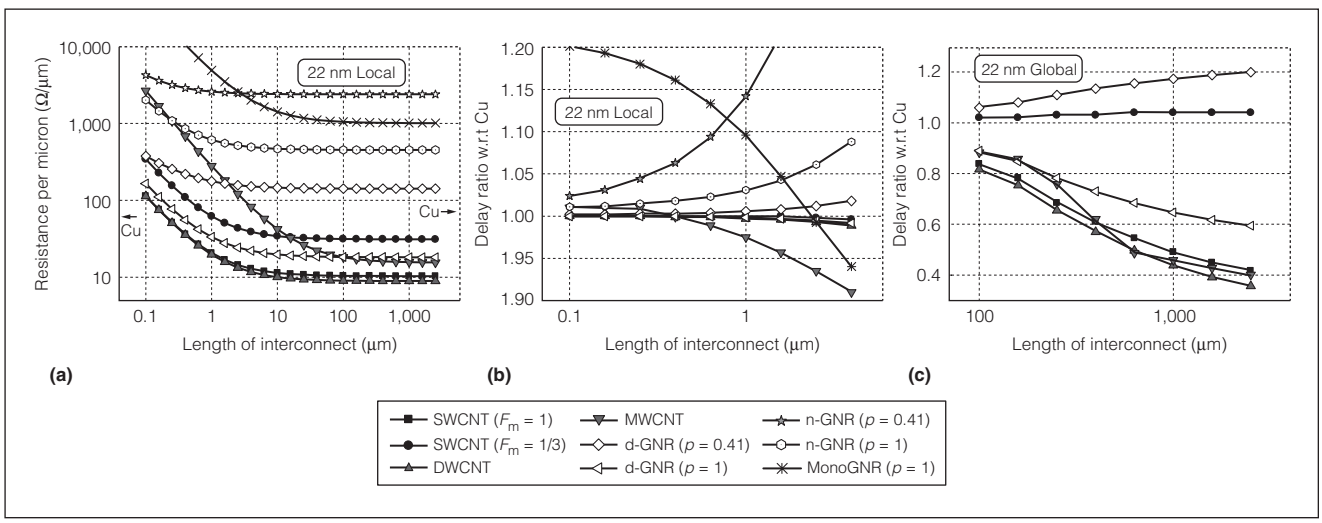

Figure 3. Resistance per unit length comparison for different types of CNT and GNR interconnects for the dimensions predicted in the 2008 *International Technology Roadmap for Semiconductors* (http://public.itrs.net) for local interconnects at the 22-nm technology node (22-nm width and 44-nm height) (a). Signal delay ratios (with respect to copper) of SWCNT, DWCNT, MWCNT, and different types of GNRs at the 22-nm technology node for local (b) and global (c) interconnects. The driver size is assumed to be 2 in (b) but is set to 100 in (c). The global-interconnect width is set to be five times the minimum width, as predicted by the *ITRS*. F_m indicates the fraction of metallic SWCNTs in the SWCNT bundle; n-GNR and d-GNR represent neutral multilayer GNRs and AsF_5 (arsenic pentafluoride) intercalation-doped GNRs, respectively; and p indicates the specularity of a GNR edge: p = 1 indicates no edge scattering (best case), and p = 0 implies a completely diffusive edge (worst case). For the DWCNT, the diameter is set to 1.5 nm, and metallic fraction F_m = 1. The diameter of the MWCNT and the width of the GNR are equal to the wire width (W).

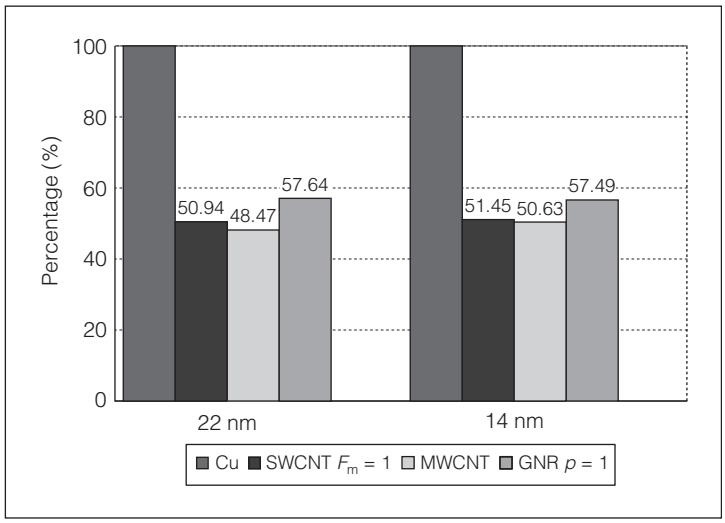

Figure 4. Normalized global-interconnect power consumption of carbon-based interconnects with a delay equal to the optimal delay of copper interconnects, for different technology nodes. The width of the global interconnect is assumed to be five times the minimum width for the different technology nodes. The interconnect power considered here comprises the dynamic and leakage power of the repeaters. The diameter of the SWCNTs is 1 nm; the diameter of the MWCNTs is the minimum width of the wire (32 nm for the 22-nm node, and 21 nm for the 14-nm node). The GNR is assumed to be an AsF_5 intercalation-doped multilayer GNR with a width equal to that of the interconnects.

Similarly, to establish a current in a system, the number of charges moving in one direction must exceed the charges moving in the other direction. These excess moving charges also require excess energy to occupy higher energy states, and the excess energy associated with the moving charges can be modeled as the kinetic inductance L_K (about 8 nH/μm per channel) in series with the conventional magnetic inductance L_M. The value of kinetic inductance is about three orders larger than that of magnetic inductance in a single CNT or monolayer GNR. (Other experimental work on the high-frequency characterization of CNTs has verified the existence of kinetic inductance; see the work of Li et al. for details.[1])

Interconnect performance analysis

We've compared the performance of different carbon-nanomaterial–based interconnects with that of copper interconnects on the basis of the model in Figure 2. Figures 3b and 3c show the delay ratios of CNT and GNR interconnects with respect to copper for local- and global-level interconnects at the 22-nm technology node.[1]

For local interconnects, most CNT and GNR interconnects are comparable to copper, except monolayer GNRs and diffusive-edge neutral multilayer GNRs. This is because the driver size at the local level is typically very small (2 in this work), and driver resistance dominates the total resistance of the interconnect system. SWCNTs, DWCNTs, and doped GNRs ($p = 1$) are slightly better than copper. MWCNTs are slightly worse than copper at short lengths but become better for lengths greater than 0.5 μm because of the smaller capacitance of MWCNT interconnects.[1]

For global interconnects, most CNTs (except SWCNTs with a one-third metallic fraction) outperform copper, whereas only doped GNRs with $p = 1$ are better than copper. Ideal SWCNT (all metallic) and DWCNT cases (where all the shells are metallic) have similar performance: both could provide more than 50% delay enhancement at a 1-mm length for the 22-nm technology node. The ideal GNR case (doped GNR with $p = 1$) still cannot be better than the ideal SWCNT, DWCNT, or MWCNT case, because of GNR's lower conductance.

Besides delay improvement, CNT interconnects also lower power consumption. This is because lower resistance of CNT interconnects requires fewer repeaters, thus reducing the power consumption of the global wires. Figure 4 shows that if the delay of CNT and GNR interconnects is kept at the optimal delay of copper interconnects, CNT- and GNR-based interconnects would reduce the global interconnect power consumption by ~50% compared to that of copper interconnects. Moreover, employing MWCNT bundles lowers the capacitance of local wires (by about 10%),[1] which also reduces the overall interconnect-related power consumption.

High-frequency properties

Because of its large kinetic inductance or large momentum relaxation time, the high-frequency behavior of a CNT bundle differs considerably from that of conventional metals.[1] Figure 5a shows the skin depths of CNTs as a function of frequencies, and the equation to calculate the skin depth δ of CNTs follows[1]:

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma_0}} \cdot \sqrt{[(\omega\tau)^2 + 1] \cdot \left[\sqrt{(\omega\tau)^2 + 1} - \omega\tau\right]}$$

where ω, μ, σ_0, and τ are the angular frequency, permeability, DC conductivity, and momentum relaxation time, respectively.

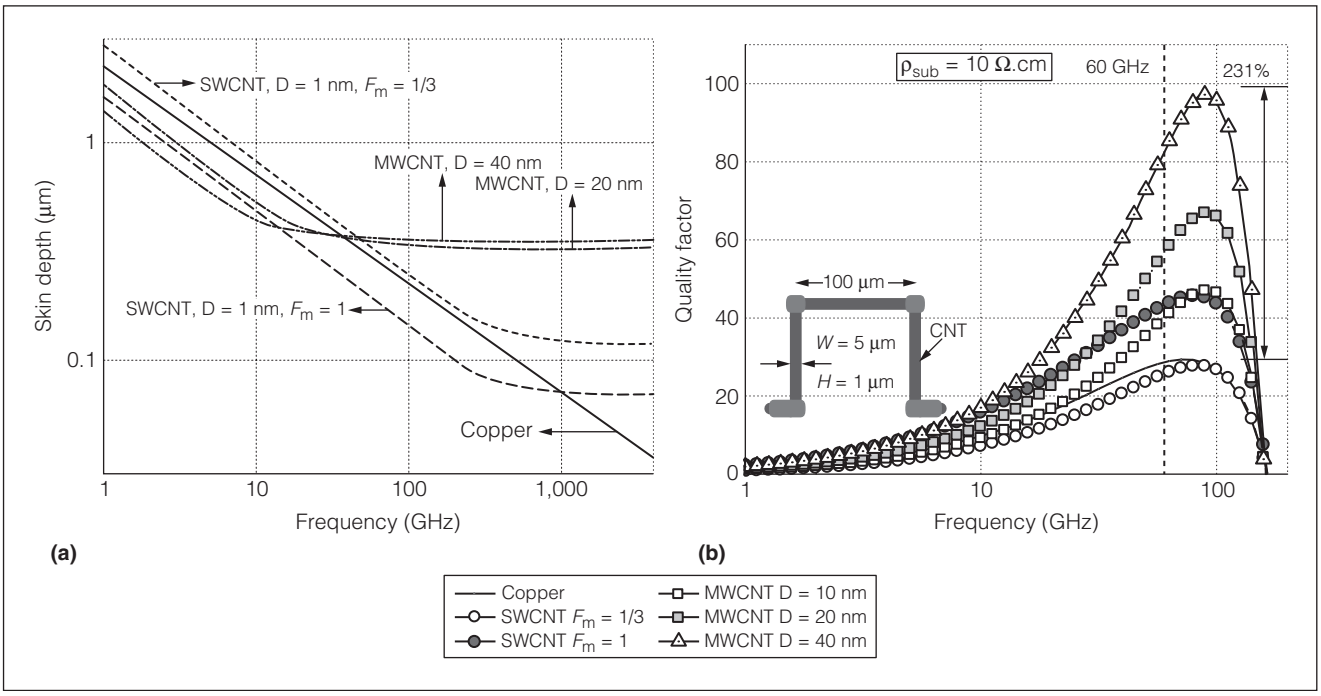

Figure 5. Skin depths of different types of CNT bundles and copper, as a function of frequency (a). Quality factor of 0.75-turn inductors based on copper, SWCNT, and MWCNT interconnects, as a function of frequency for substrate resistivity ρ = 10 Ω·cm (low loss) (b). All CNT bundles are assumed to be ideally densely packed (at intervals of about 0.34 nm). The structure of the CNT inductor is shown in inset of (b), where the dark areas represent CNT bundles, and the gray metal stacks connect the CNTs at each corner; *W* and *H* are the line width and height of CNT or copper wire. (*D* represents the diameter of the CNTs.)

The skin depth of copper wire continues to decrease with frequency, as expected from conventional theory. But the skin depths of CNTs first decrease with frequency, then saturate after certain frequencies, implying reduced skin effects in CNTs. As Li et al. explained,[1] this is due to the large kinetic inductance or large momentum relaxation time τ associated with CNTs. This unique high-frequency behavior of CNT interconnects is very promising for high-frequency applications; one of the important issues in high-frequency circuit design is that the conductor loss increases dramatically because of skin effects. If the resistance of interconnects increases by a smaller amount or even remains practically unchanged at high frequencies, employing CNT interconnects can significantly enhance the circuit's high-frequency performance. It is interesting that MWCNTs not only start saturating at a relatively lower frequency but also have relatively large saturated skin depths, indicating their promising applications in future high-frequency circuits.

GNRs share many unique properties with CNTs, including large kinetic inductance, so we expect GNR-based interconnects to also have reduced skin effects. However, because the mean free path of GNRs could be on the same order as their width, an anomalous skin effect (which arises when the skin depth becomes comparable to the mean free path of the carriers in the conductor) would begin to play a role in the GNRs' conductance.[1] Quantitative analysis is required to accurately estimate the skin effect in GNRs.

CNT-based inductors

To take advantage of the unique high-frequency properties of CNTs, researchers have designed and analyzed CNT-based on-chip inductors.[1] Figure 5b shows that the maximum *Q* factor of a 0.75-turn inductor can be increased by as much as 230% (3.3 times) by replacing copper with CNTs for a low-loss substrate ($\rho_{sub} = 10\ \Omega$ cm). This significant enhancement in the *Q* factor arises not only because of the lower DC resistance of CNTs, but also because of the reduced skin effect in CNT interconnects discussed earlier.

CNT vias (vertical interconnects)

Thus far, most CNT interconnect fabrication processes have focused on short vertical interconnects

(vias) because of their ease of fabrication. Moreover, for vias, where reliability is more critical than performance, the outstanding current-carrying capacity of CNTs can be leveraged. Hence, thermal analysis of CNT vias and their impact on the thermal management of the back end (which significantly impacts reliability) must be quantified. Since typical via height is smaller than 300 nm, which is smaller than both the electron and phonon mean free paths of CNTs, CNT vias are both electrically and thermally in the ballistic-transport regime. However, because of the existence of a large quantum contact resistance, ballistic CNT vias would not provide lower conductance than copper vias except for very small diameters and ideally densely packed SWCNT bundles.[1] The electrothermal analysis for a typical metal-via-metal structure also shows that the maximum temperature increases monotonically with via height for copper vias but, because of thermal ballistic transport, remains relatively unchanged for CNT vias. Although the electrothermal performance of both SWCNT and MWCNT interconnects would be better than that of tungsten vias, if the objective is to outperform copper vias, then small-diameter and densely packed SWCNT vias with good electrical and thermal contacts are needed. Moreover, taller vias are preferred for the CNT case, which indicates their potential applications in 3D integration.

In 3D ICs, a key technology is high-aspect-ratio vertical interconnects, or TSVs, which provide connectivity between different active layers. Because CNT bundles can potentially offer excellent electrical and thermal properties, they can be excellent candidates for TSVs in 3D ICs.[1] In fact, well-aligned high-aspect-ratio CNT TSVs have been demonstrated.[2] Most recently, Xu et al. developed an accurate compact AC model that is valid for various frequency regimes and different materials, including CNTs.[3] Although the electrical performance of CNT TSVs is comparable to that of copper TSVs, the former are very good candidates for TSVs because of their superior thermal and reliability properties.

CNT-based capacitors

The small form factor and high surface-area-to-volume ratio of CNTs are beneficial for metal-insulator-metal (MIM) capacitor applications. In particular, the bottom-up process allows fabrication of high-aspect-ratio CNTs,[4] which potentially could be used for designing high-density capacitors. Simulation results for possible CNT-based vertical capacitor structures have shown that the capacitance density of such CNT-based capacitors can reach as high as 38.39 fF/μm^2,[1] far larger than the *ITRS* requirement of 12 fF/μm^2 for year 2022, indicating excellent potential to replace current MIM capacitors.

Off-chip applications

Besides on-chip interconnect-related applications, CNTs can also serve as chip-to-packaging interconnects, thanks to CNTs' superior electrical, thermal, and mechanical properties. Iwai et al. have used CNTs as flip-chip bumps for packaging high-power amplifiers (HPAs),[5] and they've shown that, besides enhancing an HPA's high-frequency performance, CNT bumps also facilitate heat removal. Recently, Kordás et al. have used patterned CNTs as heat spreaders for chip cooling,[6] not only achieving better thermal performance compared to copper cooling structures but also providing a lightweight and mechanically robust cooling system.

Fabrication and integration challenges

Although CNT and GNR fabrication technologies have progressed rapidly since they were first discovered, their large-scale integration into current VLSI technology still faces several challenges.

CNT interconnects

For CNT interconnect applications, chemical vapor deposition (CVD) methods are most suitable for growing CNTs, because of their selective-growth, large-area deposition, and aligned-CNT-growth capabilities. Thus far, most CNT interconnect fabrication work has focused on MWCNTs, which can guarantee metallic behavior. Several groups—for example, Nihei et al.[7]—have pursued conventional etch-first approaches. Such approaches deposit the dielectric and etch the via holes before growing the nanotubes. Li et al. have proposed an alternative bottom-up approach,[4] which first grows the CNT via on the patterned catalyst at the bottom metal layer before depositing the dielectric. Most recently, Katagiri et al. have obtained high-density and high-quality MWCNT bundles by using low-temperature growth (450°C), achieving a resistance of 52 Ω for a 70-nm diameter via, where the CNT diameter is 10 nm and the density is $3 \times 10^{11}/cm^2$ (about 27.8% of the ideal packing-volume fraction).[8] Dijon et al. have also reported CNT bundles with a diameter of 3.8 nm and a density of

$1.2 \times 10^{12}/cm^2$ (about 20% of the ideal packing-volume fraction).[9] As Figure 6 shows, for MWCNTs to have a lower resistance than copper, a higher volume fraction of MWCNTs must be achieved in future fabrication processes. Also, the required volume fraction decreases with increasing length because of the lower impact of the contact resistance in long CNTs. Note that the high density number will not necessarily result in large volume fraction, because the latter also depends on the diameter of the CNTs. This can be clearly observed by comparing the diamond and circular dots in Figure 6.

Until recently, growing dense bundles of SWCNTs was difficult because the fertility of the catalyst particles for SWCNT growth was low. However, Futaba et al. have reported advances in the densification of SWCNT bundles along with a supergrowth process.[10] In this process, SWCNT bundles can achieve a density as high as $8.3 \times 10^{12}/cm^2$ (a diameter of about 2.8 nm, which is 72% of the ideal packing-volume fraction). From Figure 6, we observe that SWCNTs with this density have a lower resistance than copper. Most recently, researchers have reported significant progress regarding the chirality control of SWCNTs: Harutyunyan et al. have achieved 91% metallic SWCNTs using the CVD method by varying the noble-gas ambient temperature during catalyst annealing, combined with oxidative and reductive species.[11]

From a CMOS integration aspect, Kawabata et al. have achieved low-temperature (365°C) growth for on-chip CNT vias.[12] They have also shown that, at low temperatures, CNT vias can be successfully incorporated in ultralow-K dielectrics ($K = 2.6$) with negligible impact on electromigration reliability. In addition, Xu et al. have demonstrated growth of well-aligned high-aspect-ratio CNT bundle-based TSVs,[2] implying potential applications in emerging 3D ICs.

Although significant progress in CNT fabrication and integration has been made, one of the greatest challenges remaining is to grow long horizontal CNT bundles. Because CNT bundles always tend to grow perpendicular to a surface, depositing the catalyst on sidewalls would enable growth of horizontal CNTs. However, the key issues associated with this approach are the catalyst deposition techniques and the achievement of long-length high-density bundles. Nihei et al. have demonstrated short-length (about 5 μm) horizontal CNT bundles.[7] The same has not yet been accomplished for long lengths, however. Controlling CNT orientation is also possible by rotating the substrate with respect to the direction of gas flow in the CVD system. Other approaches, such as electric-field-induced multidirectional growth or fluidic methods, are not suitable for large-scale integration.

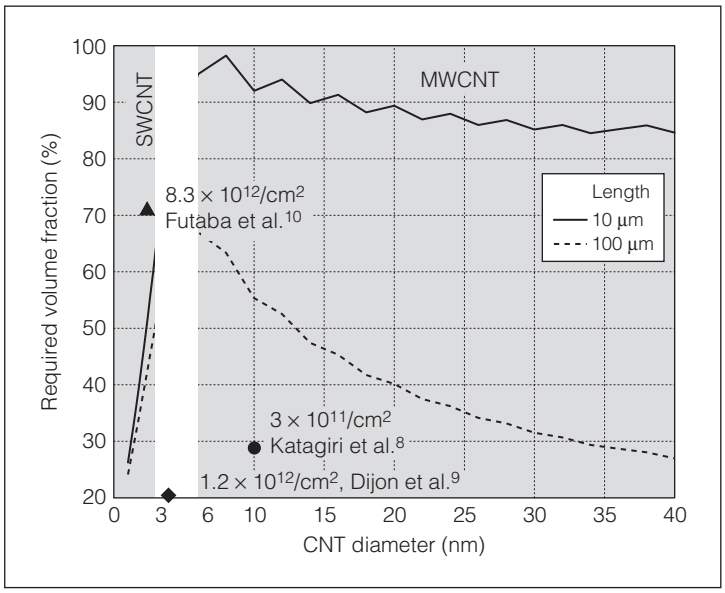

Figure 6. The required volume fraction of CNT bundles to have lower resistivity than copper as a function of CNT diameter for two typical interconnect lengths, 10 μm and 100 μm. The resistivity of copper is set to 4.2 μΩ·cm, which is the *ITRS*-predicted value for global interconnects at the 22-nm technology node. The volume fraction is defined as the density with respect to the ideal maximum densely packed case (at CNT intervals of about 0.34 nm). The diameter range considered for SWCNTs is 1 nm to 3 nm, whereas for MWCNTs it is from 6 nm to 40 nm. The metallic fraction of the SWCNT bundle is set to be 100%. For lower metallic-fraction SWCNT bundles, the value of the required volume fraction needs to increase accordingly. The figure also shows three recent experimental data points for which the *y*-axis should be interpreted as "achieved volume fraction." This data highlights the fact that both density and diameter of CNTs are important factors for determining the volume fraction as well as the resistivity of a bundle.

GNR interconnects

Because GNRs can be obtained by patterning graphene, their fabrication is considered more controllable than that of CNTs. Various methods of fabricating GNRs have been pursued, but difficulties also exist in those methods. Although the thermal decomposition of single-crystal SiC (silicon carbide) can be employed to produce thin graphene films, this

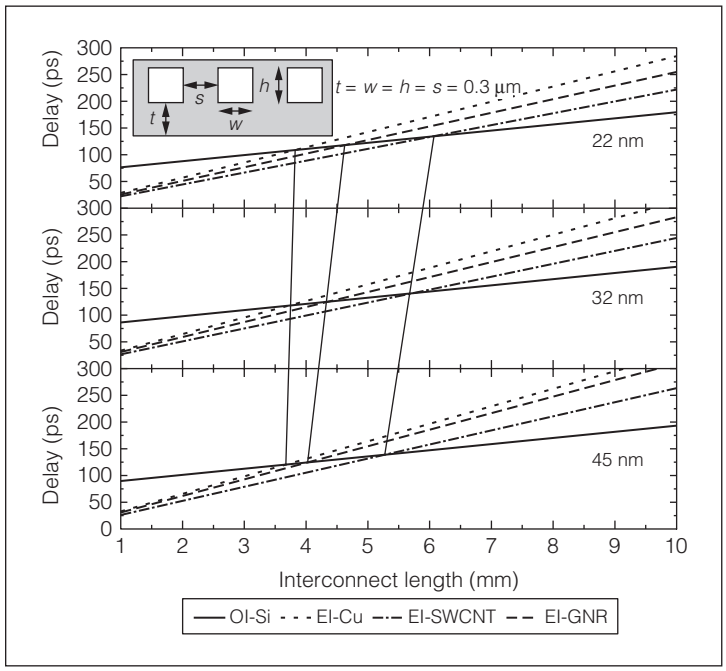

Figure 7. Delay comparison between optical interconnects (OIs) and RLC electrical interconnects (RLC-EIs) with different materials for different technology nodes. Both the width and height of the interconnects are assumed to be 0.3 μm. The diameter of the SWCNTs is set at 1 nm, and the metallic fraction of the SWCNT bundle is assumed to be 100%. The GNR is assumed to be an AsF_5-doped multilayer GNR with perfectly smooth edges. (The OI delay is adapted from Figure 7 of Koo et al.,[16] but the unit of delay [latency] was incorrectly labeled there; it should be in ns rather than in ns/mm.)

approach requires a single-crystal substrate, which is not suitable for interconnects that are typically formed over some dielectric material. This technique also requires a high temperature, which isn't suitable for interconnects, due to the relatively low back-end thermal budget (about 400°C) in IC fabrication technologies.

Graphene can also be mechanically exfoliated from graphite and deposited onto an insulating substrate, but this approach is uncontrollable for large-scale fabrication. Yu et al. segregate graphene by dissolving carbon in a nickel substrate at high temperatures,[13] covering the graphene with a silicone film, and then transferring the graphene to another desired substrate. The nickel substrate can be subsequently removed to allow GNR wire and contact formation through patterning. Similarly, graphene can be deposited on copper foils (which can be removed later) and transferred to insulating substrates.[14] These approaches appear to be promising for interconnect applications, but further investigation is necessary.

To improve the conductivity of multilayer GNRs, Li et al. have proposed intercalation doping,[1] which has been studied for a long time in bulk graphite. Generally, graphite can be intercalation-doped through exposure to dopant vapors (e.g., AsF_5). Because multilayer GNRs can be considered as patterned bulk graphite, intercalation doping should be achievable in multilayer GNRs.

Most recently, Fujitsu has demonstrated the possibility of building "all carbon" interconnect structures by combining CNTs and GNRs.[15] This approach first grows the horizontal GNR layers on a cobalt film, which is followed by vertical CNT growth after the cobalt film disaggregates to form cobalt nanoparticles during the CVD process. However, the contacts between the CNT bundle and the GNR layers in this structure need more investigation and engineering.

Comparison with other emerging interconnect technologies

Besides carbon-nanomaterial-based interconnects, other emerging interconnect technologies include optical interconnects (OIs), and RF or wireless interconnects (RF-Is). Both are expected to transfer signals at the speed of light. In OIs, the optical signal is generated from laser sources and is modulated so that electrical signals are translated to optical signals. The optical signals are then transferred through optical waveguides. Using photodetectors and demodulators, the optical signals can be translated back to electrical signals.

Koo et al. have presented a performance comparison and power analysis of OI and RLC electrical interconnects (RLC-EIs).[16] The results indicate that OIs are much better than copper even at 1-mm-length global interconnects. However, there are assumptions in their study that are either unfair to RLC-EIs or overoptimistic for OIs. First, in the latency comparison for all technology nodes, the OIs are assumed to have a 0.6-μm pitch, but the RLC-EIs are assumed to follow *ITRS* dimensions, which shrink as technology scales. This underestimates the performance of RLC-EIs. The *ITRS* global-interconnect dimensions are the minimum dimensions but not those that must be used in practical global interconnects. In addition, the inductance is estimated by considering only partial self-inductance without a return path, which greatly overestimates the total inductance of the wire. Figure 7 shows the

delay comparison between OIs and RLC-EIs at different technology nodes when the dimension of the global wires is set to $0.3 \times 0.3\ \mu m^2$ (half the pitch of 0.6 μm) rather than the *ITRS* dimensions. To be comparable with the delay of copper interconnects, the minimum required length of an OI must be greater than 3.5 mm. This required length would need to be even greater to be comparable to the delay of carbon interconnects (about 5.5 mm for SWCNT interconnects). Moreover, this requirement must increase further when the technology scales down.

Second, even the 0.6-μm pitch is overoptimistic for silicon-based OIs. The evanescent coupling between neighboring waveguides (or crosstalk) restricts the minimum pitch to 0.75 μm.[17] Moreover, implementing the wavelength division multiplexing (WDM) technique, which allows multichannel and far higher bandwidths, requires increasing the waveguide width further to make all the selected wavelengths transportable in the waveguides. Therefore, the estimated bandwidth of OIs in the work of Koo et al. is overly optimistic.[16] At the 22-nm technology node, the silicon-based OIs have a lower bandwidth than the RLC-EIs unless there are more than 9 WDM channels in the OIs.[17] The OIs also have large power consumption at both the optical generator and modulator side and the optical detector and demodulator side. Moreover, OIs require lasers, photodetectors, and other optical or optoelectronic devices and circuits, which are not compatible with mainstream CMOS technologies, making them highly cost-ineffective.

Another possible interconnect configuration is RF-Is. This approach modulates the signals in different frequencies from a transmitter and couples them to a shared transmission line. The signals travel through the transmission line at the speed of light; then, they are demodulated and recovered by the receivers. The benefit of RF-Is is that, unlike OIs, they are compatible with mainstream back-end-of-line (BEOL) technologies. Moreover, unlike RLC-EIs, they maintain the speed of light in signal transferring. Also, as with OIs, RF-Is allow multichannel signal transfer, which increases the bandwidth. One of the major issues of RF-Is, however, is their wire width. The typical wire width of a low-loss transmission line is above 10 μm, whereas the ground or return path (the sides of the coplanar waveguide or the bottom plate of the microstrip transmission line) is even wider. Chang et al. have proposed a configuration that treats RF-Is as "freeways" (only a few points are connected using RF-Is) and treated RLC-EIs as "local roads" (most other connections are RLC-EIs).[18] It is important to note that the RF-I configuration does not conflict with the application of carbon nanomaterial interconnects. With smaller resistances and reduced skin effects, the transmission lines based on CNTs or GNRs can be made smaller than copper lines to satisfy the requirement of low loss.

Another innovative configuration of wireless interconnections is inductively coupled superconnects in 3D ICs to replace the function of TSVs.[19] The advantage of this configuration over physical TSVs is that it avoids the reliability issue in TSVs, simplifies the fabrication of 3D ICs, and allows different supply voltages to be used in different stacked chips. However, wireless inductively coupled superconnects are much larger than physical TSVs (about 100 μm compared to about 5 μm for TSVs[3]), have higher power consumption, need additional power and clock-bonding wires, and require a careful design to avoid any noise. Moreover, unlike physical TSVs, this configuration cannot provide efficient thermal dissipation paths.

Both optical and RF interconnects require complicated circuit designs to be implemented correctly and to exhibit certain advantages over electrical interconnects for very long lengths (several millimeters), which is rare in on-chip interconnects. On the other hand, optical and RF interconnect configurations have potential for off-chip interconnect applications.

Table 2 provides a qualitative comparison of different interconnect technologies with respect to copper electrical interconnects. This table makes it clear that carbon-nanomaterial–based interconnects would be the ideal choice for the next-generation interconnect technology.

From this theoretical analysis, it's clear that carbon nanomaterials are the ideal choice for next-generation interconnects in all domains, including local and global interconnects, vias, TSVs, and off-chip interconnections. Both CNTs and GNRs can reduce interconnect delays (by up to ~60% for global interconnects) and power consumptions (by up to ~50% for global interconnects). However, many fabrication and integration challenges remain, although significant progress has been achieved during the past few years. The main challenges for CNT-based interconnects are the fabrication of high-metallic-fraction (for SWCNT), high-density, and well-aligned bundles, as well as fabrication of long horizontal

Table 2. Comparison of different emerging interconnect technologies with respect to copper interconnects from electrical, thermal, and reliability perspectives.

Emerging interconnect technology	Local interconnects	Global interconnects	On-chip vias	Through-silicon vias	Off-chip interconnects
SWCNT	Comparable for electrical but better for reliability	Depends on metallic fraction (could reduce both delay and power)	Could be comparable for electrical and thermal but much better for reliability	Comparable for electrical but better for thermal and reliability	Depends on metallic fraction
MWCNT	Comparable for electrical but better for reliability and for lower power	Better (reduces both delay and power)	Worse for both electrical and thermal but better for reliability	Comparable for electrical but better for thermal and reliability	Better
Monolayer or neutral GNR	Worse	Worse	NA	NA	NA
Multilayer doped GNR	Comparable	Depends on edge specularity (could reduce both delay and power)	NA	NA	NA
Optical	NA	Worse or comparable	NA	NA	Better
RF or wireless	NA	Only better in specific applications	NA	(Wireless superconnect) worse from both electrical and thermal perspectives but possibly better from a reliability perspective	Better

bundles. For GNR-based interconnects, the key issues are fabrication of doped multilayer GNRs and good control of edge roughness. ■

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