

Current Status and Future Perspectives of Carbon Nanotube Interconnects

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Abstract

Abstract- In this paper, we review the current status of CNT interconnect research, from both fabrication and modeling aspects. The fabrication issues of vertical and horizontal CNT interconnects and remaining challenges are discussed. State-of-the-art in both SWCNT and MWCNT modeling and performance analysis are presented. In addition, high-frequency effects, off-chip application, and process variation of CNT interconnects have also been discussed.

Keywords: carbon nanotube, interconnect, performance analysis, high-frequency, process variation.

1. Introduction

The resistivity of Cu interconnects in current and imminent technologies is increasing rapidly under the combined effects of grain boundary scattering, surface scattering and the presence of a highly resistive diffusion barrier layer [1], [2]. The steep rise in parasitic resistance of Cu interconnects not only increases interconnect delay (degrades electrical performance) but also leads to significant reliability issues [3] due to decreasing thermal conductivity of low-k dielectrics [2] and increasing current density demands from interconnects [4]. Due to their long mean free paths (MFP), high current carrying capability and high thermal conductivity, Carbon Nanotubes (CNTs) are expected to be a very good alternative material for future nanoscale interconnects, which can enhance the electrical performance as well as eliminate electromigration reliability concerns that plague nanoscale Cu interconnects. CNTs are sheets of graphene rolled up as hollow cylinders. CNTs can be classified as Single-Walled (SWCNTs, with only one shell and diameter ranging from 0.4 nm to 4 nm) and Multi-Walled (MWCNTs, with several concentric shells and diameter ranging from several nm to tens of nm). While SWCNTs can be either metallic or semiconducting depending on their chirality (the direction in which they get rolled up); giving rise to zigzag (mostly semiconducting), armchair (metallic) or chiral nanotubes (mostly semiconducting), MWCNTs are always metallic. A comparison of the properties of Cu, single-walled (SWCNT) and multi-walled CNTs (MWCNT) is shown in Table I. Specifically, Fig. 1 shows the resistivity comparison among Cu wire, SWCNTs and MWCNTs for different lengths.

2. CNT Interconnect Fabrication and Integration

For interconnect applications, chemical vapor deposition (CVD) methods are most suited since they have the capability of selective growth, large area deposition, and aligned CNT growth. Moreover, the high resistance associated with an isolated CNT (greater than 6.45 K Ω) [8] necessitates the use of a bundle of CNTs conducting current in parallel to form an interconnection [10]-[13]. The current state-of-the-art of on-chip integration of CNTs as interconnects focuses on vertical interconnects (vias) [10]-[13], while growing long length horizontal CNT interconnects remains challenging. The demonstration of CNT bundle growth in a horizontal direction uses the fact that CNT bundles always tend to grow perpendicular to a surface [14]. The orientation of nanotubes is directly controlled by the direction of gas flow in the CVD system [15]. The substrate needs to be rotated to get different orientation of the CNTs. Other approaches like electric field induced alignment [16] or fluidic methods are not suited for large scale integration [17].

TABLE I. Comparison of properties among Cu, SWCNT, and MWCNT.

	Cu	SWCNT	MWCNT
Max. current density (A/cm ²)	<1x10 ⁷	>1x10 ⁹ [5]	
Thermal conductivity (W/mK)	385	5800 [6]	3000 [7]
Mean free path (nm) @ 300K	40	>1000 [8]	>25000 [9]*

* MFP of MWCNTs depends on their diameters. The value shown here is for the MWCNT with outmost shell diameter of 100 nm.

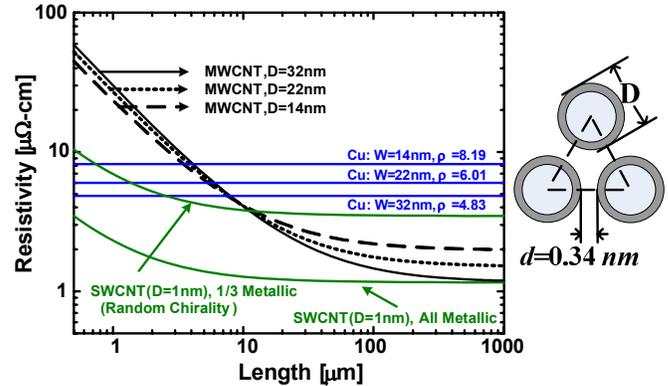


Fig. 1. Comparison of resistivity among MWCNTs with various diameters, Cu wires with different dimensions, and SWCNT bundles with different chiralities. Dimension of Cu wires are adopted from ITRS. SWCNT bundles are assumed to be densely packed (interval is 0.34 nm as shown alongside).

Until recently it has been difficult to grow dense bundles of SWCNTs because the fertility of the catalyst particles for SWCNT growth was low. Although 84% catalyst activity has been reported in [18], the grown SWCNT bundle is very sparse, only occupying 3.6% of the total volume. Moreover, the lack of control on chirality means that it is difficult to ensure that the SWCNTs forming a bundle are all metallic. Although 87% metallic SWCNT bundle has been reported [19], it is not suitable for large scale integration and the density of bundle after separation is quite low.

Since it is very challenging to obtain densely packed bundles of metallic SWCNTs, all of the CNT bundle fabrication work has been focused on MWCNTs which can guarantee metallic behavior. Two

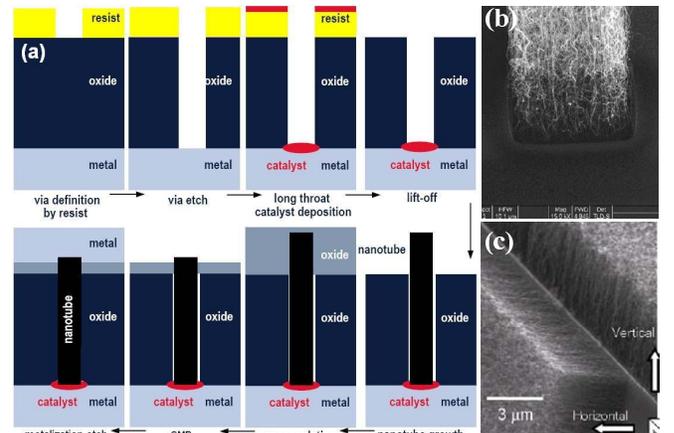


Fig. 2. (a) Process sequence for CNT vias. (b) The first CNT via by Kreupl et al., [11]. (c) Vertical and horizontal CNT bundles from Fujitsu [12].

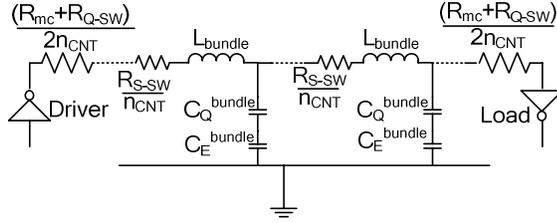


Fig. 3. Equivalent circuit model for SWCNT bundle interconnects.

different approaches to integrate CNTs have been investigated. Li *et al.* [10] have proposed a “bottom-up” approach. One drawback of this approach is that the fibers do not always grow at the selected location and are sometimes shifted and tilted from the projected locations. The more conventional approach of etching the vias down to metal layer one and growing the CNTs in these vias has been pursued by semiconductor companies and results have been presented by Kreupl *et al.* (Infineon) [11], Nihei *et al.* (Fujitsu) [12], and Choi *et al.* (Samsung) [13]. Schematic of the process sequence and some TEM pictures are shown in Fig. 2. In [12], using size-controlled catalyst nanoparticle deposition technique, the diameter of nanotube has been well controlled and the density of CNTs achieved has been as high as $9 \times 10^{11}/\text{cm}^2$. Most recently, low temperature (365°C) growth has been achieved for on-chip CNT vias [20]. It has been shown that at low temperatures, ultra low-k dielectric ($k=2.6$) can be used in via structures without apparent damage. Growing well aligned high aspect ratio CNT bundle (length $> 100 \mu\text{m}$) has also been demonstrated in [21], which could possibly be used as through-wafer vias in 3D ICs. In addition, progress has also been recently reported on the densification of CNT bundles [22], which can increase CNT density by 5~25 times.

3. Modeling and Analysis of SWCNT Interconnects

Burke [23] has applied Luttinger liquid theory to obtain the circuit model of ballistic individual CNTs. Subsequently, several works have investigated the modeling and performance of SWCNT bundles for interconnect applications [24]-[26]. For each conducting channel in a CNT (each conducting channel has 2 modes due to spin degeneracy), quantum resistance $R_Q = h/2e^2 = 12.9 \text{ K}\Omega$, kinetic inductance $L_K = h/4e^2v_F = 8 \text{ nH}/\mu\text{m}$, quantum capacitance $C_Q = 4e^2/hv_F = 194 \text{ aF}/\mu\text{m}$, where h is the Planck’s constant, e is the elementary charge, and v_F is the Fermi-velocity of CNTs. Scattering induced resistance per unit length $R_S = R_Q/\lambda$, where λ is the MFP of CNT ($\lambda \sim 1 \mu\text{m}$ for SWCNT). Another important parasitic parameter is the imperfect contact resistance (R_{mc}) between CNT and metal, which depends on nanotube diameter, process technique and some other factors. Laboratory experiments [9, 12] have recently demonstrated that R_{mc} could be very small compared to the total resistance.

Fig. 3 shows the circuit model of SWCNT bundle (each SWCNT has 2 channels due to lattice degeneracy, hence, total of 4 conduction modes). Since all SWCNTs are in parallel in the bundle, the total resistance of SWCNT bundle can be given by

$$R_{\text{bundle}} = (R_{mc} + R_{Q-SW} + R_{S-SW} \cdot l) / n_{\text{CNT}} \quad (1)$$

where n_{CNT} is the number of CNTs in the bundle, l is the length of CNT bundle. R_{Q-SW} and R_{S-SW} ($= R_{Q-SW}/\lambda$) are the quantum and scattering resistance of each SWCNT, respectively.

Similarly, the effective quantum capacitance of a SWCNT bundle is given by $C_Q^{\text{bundle}} = n_{\text{CNT}} \cdot C_{Q-SW}$. The electrostatic capacitances of SWCNT bundle depend on the geometry of the bundles and interconnect structures. Considering the structure shown in Fig. 4(b), we applied the full 3-D simulator FastCap [27] to calculate electrostatic capacitance. Fig. 4(c) shows the comparison between CNT bundles and Cu wires of realistic dimensions below the 22 nm technology node. In the case of maximally dense bundles, the CNT bundle electrostatic capacitance is still found to be around 6% lower

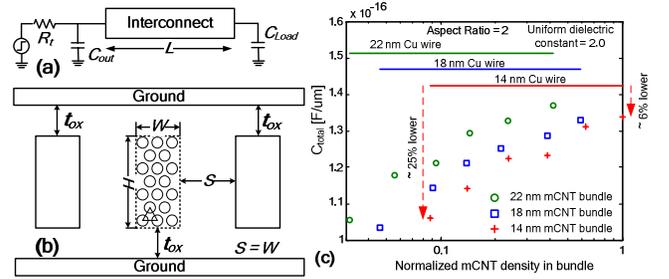


Fig. 4. (a) Schematic of circuit used for performance evaluation. (b) Cross-section of typical interconnect configuration in advanced IC designs. (c) Total electrostatic capacitance of realistic dimension SWCNT bundles at different technology nodes as a function of bundle density.

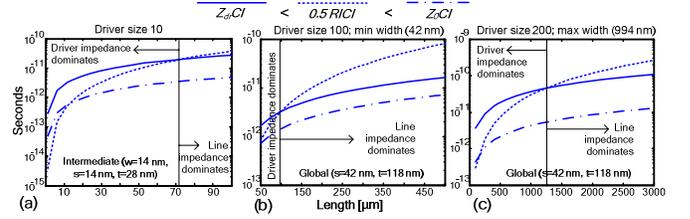


Fig. 5: Comparison of contribution to delay from different components of impedance (driver, line and characteristic impedance) as a function of CNT bundle line length at (a) intermediate and (b-c) global interconnect levels, at 14 nm technology node. Here ‘w’ and ‘t’ are wire width and thickness, respectively. ‘s’ is spacing between adjacent interconnects.

than that of Cu. However, as the m-CNT density is reduced (assuming uniform distribution of metallic CNTs in the bundle) the capacitance becomes significantly lower than that of Cu interconnects. In the following delay analysis of interconnects, we will use Cu wire capacitance which provides an upper bound for dense CNT bundle capacitance.

Before we discuss the inductance model of a CNT bundle, the importance of considering inductance in interconnect delay is analyzed. Following the methodology in [28], it can be shown that R - C -only model becomes inaccurate and inclusion of inductance becomes necessary if the following inequality is satisfied

$$Z_{dr}Cl < 0.5RCl < Z_0Cl \quad (3)$$

where Z_{dr} is the driver impedance, R , C and L are the per unit length interconnect resistance, capacitance and inductance, respectively, l is the interconnect length and $Z_0 = \sqrt{L/C}$ is the characteristic impedance of the interconnect. Fig. 5 plots the three terms in the inequality (3) for different CNT bundle interconnect geometries. It is observed that inequality (3) is never satisfied. Hence, it is reasonable to assume that simple RC circuits (ignoring line inductance) will suffice to model most CNT bundle interconnects. Hence, in the following delay performance analysis of SWCNT bundle, we use RC circuit rather than RLC . The accurate inductance model of CNT bundle will be discussed in the next section of high-frequency analysis.

Studies in [24]-[26] have shown that dense CNT bundle interconnects can easily outperform Cu at the global level, while the propagation delay of CNT bundle at local level is nearly the same as that of Cu wires. In order to outperform Cu at short local interconnect, monolayer CNT structure has been proposed in [26]. It is claimed that

TABLE II: RESISTANCE FOR DIFFERENT DRIVER SIZES, CU WIRE AND MONOLAYER CNTS WITH DIFFERENT LENGTHS AT 22 NM NODE.

R_{dr} (Ω) (driver size)	16810 (minimum size)	1681 (10 \times minimum size)			
Length (μm)	2	8	12	16	20
Cu Resistance (Ω)	124.2	496.8	745.2	993.6	1242
Monolayer-CNT Resistance (Ω) 10 m-CNTs, $MFP = 1 \mu\text{m}$	1290	5160	7740	10320	12900

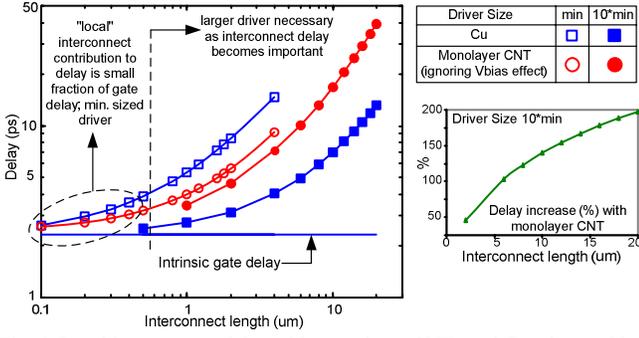


Fig. 6. Local interconnect delay with monolayer CNTs and Cu wires at 22 nm node, as a function of interconnect length, with minimum sized drivers (hollow symbols) and drivers of size = 10×minimum (solid symbols). Dotted lines identify roughly the regions where minimum sized drivers and larger (size = 10×minimum) drivers should be used. Percent increase in delay with monolayer CNTs for driver size = 10 × minimum and interconnect lengths 2-20 μm is shown alongside.

monolayer CNT can provide better performance than Cu for interconnects as long as 2-20 μm at the 22 nm node. Table II shows the driver resistance for two different driver sizes, and the Cu interconnect resistances as well as monolayer CNT interconnects at the 22 nm node. It is evident from Table II that although Cu interconnect resistance is small compared to driver resistance for several micron lengths, this is not true for monolayer CNT interconnects *unless* the driver is minimum-sized. Fig. 6 shows a comparison between Cu and monolayer CNT local interconnect delays for two different driver sizes (with a fanout of four identical gates). For minimum-sized drivers (hollow symbols), monolayer CNTs have lower delay than Cu because of the significantly lower capacitance. However, minimum-sized drivers can only be used when interconnect delay is a small fraction of the intrinsic gate delay. It is observed that at about 1 μm length, the interconnect contribution to delay becomes equal to the intrinsic gate delay. At such lengths it is necessary to use larger drivers. There is a clear reduction in delay with driver size 10 times the minimum (solid symbols). However, in this case the large resistance of monolayer CNTs increases delay by 100-200% as compared to Cu, in spite of the lower capacitance.

4. Modeling and Analysis of MWCNT Interconnects

As we discussed in Section 2, most of the CNT interconnect fabrication work focuses on MWCNTs, however, few modeling efforts have addressed MWCNT interconnect modeling. Our recent work [29] has comprehensively investigated the modeling and performance analysis of MWCNT interconnects.

The number of conducting channel of each shell can be obtained approximately [30] by

$$N_{shell}(D) \approx aD + b, \quad D > 3 \text{ nm} \quad (4)$$

where D is the diameter of the shell, $a = 0.0612 \text{ nm}^{-1}$, and $b = 0.425$. Similar to SWCNT, the resistance, kinetic inductance and quantum capacitance of each shell can be given by

$$R_{shell} = (R_Q + R_S l / \lambda) / (a \cdot D + b) \quad (5a)$$

$$L_{K/shell} = L_K / (a \cdot D + b) \quad (5b)$$

$$C_{Q/shell} = C_Q (a \cdot D + b) \quad (5c)$$

Combining all shells together, we have proposed the MWCNT circuit model as shown in Fig. 7. It is important to note that there are tunneling conductance, mutual inductance and shell-to-shell capacitance between shells. Detailed discussion of this model can be found in [29]. Note that there is only one total ground capacitance C_E in the model in Fig. 7. This is because only the outermost shell has electrostatic interaction with the ground, while others are shielded.

Based on the equivalent circuit model, the performance of MWCNT

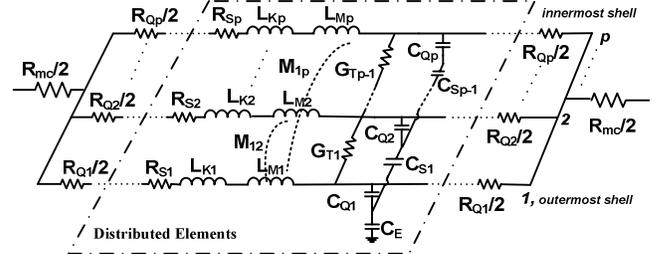


Fig. 7. The equivalent distributed circuit model of a MWCNT with p shells. Besides the lumped imperfect contact resistance R_{mc} and lumped quantum resistance R_Q per shell, each distributed cell has scattering resistance R_S , kinetic inductance L_K , magnetic inductance L_M , mutual inductance M and quantum capacitance C_Q . Only the outermost shell has electrostatic capacitance C_E with the ground. The shell-to-shell capacitance, C_S , and the tunneling conductance, G_T , only have $p-1$ distributed components for the entire MWCNT [29].

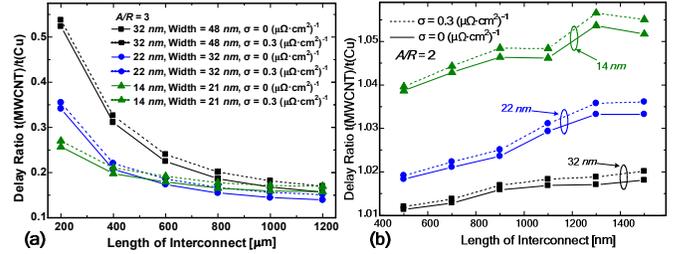


Fig. 8. Signal delay ratios of MWCNT interconnect to Cu interconnect at the (a) global, (b) local level interconnects [29].

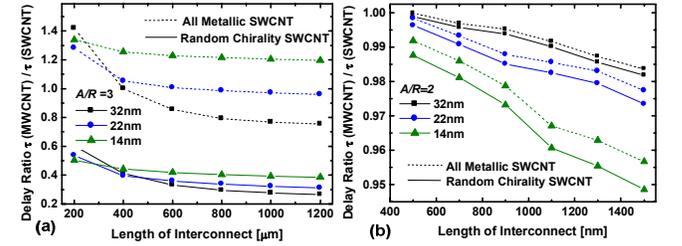


Fig. 9. Signal delay ratios of MWCNT to SWCNT interconnect at (a) global, (b) local level for 32 nm, 22 nm, 14 nm technology nodes, respectively [29].

interconnect can be analyzed. The comparison of delay between MWCNT and Cu interconnects at the global level is shown in Fig. 8(a). It can be observed that the delay of MWCNT interconnects is smaller than that of Cu interconnects and this improvement increases for longer lengths. This indicates that MWCNT can improve the circuit performance significantly in future interconnect applications. Fig. 8(b) shows the comparison of signal delay between local level MWCNT and Cu interconnects. Unlike the case of global level, the delay of MWCNT interconnects at the local level is marginally larger than that of Cu (by ~ 1-6%).

It is also important to investigate how SWCNT and MWCNT compare with each other. This is due to the fact that at present, several fabrication challenges need to be overcome for densely-packed near-100% metallic SWCNT bundles. Two cases of SWCNT bundles are examined: 1) all the SWCNTs in the bundles are metallic; 2) the SWCNTs in bundles have random chiralities, that is only 1/3 of the SWCNTs are metallic. Fig. 9(a) shows the delay comparison between MWCNT and SWCNT bundle interconnect at the global level. It is found that the chiralities of SWCNTs in the bundle has significant effect on the interconnect performance. If the SWCNTs are all metallic, SWCNT interconnects can outperform MWCNT at highly scaled technologies (such as in 14 nm technology node). However, if the SWCNTs have random chiralities, the MWCNT interconnect can achieve much better performance than that of SWCNT bundles. For local interconnects, the comparison between MWCNT and SWCNT

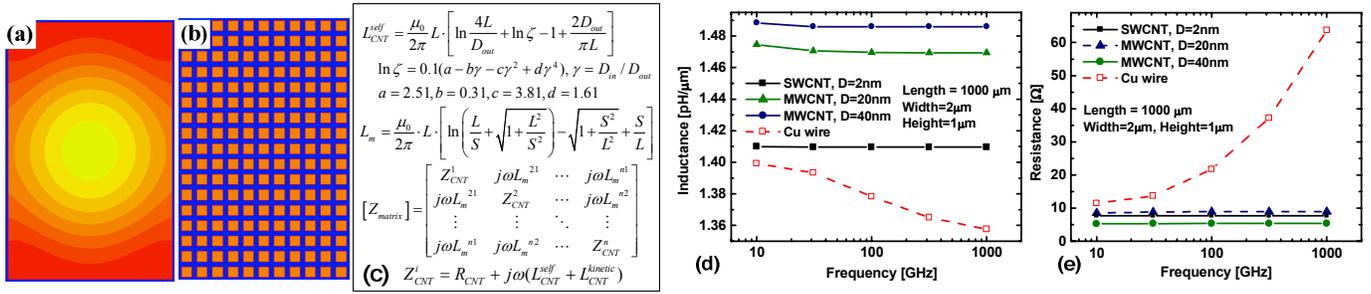


Fig. 10. (a) Current density distribution at 100 GHz of (a) single solid 500 nm × 320 nm cross-section interconnect, and (b) discrete conductor (each 20 nm square cross-section, 10 nm interval) using electromagnetic field solver Maxwell [33]. Both of them have identical “equivalent conductivity”, and identical current density is applied. Color coding in the two cases is identical. (c) Equations of inductance model. L_{CNT}^{self} and L_m are magnetic self- and mutual- inductance of each CNT. Z_{matrix} is the impedance matrix of CNT bundle. Effective total (d) inductance, and (e) resistance of SWCNT and MWCNT bundles, and Cu interconnects as a function of frequency for the same dimension.

interconnects is shown in Fig. 9(b). Unlike global interconnects, the chiralities of SWCNTs in bundles have little effect on their performance. When the chiralities of SWCNTs are changed from all metallic to random, the delay ratios change by only < 5%. To summarize, in order for SWCNT bundles to be competitive (or better) with respect to MWCNT interconnects, dense SWCNT bundles with high metallic fraction are necessary.

5. Electro-thermal Analysis of CNT Vias

In addition to electrical performance, the thermal and reliability analysis of CNT interconnect was performed in [25]. It was shown that high thermal conductivity of CNTs can potentially improve thermal and reliability performance significantly. More specifically, [31] has investigated electrothermal performance of CNT vias, where reliability is a more critical issue. It provides insight into the intrinsic properties of CNTs and those of CNT-metal interfaces that must be carefully engineered to derive maximum benefit from CNT vias. It is shown that MWCNT vias, which are currently being fabricated, cannot match the electrical and thermal performance of Cu or SWCNT vias for nanometer geometries. Dense SWCNT bundles with small diameter and good contact (both thermal and electrical) between CNT and metal are needed for via applications.

6. Inductance Modeling and High-Frequency Analysis

For high-frequency analysis, inductance will play a critical role. The only existing method for calculating magnetic inductance of CNT bundle is the “equivalent conductivity model” proposed in [32]. However, there are several fundamental issues that need to be justified in that model. First, in that model, each carbon nanotube is treated as a solid square metallic conductor rather than realistic hollow cylinder structure. Second, the realistic CNT bundle with discrete conductors is replaced by a single identical dimension solid conductor with an equivalent conductivity. As shown in Fig. 10, there could be very large differences in current distribution between the bundle structure and a single solid conductor, which indicates that the model is fundamentally incorrect. Third, the model does not consider the impact of kinetic inductance when calculating magnetic inductance. As will be shown later in this section, kinetic inductance strongly affects the current redistribution and, in turn, affects the magnetic inductance significantly.

In order to address the issues discussed above, we have developed accurate inductance models for both SWCNT and MWCNT bundles [34]. The realistic hollow cylinder structure of CNTs and the discrete bundle structure have been taken into account. Kinetic inductance is also taken into account. The model allows accurate estimation and deeper understanding of inductive effects in high-frequency CNT interconnect analysis.

Based on the equations in [35], both self- and mutual- inductance

model of individual SWCNT and MWCNT have been derived as shown in Fig. 10 (c). Thereby, the impedance matrix of CNT bundle can be obtained (also shown in Fig. 10(c)). Note that the self-impedance of each nanotube consists of resistance and inductive reactance (both kinetic and magnetic). Once the impedance matrix is obtained, the effective total impedance (effective resistance and inductance) of CNT bundle can be calculated.

Fig 10 (d) and (e) shows the total inductance and resistance of SWCNT, MWCNT, and Cu interconnects as a function of frequency. It can be observed that the inductance of Cu decreases with increasing frequency while the resistance of Cu increases at high frequencies. This can be explained by the current redistribution (i.e. skin effect) at high frequencies. At 100 GHz, the skin depth of a Cu is about 250 nm, which implies that the skin effect is significant for cross-sections of ~ 1 μm. It can also be observed that the value of inductance of CNT interconnect is larger than that of Cu wire. This is because of the presence of large kinetic inductance. In addition, due to the presence of large kinetic inductance component in the self-impedance terms (diagonal elements in the impedance matrix) as shown in Fig.10(c), the self-impedance of each CNT is always much larger than the mutual impedance component ($j\omega L_m$), which restrains the current redistribution. As a result, the resistance and inductance of CNT bundle almost remains unchanged with frequency as shown in Fig. 10(d) and (e), respectively. Hence, it can be concluded that both SWCNT and MWCNT interconnects have negligible skin effect, which is very attractive for high-frequency applications including inductor design in high-performance analog/RF circuits.

7. CNT Chip-to-Packaging Interconnects

Besides on-chip interconnect application, CNTs can also be used as chip-to-packaging interconnects. The properties of CNTs, such as high current carrying capacity, high thermal conductivity and mechanical strength, are highly favorable for packaging applications. In addition, CNTs can provide fine form factor which is also preferable for small size of future I/O pads. Utilizing CNTs as flip-chip bumps for the packaging of high power amplifiers (HPA) has been demonstrated (by Fujitsu) in [36], as schematically shown in Fig.11. CNT bumps not only provide electrical interconnection for drain, source, and gate, but also provide thermal dissipation path for heat source (HPA). Thermal conductivity of CNTs was achieved to be as high as 1400 W/mK. Because of this high thermal conductivity, the flip-chip structure can be successfully fabricated without degrading thermal performance. In the mean time, because of the absence of long wire bondings, flip-chip structure has less parasitic inductance; therefore, it achieves better high-frequency performance as demonstrated in [36]. A low temperature approach for CNT soldering for packaging has been proposed in [37]. This approach first employs high quality open-ended CNT growth at high temperature (775°C), followed by CNT adhesion onto the substrate at low temperature (270°C), which is compatible with microelectronic back-end process. This process could overcome

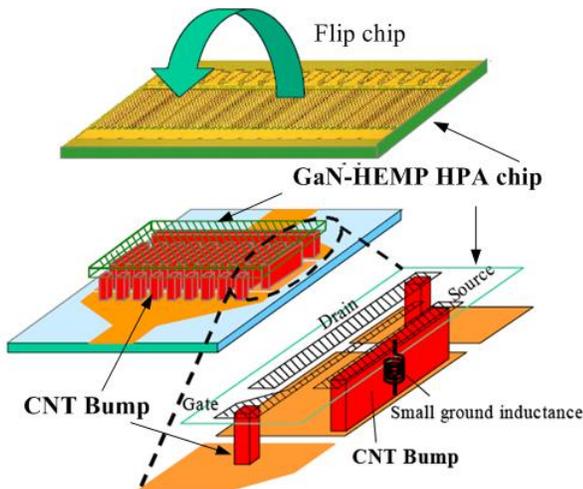


Fig. 11. Schematic diagram of flip-chip high power amplifier (HPA) packaging employing CNT bumps [36]. CNT bumps provide both electrical and thermal interconnections for HPA heat source.

the serious obstacles of integration of CNTs into integrated circuits and microelectronic device packages by offering low process temperatures and improved adhesion of CNTs to the substrates. Several works have also studied using CNT as Thermal Interface Materials (TIM) for packaging [38] and have demonstrated that using CNTs can provide lower thermal resistance. Recently, patterned CNTs have been used as heat spreader for chip cooling [39]. By soldering CNT arrays on to the back side of chips as heat spreader, chip packages can not only achieve fairly equal thermal performance compared to Cu cooling structure but can also provide light-weight, mechanically-stiff cooling system.

8. CNT Interconnect Process Variation

Sustained efforts for developing processes geared towards the large-scale, CMOS compatible, fabrication of CNT based interconnects have yielded promising results. Of particular note are the consistent improvements reported in the fabrication of CNT based vias compatible with CMOS technologies [12], [20]. However, as expected with all nano-scale technologies, CNT interconnects will also encounter significant process variation challenges. These can arise from several sources - variation in the population of metallic CNTs in a bundle, variations in the diameter and spacing of individual CNTs, contacts to metal, defects along the nanotubes, temperature effects, etc.

While there are some preliminary studies on the impact of process variations in CNT interconnects [40], there is a need for a realistic understanding of the sources of variation which is in tune with state-of-the-art CNT interconnect fabrication processes. As an example, traditionally used processes for the fabrication of bulk CNT samples exhibit large variations in CNT diameters. However, such processes as arc discharge or laser ablation are clearly not suitable for large-scale integration with CMOS. On the other hand, processes that have been demonstrated as compatible with CMOS interconnects - low temperature CVD growth from pattern deposited catalysts - have shown excellent control on parameters such as CNT diameter. Modeling efforts to comprehend the relevant process variation challenges in CNT interconnects are as important as developing robust processes that minimize variations.

9. Summary

The current status of CNT interconnect research, from both fabrication and modeling perspectives, has been reviewed in this paper. State-of-the-art in both SWCNT and MWCNT modeling and performance analysis are presented. It is shown that in order for SWCNT bundles to outperform MWCNT interconnects, dense and high metallic-fraction SWCNT bundles are necessary. On the other hand, since MWCNTs are easier to fabricate with less concern about

the chirality and density control, they can be attractive for immediate use as horizontal wires in VLSI, including local, intermediate and global level interconnects. A comprehensive analysis of high-frequency effects in SWCNT and MWCNT bundle structures has been performed. It is shown that due to the presence of large kinetic inductance, the current redistribution in a CNT bundle is negligible even at large cross-sections and very high frequencies. This unique characteristic of CNT bundle is very important and promising for future high-frequency interconnect applications including inductor design in high-performance analog/RF circuits. In addition, because of very good electrical and thermal properties, CNTs are also very promising for various chip-to-packaging interconnect applications.

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