A New Analytical Thermal Model for Multilevel ULSI Interconnects Incorporating Via Effect

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Abstract

This paper presents a compact analytical model for estimating the temperature rise of multilevel ULSI interconnects incorporating via effect. For the first time, an analytical expression is derived for the via correction factor, η, which quantifies the effect of via separation on the effective thermal conductivity of ILD (inter-layer dielectrics), $k_{ILD,effective}$, with $k_{ILD,effective} = k_{ILD}/ k_{ILD,effective}$, where $0<\eta<1$. Both the temperature profile along the metal lines and average temperature rise of the lines can be easily obtained using this analytical model. The predicted temperature profiles are shown to be in excellent agreement with the 3-D finite element thermal simulation results. The model is then applied to estimate the temperature distribution in multi-level interconnects. Significant difference in temperature distribution and maximum temperature rise is observed between the realistic situation of heat dissipation with vias and the overly simplified case that ignores via effect.

Introduction

In advanced ULSI technology, a variety of low-k materials have been introduced to reduce the RC delay, dynamic power consumption and crosstalk noise. Poor thermal conductivity has been a major concern to cause substantial rise in interconnect temperature. The combination of increasing current density, more interconnect levels, and the introduction of low-k ILD's leads to non-negligible interconnect Joule heating. Recent publications have addressed the issue of poor thermal conductivity of low-k dielectrics and their impact on interconnect reliability and performance [1]. However, the effect of vias, which have much higher thermal conductivity than the dielectrics, on the thermal characteristics of interconnects has not been addressed adequately. Consequently, the predicted temperature is much higher than the temperature in practical situation. Recently, we analyzed the thermal effects in interconnects using a lumped circuit simulation approach [2, 3]. In this work, an analytical model based on first principles is developed under steady state conditions and the influence of vias on the temperature profile is evaluated. By defining the via correction factor (η), the via effect can be incorporated into the effective thermal conductivity of ILD, $k_{ILD,effective}$. The conventional thermal equations can, thus, be conveniently used by replacing nominal k_{ILD} by $k_{ILD,effective}$. It is shown that η is highly dependent on via separation. Additionally, a simple heat spreading factor, s, is developed to accommodate the fact that heat can dissipate through larger area than the nominal contact area. The solution of s is validated by 3-D finite element simulation (ANSYS) and shows excellent agreement.

Analytical Model and Assumptions

Consider a rectangular metal wire with thickness H, width w, length L, resistivity ρ and thermal conductivity k_M, separated from the underlying layer by ILD of thickness t_{ILD} and thermal conductivity k_{ILD}. With x-coordinate set to zero at the middle of the wire, the two ends, $x=\pm L/2$, of the wire are connected to the underlying layer through vias. The temperature at the ends of the wire is assumed the same as the underlying layer temperature, T_0, thus $T(\pm L/2)=T_0$. It is further assumed that heat only flows downwards toward silicon substrate which is usually attached to a heat sink. Under steady state conditions, with uniform root-mean-square current, j_{rms}, flowing in the wire, the governing heat equation is

$$\frac{d^2T}{dx^2} - \frac{T-T_0}{L_H^2} = -\frac{\rho j_{rms}^2}{k_M}, \tag{1}$$

where healing length, $$L_H \equiv \left[\frac{k_M H t_{ILD}}{k_{ILD}}\left(\frac{1}{s}\right)\right]^{1/2}, \tag{2}$$

and heat spreading factor, $s \equiv w_{effective}/w$. (3)

The $w_{effective}$ is used to represent the deviations from one-dimensional heat flow. It can be thought that within the range of thermal healing length, L_H, from vias, heat generated will flow through vias to the underlying layer. Beyond L_H, heat will flow through ILD and the via effect is diminished. The heat spreading factor, s, is employed to correct the deviation from 1-D heat flow between metal wire and underlying layer.

The temperature along the wire can then be solved as

$$T(x) = T_0 + \Delta T_{Max}\left(1 - \frac{\cosh(x/L_H)}{\cosh(L/2L_H)}\right), \quad -L/2 \le x \le L/2 \tag{4}$$

where $\Delta T_{Max}(=j_{rms}^2 \rho L_H^2/k_M)$ is the temperature rise in the wire when via effect is ignored. T(0) is the temperature at the middle of the wire (x=0) which represents the maximum temperature in the metal. It should be noted that the resistivity used in this work is assumed to be a constant at $\rho(T_{Die})$ to a first order approximation. Simulations based on temperature dependent $\rho(T)$ and fixed value $\rho(T_{Die})$ were carried out for several conditions and the difference in temperature rise was found to be small. Meanwhile, the much less complex expression as shown in (2) could provide more insight for design guidance. A similar derivation

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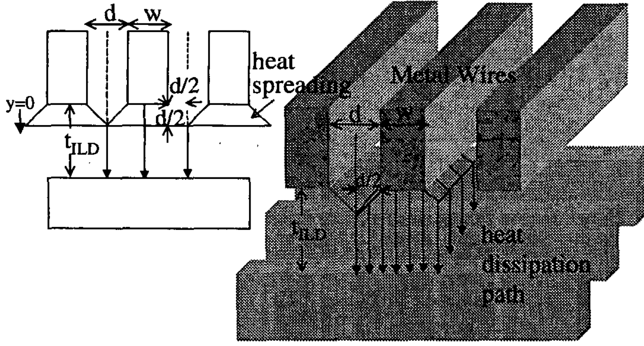

Figure 1. Geometry used to calculate R_{ILD} and spreading factor s. Cross-section view is shown at the upper left corner. Space between two wires are shared for heat dissipation.

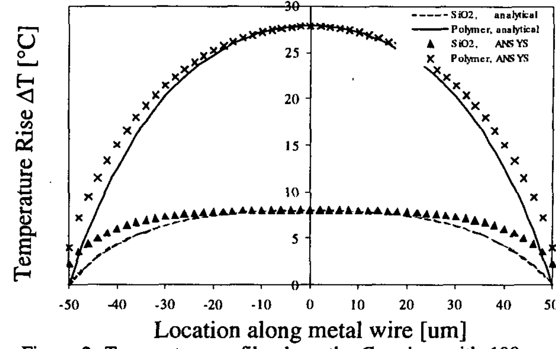

Figure 2. Temperature profile along the Cu wires with 100 µm via separation. $H = t_{ILD} = 0.8$ µm, $w = d = 0.3$ µm, quoted from ITRS [6] 0.1 µm node for global interconnects.

including linear temperature dependent resistivity can be found in [4].

The commonly used Bilotti's equation [5] is not adopted in this work to account for the deviations from 1-D heat flow. This is due to the fact that it assumes a single heat source, whereas, in typical IC layout, there are multiple heat sources due to parallel metal wire array. A new expression of heat spreading factor, s, is therefore derived here. For the worst case analysis, all metal wires are assumed to carry the maximum RMS current density and separated by spacing d. As shown in Figure 1, the Joule heat transfers downward as well as spreads laterally in the ILD. Assuming the lateral spreading to increase linearly with vertical coordinate, the spreading thermal resistance, R_{spr}, can be derived as

$$R_{spr} = \int_0^{d/2} \frac{1}{k_{ILD}} \frac{dy}{w+2y} = \frac{1}{2k_{ILD}} \ln\left(\frac{w+d}{w}\right). \quad (5)$$

Then, the total thermal resistance of ILD, R_{ILD}, can be calculated by combing the spreading resistance with the volume resistance,

$$R_{ILD} = \frac{1}{2k_{ILD}} \ln\left(\frac{w+d}{d}\right) + \frac{1}{k_{ILD}} \frac{t_{ILD} - d/2}{w+d}. \quad (6)$$

On the other hand, R_{ILD} can be also expressed as

$$R_{ILD} = \frac{t_{ILD}}{k_{ILD} w_{effective}} = \frac{t_{ILD}}{k_{ILD} ws}. \quad (7)$$

By comparing (6) and (7), s, can be obtained as

$$s = \left(\frac{w}{t_{ILD}} \frac{1}{2} \left(\frac{w+d}{w}\right) + \frac{w}{t_{ILD}} \frac{t_{ILD} - d/2}{w+d} \right)^{-1}. \quad (8)$$

After the s factor is installed in (2), effect of the via separation and heat spreading on the temperature profile along metal wire can be captured completely by (4). As can be observed form Figure 2, the result from analytical expression is shown to be within 5% agreement with the 3-D finite element thermal simulation using ANSYS.

Impact of Via Separation on Effective k_{ild}

It should be noted that as predicted from (2) and validated from Figure 2, the thermal healing length, L_H, in the wire is longer if ILD has lower thermal conductivity, ($k_{polymer}$ = 0.3 W/mK v.s. k_{oxide} =1.2 W/mK). Consequently, via effect is more important for the low-k insulators. For the first time, an analytical expression of $k_{ILD,eff}$ incorporating via effect is derived here. ΔT_{ave} is defined as the average temperature rise in one metal layer and it can be expressed as

$$\Delta T_{ave} = q * R_{th} = j_{rms}^2 \rho \frac{Ht_{ILD}}{k_{ILD,eff}}. \quad (9)$$

On the other hand, ΔT_{ave} can also be obtained from (4) as

$$\Delta T_{ave} = \frac{1}{L} \int_{-L/2}^{L/2} \left(T(x) - T_0\right) dx \quad (10)$$

$$= j_{rms}^2 \rho \frac{Ht_{ILD}}{k_{ILD}} \left[1 - \frac{\tanh\left(\frac{L/2}{L_H}\right)}{\frac{L/2}{L_H}} \right]. \quad (11)$$

Comparing (9) and (11), via correction factor, η, can be deduced as

$$\eta = 1 - \frac{\tanh\left(\frac{L/2}{L_H}\right)}{\frac{L/2}{L_H}}, \quad 0 \le \eta \le 1 \quad (12)$$

and

$$k_{ILD,eff} = k_{ILD} * \frac{1}{\eta}. \quad (13)$$

The $k_{ILD,eff}$ is then plotted against via separation in Figure 3 for three different ILD materials. The geometries of interconnect structure is taken from ITRS [6] 0.1 µm technology node for global wires. It can be observed that incorporation of via effect results in increased $k_{ILD,eff}$ especially for ILD materials with lower nominal thermal

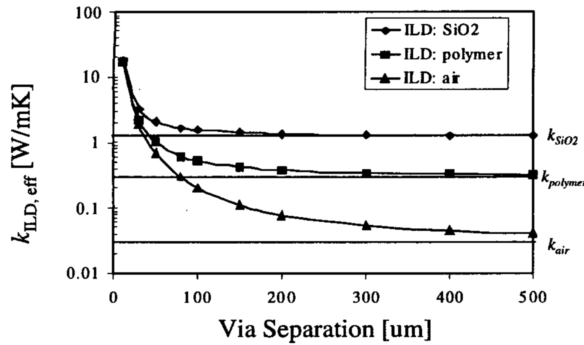

Figure 3. Effective ILD thermal conductivity increases with shorter via separation. The lower the nominal k_{ILD}, the longer the L_H, hence stronger via effect.

conductivity. This fact can explain why the interconnect temperature is not as high as commonly assumed when low-k ILD is implemented in the advanced interconnect structure.

Temperature in Multilevel Metal Layers

Generally, Joule heat generated in metal wires is considered to dissipate only through the heat sink attached to the Si substrate. Therefore, all the heat generated in the upper metal levels has to transfer through the lower metal levels to substrate. With $\Delta T_{i-1,\ i}$ defined as the average temperature rise between metal layers *i-1* and *i*, the temperature rise at the top layer for an N-level metal interconnect can be obtained as

$$\Delta T_N = T_N - T_{substrate} = \sum_{i=1}^{N} \Delta T_{i-1,i} = \sum_{i=1}^{N} q_i * R_{th,i} \quad (14)$$

$$\cong \sum_{i=1}^{N} \frac{t_{ILD,i}}{k_{ILD,i}} \eta_i \sum_{j=i}^{N} j_{rms}^2 \rho H_j . \quad (15)$$

For the case when via effect is neglected, η_i is set to be 1. As can been seen from (15), there is more heat flowing through lower levels since q_i represents the sum of all the heat generated from i_{th} layer to N_{th} layer. As a result, substantial temperature rise will occur in local wires if the effect of the dense via population is not taken into account. For the purpose of demonstration of the importance of via effect, some reasonable values of via separation are assigned to each of the 8 metal layers and polymer is used as ILD for the 0.1 μm technology node. In addition, a worst case current density, j_{rms}, of 1.4e6 A/cm^2 is assumed for all wires. First, as shown in Fig. 4, the overall temperature rise is much lower with the help of vias. Second, it can be observed that the temperature distribution among metal layers is quite different in these two cases. Ignoring via effect results in large temperature jump in the lower layers and then the temperature rise levels off. On the other hand, with via effect considered, there is hardly any temperature rise in the lower levels even when $k_{polymer}$ is only one fourth of k_{oxide}. Most of the temperature rise is attributed to the upper metal layers with long via separation. Therefore, from the thermal design point of views, global interconnects are more problematic. The concern of RC delay in the global wires may get worse with this additional temperature effect.

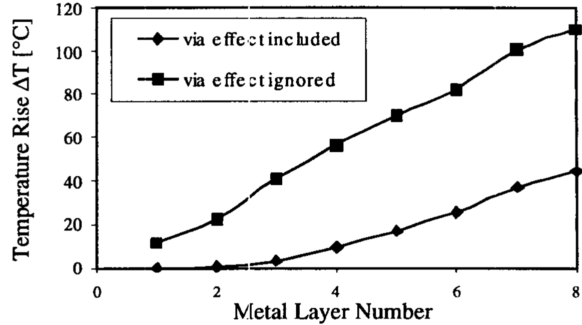

Figure 4. Temperature rise distribution along metal layers from substrate to top metal level. For the case with via effect included, the via separations assigned to the metal layers, from 1st to 8th levels, are 1, 5, 15, 30, 50, 80, 120 and 200 μm respectively.

Summary

In conclusion, a first principle based compact analytical model to evaluate interconnect $k_{ILD,effective}$ under the influence of vias is presented. Both via effect and heat spreading have been taken into account to ensure predictions within 5% agreement with the 3-D finite element thermal simulation (ANSYS) results. Quick evaluation of interconnect temperature rise can then be done by using these expressions. It has been shown that with the help of vias as efficient thermal paths, the $k_{ILD,effective}$'s can be significantly higher than their nominal values if via separation is comparable to L_H. Therefore, the thermal problem associated with low-k insulators is not as bad as it appears. Additionally, global interconnects would suffer much higher temperature rise than local interconnects due to the much longer via separation. Therefore, thermal effect should be evaluated carefully in the global interconnect for reliability as well as speed issues.

Acknowledgment

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