Characterization of VLSI Circuit Interconnect Heating and Failure under ESD Conditions

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Abstract - **The high current and ESD effects on VLSI interconnect metallization have been characterized and a model for heating under ESD conditions is presented. It is shown that thermal breakdown occurs when the resistances increase by a factor of >3.6 due to melting of metal lines. After the metal is molten, the thermal stress is required to exceed the fracture strength of the oxide/nitride layers in order for the overlying dielectric to be cracked and an open circuit to take place. The critical failure current is strongly influenced by the metal thickness and thermal capacity. It is shown that for current pulses below the failure threshold, the metal will return to its original solid state with no change in DC resistance, but it will have a lower electromigration lifetime. This is a potential latent failure. The model is applied to derive relations between critical current, line width and pulse width for determining design guidelines for ESD and I/O buffer interconnects.**

INTRODUCTION

Electrostatic discharge (ESD) is a high current (>1 A), short duration (<200 ns) event which causes irreparable damage to all categories of IC devices. Protection circuits are generally designed to minimize ESD damage. For improving reliability, ESD testing on these circuits is usually done by exposing them to typical discharge pulses to which the IC may be exposed during manufacturing or handling [1- 2].

Metal interconnections in protection circuits are heavily stressed during ESD due to high joule heating. The continuous drive to scale down IC devices for achieving higher circuit density and faster speed have reduced the dimensions of both the devices and the metal lines that form the interconnection system between the devices and also to the power lines in the chip [3]. This reduction in line dimension can increase their susceptibility to ESD damage. Recently, thermally accelerated open circuit metal failure have been observed during ESD testing [4]. It is therefore desirable to characterize heating and subsequent failure of thin AlCu metal lines under ESD conditions to provide guidelines for designing protection circuit and I/O buffer interconnects. This work reports a comprehensive study of metal heating and failure under high current (ESD) stress. A model incorporating the heating of the interconnect and the surrounding oxide under high current pulse conditions is presented. The critical resistance rise due to ESD pulse discharge through the interconnects has been extracted from experiment. A relationship has been derived using the heating model and it has been shown to be useful for interconnect design. Furthermore, a potential reliability hazard in the form of *"latent ESD damage"* has been identified. It can affect the electromigration (EM) performance of these interconnects exposed to ESD pulses during burn-in and final test, thereby reducing the reliability of the integrated circuit.

EXPERIMENTAL

Interconnect System

A quadruple level metallization (QLM) wafer was used in this study. The stacking sequence was Si/~1.4 μm FieldOxide+Dielectric/Metal1/Dielectric/Metal2/Dielectric/ Metal3/Dielectric/Metal 4/~2 μm -Oxide/Nitride. Each metal module were isolated, i.e., they were not stacked vertically on top of each other. The interlevel dielectrics were around 1μm thick. Each metallization level was multilayered with the stacking sequence TiN/AlCu/TiN excepting metal 4 where the AlCu thickness was doubled to 1.2 μm. Also, metal 1 had an extra layer of Ti under the TiN barrier. All the metal lines were 1000 μm X 3 μm standard NIST recommended structures.

Transmission Line Pulsing (TLP) System

ESD usually involves a complex voltage waveform but the basic failure mechanisms and electrical response of a metal line under ESD stress can be reproduced by using a charged transmission line [5-6] that can generate high

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constant current pulses of varying widths (Δt) and heights (I). The circuit used in this study is shown in Fig. 1.

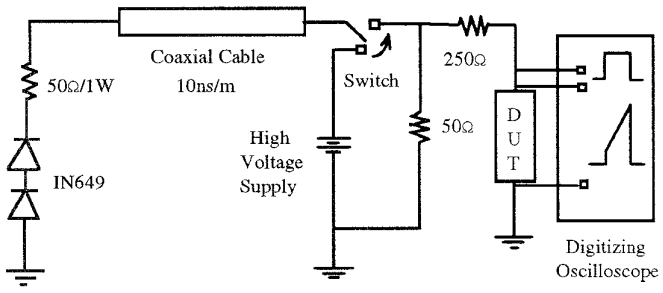

Figure 1. The Transmission line Pulser circuit diagram.

Variation in the voltage used to charge the transmission line was employed to generate current pulses with different amplitudes. Also, four different cable lengths were used for generating various pulse widths. The current pulse (using a current probe) and the instantaneous voltage developed across the device under test (DUT), in this case, metal lines, were captured on a dual channel digitizing oscilloscope.

RESULTS AND DISCUSSION

Interconnect Heating under ESD Stress

Initially the DC joule heating was measured for the QLM wafer under study and the results are shown in Fig. 2. As expected the thermal impedances increased from 150°C/W for metal 1 to about 250°C/W for metal 4. Identical structures

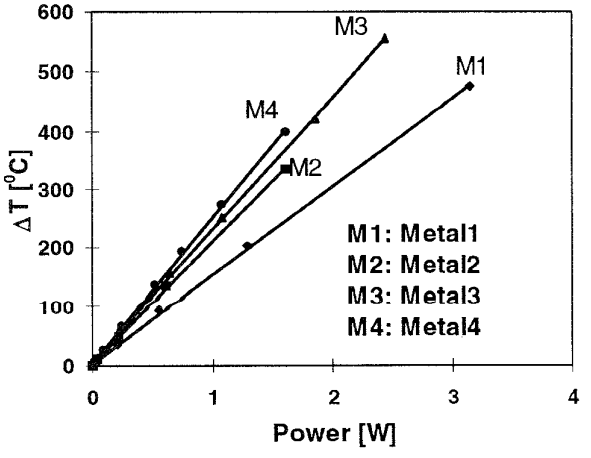

Figure 2. DC current induced self heating in the QLM wafer under study.

from each metal level were then subjected to pulses generated during the discharging of the charged transmission line cable. The voltage, and hence the resistance of the metal lines, increased roughly linearly with time during all the pulsing events even through the phase change to the liquid state, when the metal melts. This result was in agreement with [7] where heating under the Charged Device Model (CDM, a <1 ns event) was analyzed. Figures (3-6) show the maximum resistance rise factor above initial room temperature value, $\Delta R_{max}/R_0$ (henceforth referred to as γ), in the various metallization levels due to stressing by current pulses of different widths (100 ns, 200 ns, 400 ns & 500 ns). By taking the resistivity of the metal to be a linear function of temperature, the corresponding maximum temperature rise ΔT_{max} is also shown along the second y axis. The melting point of 660 ^{0}C which corresponds to γ of ~2.3 is shown by the dashed line in Fig. 3.

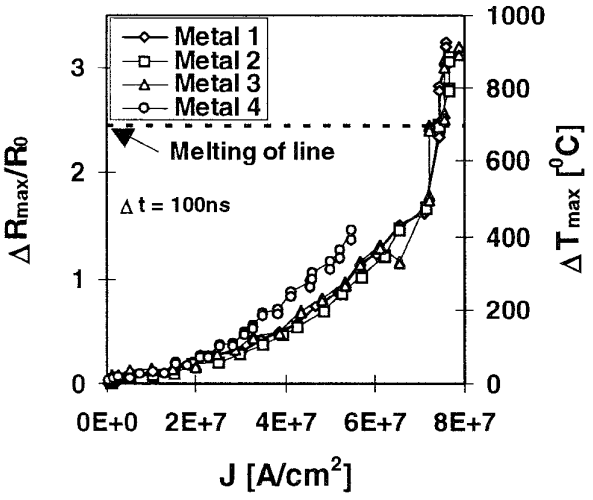

Figure 3. Maximum resistance rise factor, $\Delta R_{max}/R_0 = \gamma$, in metal leads stressed by a 100 ns pulse.

The last data point on each curve corresponds to the highest current value at which there was no open circuit failure. From these figures we can see that metals at all levels with similar dimension have nearly identical values of γ. Therefore the temperature rise of metal 1, 2 and 3 is approximately same. The reason for such behavior stems from the fact that the metal lines exist in a non equilibrium state during the pulsing event since the pulse widths used in this study were much smaller than the time to attain thermal steady state which is typically a few thermal time constants. The thermal time constants of the metal lines used in this study were around 0.8 μs. These thermal time constants were experimentally measured using a Wheatstone's bridge arrangement as described in reference [8]. The nature of

these curves can be understood from the physics of the joule heating of multi level metal lines in IC metallization. The resistance rise factor due to joule heating can be represented by the relationship,

$$\Delta R_{max}/R_0 = \gamma = P \,.\, \theta_j \,.\, TCR \qquad (1)$$

Where, P is the power input in the line, θ_j is the thermal impedance of the line and TCR is the temperature coefficient of resistance. Also,

$$P = J^2 \rho L A \qquad (2)$$

Where, J is the current density in the line, ρ is the resistivity of the metal line, L is the length of the line and A is the cross sectional area of the line.

From equation 1 and 2 it can be seen that metal 1, 2 and 3 should have identical values of γ. This is due to their similar dimensions and due to the fact that the thermal impedance is almost independent of the underlying oxide thickness because of the non steady state of the lines during the pulsing events. Metal 4 however, has nearly twice the cross sectional area and hence the power input is nearly double that of the other metal lines, resulting in a higher value of γ. The results shown in Figs. (3-6) therefore agree with theory. Thus the thickness of the underlying oxide has almost no impact on the value of γ provided the thickness of the line remains constant and the pulse width is shorter than a few thermal time constants such that steady state is not reached.

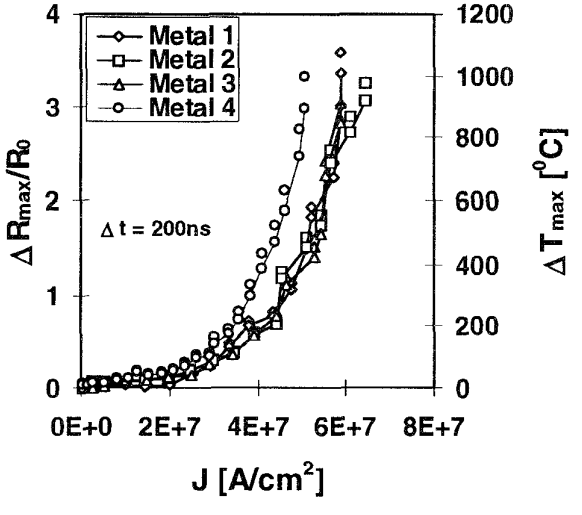

Figure 4. Maximum resistance rise factor, $\Delta R_{max}/R_0 = \gamma$, in metal leads stressed by a 200 ns pulse.

In all cases the γ rises superlinearly with J, the current density in the metal line. Also, all the metal lines fail when γ goes beyond 3.6. This value of γ is therefore identified as the critical resistance rise, γ_{crit}, shortly beyond which all the metal lines fail, thereby creating open circuits.

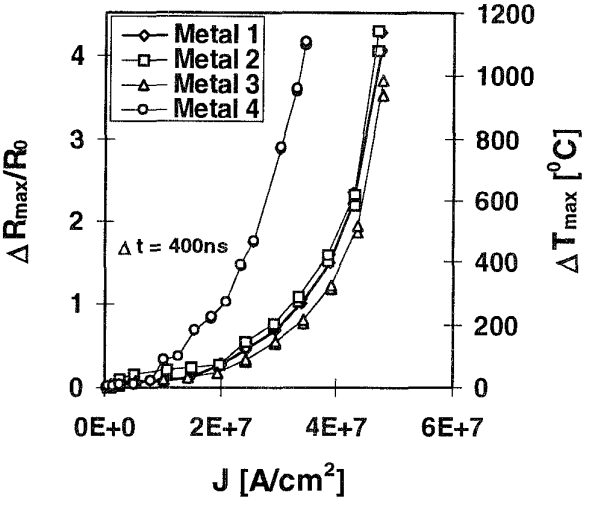

Figure 5. Maximum resistance rise factor, $\Delta R_{max}/R_0 = \gamma$, in metal leads stressed by a 400 ns pulse.

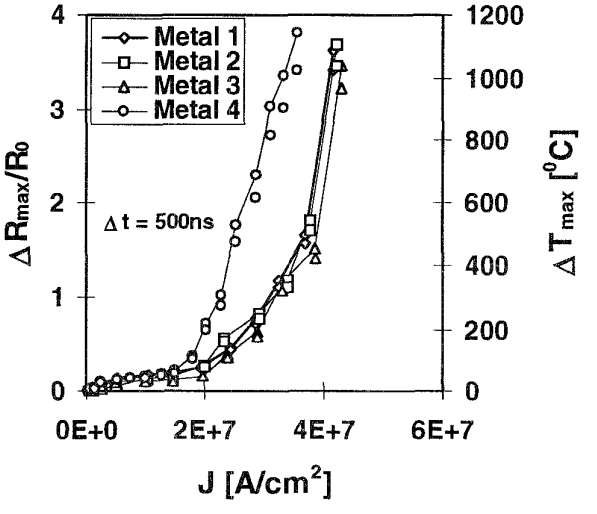

Figure 6. Maximum resistance rise factor, $\Delta R_{max}/R_0 = \gamma$, in metal leads stressed by a 500 ns pulse.

width using a high magnification optical microscope. These pulses however did not break the oxide/nitride layers and hence there was no open circuit failure. Also, the electromigration (EM) lifetime was strongly affected by such pulses indicating that there was melting. This effect is described in the last section of this paper. The final failure of the lines were always accompanied by cracking of the protective oxide/nitride layers. The fracture strength of silicon nitride is around 1 GPa [10]. Hence, the failure caused by the thermal mismatch between the metal and the surrounding dielectric would necessitate a temperature rise well past the melting temperature of 660 ^{0}C [11-12]. At around the failing temperature the thermal stress generated by the mismatch exceeds the fracture strength of the oxide/nitride layers. Therefore all the lines fail when the temperature rises beyond that critical value. At that point the oxide cracks at multiple locations. The optical micrograph of metal 1 and 2 lines blown at multiple spots is shown in Fig. 9. Similar type of multiple failure is observed for metal lines at all different levels. Further, there are no preferential site of failure as expected. Figure 10 shows a magnified view of a failure spot on metal 1 showing the cracking of the overlying layers of oxide.

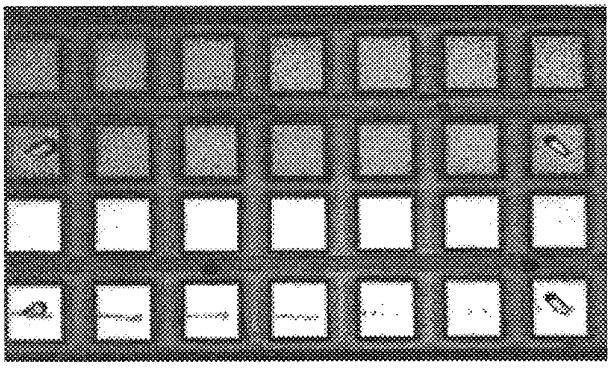

Figure 9. Optical micrograph of metal 1 (bottom) and metal 2 (top) lines blown by ESD pulse showing multiple failure spots.

Interconnect Heating Model

The minimum energy required to melt the given volume of AlCu line (metal 1, 2 & 3) was calculated to be around 8 μJ including the latent heat of fusion. The input pulse energy was calculated using the equation

$$E = \int_0^{\Delta t} I.V dt = \frac{1}{2} I^2.\Delta t.[R_0 + R_f] \qquad (3)$$

Here,
I = current through the metal line,
V = voltage developed across the line,
Δt = pulse width in ns,
R_0 = initial resistance of the unstressed line and
R_f = maximum resistance of line reached during the pulsing event.

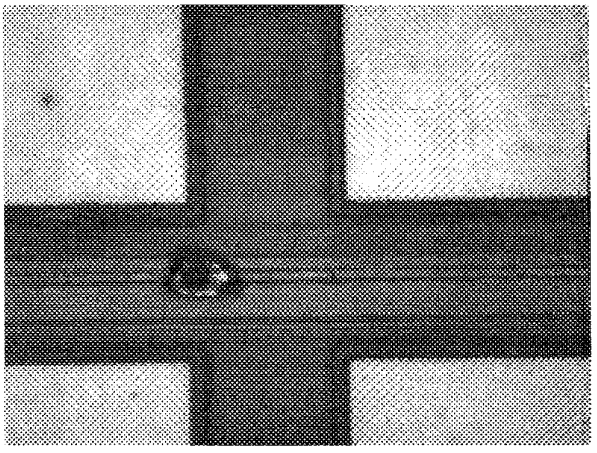

Figure 10. A magnified view of a failure spot on metal 1 showing overlying oxide cracking.

In Fig. 11 the input pulse energy has been plotted against $\Delta R_{max}/R_0$ for a 200 ns pulse for each metal level. It can be seen that the maximum value of $\Delta R_{max}/R_0$ which is γ_{crit}, is approximately same for all levels of metal. Similar results were observed for the 100, 400 & 500 ns pulses. To strengthen this point we have shown a similar result in Fig. 12 for a 500 ns pulse.

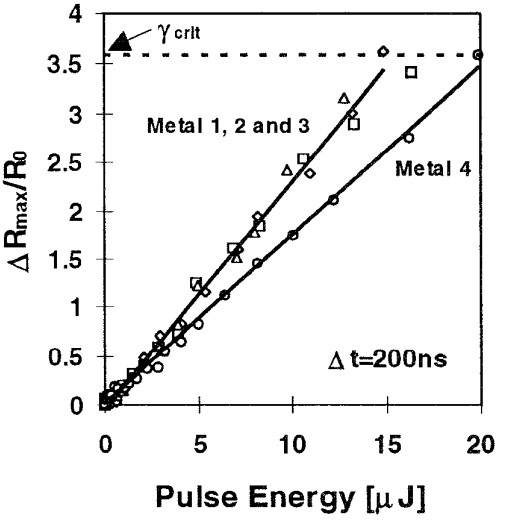

Figure 11. Maximum resistance rise factor, $\Delta R_{max}/R_0 = \gamma$, as a function of pulse energy for a 200 ns pulse.

The corresponding temperature value using the linear model for resistivity rise with temperature would be 1000 ^{0}C. Further, the resistances of all the structures were measured after each pulsing event with a low current pulse. The value of the measuring current was typically 10 mA so that there was no joule heating. The resistance values were always the same as the initial resistance of the metal lines. By doing this we could ensure that the observed rise in resistance is only due to heating of the metal and not due to any form of damage such as cracking or voiding of the lines. From this observation it could be concluded that for current pulses for which the resistance rise is just below the threshold value, the metal does indeed heat up and even melt, but returns to its original solid state with no redistribution of the metal. Some lines were also subjected to a single pulse so that the critical current value was just exceeded. These lines failed instantly, indicating that in our experiments there were no cumulative effects due to pulsing with increasing current until failure.

The DC resistance measured using a Kelvin arrangement before and after pulsing showed little change in the value of the resistance. This was done on two groups of metal lines stressed by high current pulses of two different widths such that the resistance rise was somewhat below the threshold value. However this has a significant impact on the microstructure of the metal lines and hence on the electromigration lifetime of these lines. The effect has been discussed in more detail in the last section of this paper.

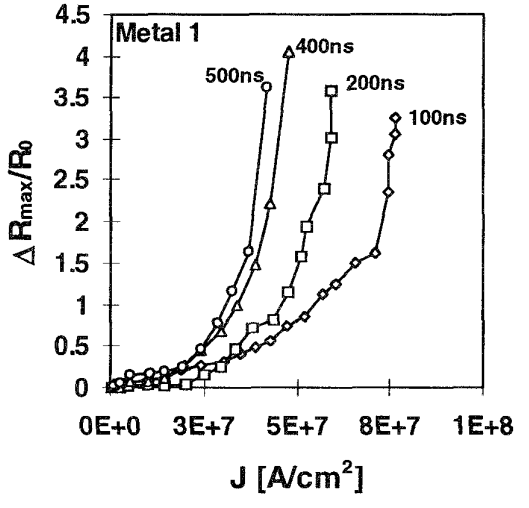

Figure 7. Maximum resistance rise in metal 1 leads stressed by pulses of varying widths.

Figure 7 shows the effect of pulse width on the maximum resistance rise in metal 1. The critical current density J_{crit} decreases with increasing pulse width. This is better illustrated in Fig. 8 for metal 1. Similar behavior was observed for other metal levels. From Fig. 7 it can be seen that the heating of the metal 1 lines caused by different pulse widths raises the resistance by a factor of >3.6. This was experimentally observed for almost all the cases irrespective of the metallization level and the pulse width. However, it was usually difficult to cause open circuit failure of metal 4 with the 100 ns pulses, since the thicker metal required a current that was greater than the compliance limit of ~2 A of the TLP system. This can be observed from Fig. 3. Also, the last points representing resistance rise factor for metal 1, 2 and 3 in Fig. 3 seem to be below 3.6, since these points represent the current density value up to which there was no open circuit failure. The final pulse causing the failure does indeed raise the resistance by a factor of >3.6.

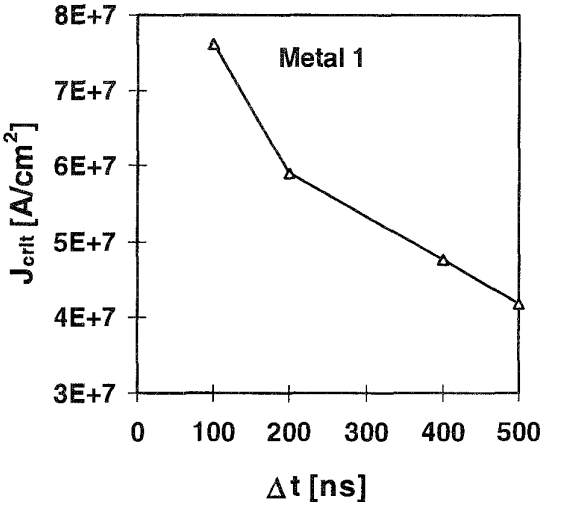

Figure 8. The decrease in critical current density J_{crit} with pulse width for metal 1.

Thermally Accelerated Metal Breakdown Mechanism

As observed the ESD pulses can heat up the metal lines beyond their melting points giving a γ of >3.6. In fact, the linear model of resistivity rise with temperature gives a maximum temperature rise value of 1000 ^{0}C. This critical rise in temperature value agrees with previous results in the literature [5]. However, the linear behavior of the resistivity of the metal with temperature is valid only up to the melting point [9]. Thus it is difficult to predict the exact temperature at which the lines fail. There is however ample evidence that the lines were melted before failing. In fact when using near critical current pulses melting could be observed in situ in some metal 4 lines. This was observed regardless of the pulse

Difference in slopes between metal 1, 2, 3, and metal 4 is due to the bigger thermal capacity of metal 4. Note that the slope of metal 4 is not exactly half that of the lower metals since the net thickness of metal 4 is less than twice that of the lower metals (only the AlCu layer is doubled). The thermal capacity is proportional to the inverse of the slopes of $\Delta R_{max}/R_0$ vs energy curves. The thermal capacity of metal 1, 2 and 3 from Fig. 11 is 15.46 X 10^{-9} J/^{0}C. This is larger than the 8.25 X 10^{-9} J/^{0}C calculated for the AlCu/TiN stack. The difference between the theoretically and experimentally determined values of the thermal capacity suggests that a finite sheath of oxide around the metal was heated.

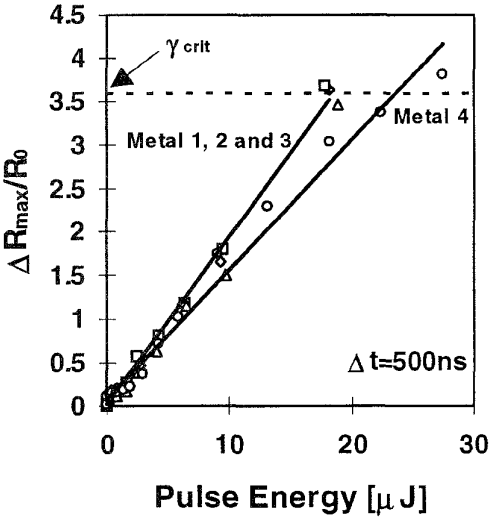

Figure 12. Maximum resistance rise factor, $\Delta R_{max}/R_0 = \gamma$, as a function of pulse energy for a 500 ns pulse.

From diffusion theory [13] we expect the thickness of the oxide sheath to be proportional to $(\Delta t)^{1/2}$. This is supported by the fact that in Fig. 12, for a 500 ns pulse, the heat capacity = 18.6 X 10^{-9} J/^{0}C for metal 1, 2 and 3 which is larger than the heat capacity of the 200 ns case. Figure 13 illustrates this effect of increasing thermal capacity with pulse width for metal 1. This difference between the thermal capacities has been used to calculate the thickness of the oxide sheath.

A uniform film of oxide of thickness d_{ox} around the metal was assumed to have been heated up during the pulsing events. The effect of the surrounding oxide is invoked now since its thickness is much smaller than the total dielectric thickness around the metal lines. Figure 14 is a plot of oxide sheath thickness vs $(\Delta t)^{1/2}$. The heat diffusion constant was extracted from this graph and has a value of 1.75 X 10^{-6} cm/(ns)$^{1/2}$. From this value of the diffusion constant the thermal diffusivity of the surrounding oxide was calculated to be 1.5 X 10^{-3} cm^2/s. Here the metal line was considered as a line source of heat and the solution to the differential equation for heat conduction for such a case was used as explained in [14]. This value is close to the theoretically calculated diffusivity value of 6 X 10^{-3} cm^2/s for silicon dioxide [15].

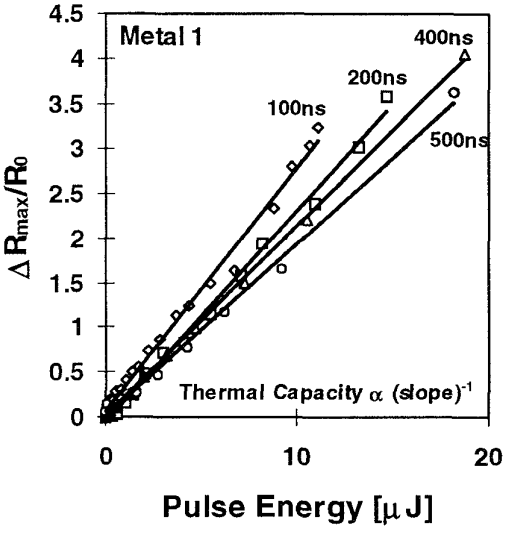

Figure 13. Effect of pulse width on the thermal capacity of metal 1.

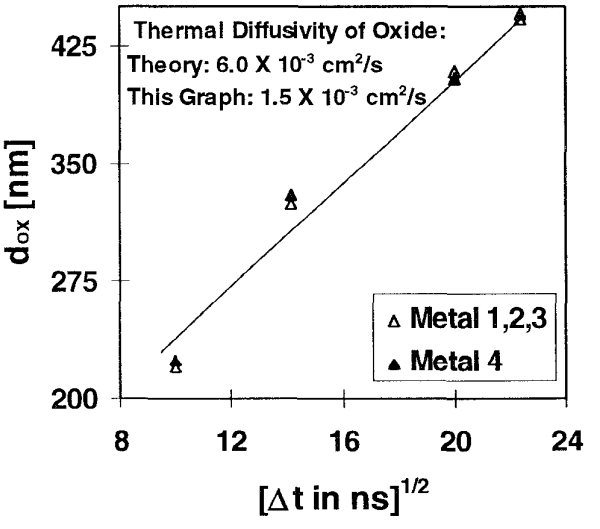

Figure 14. Oxide sheath thickness around metal lines as a function of $(\Delta t)^{1/2}$.

Design Guidelines for ESD Protection Circuits

As mentioned earlier, it is highly desirable to have a model that can be used for generating design guidelines for ESD/EOS protection circuit interconnects. These guidelines are important for the optimum design of metal interconnects so that they can carry high currents without causing open circuit failures during an ESD type event. A model is presented here that incorporates metal, barrier and oxide heating. The physics of the model is explained below. The critical energy E_{crit}, is a function of Δt and line geometry.

$$E_{crit} = [m_iC_i + m_jC_j + m_kC_k]\,\gamma_{crit}\,(TCR)^{-1} + m_iL_f \qquad (4)$$

Here, m is mass, C is specific heat, TCR is the temperature coefficient of resistance and L_f is the latent heat of fusion. Also, subscripts i, j and k are for AlCu, TiN and Oxide respectively. From equation (3), the critical value of the pulse energy can be expressed as,

$$E_{crit} = \frac{1}{2} I^2 \Delta t R_0 \{2 + \gamma_{crit}\} \qquad (5)$$

From Equations (4) and (5) we get,

$$I_{crit} = \sqrt{\frac{Wd_i(Wa_0 + a_1\beta_{ox})}{\Delta t L_e a_2}} \qquad (6)$$

Where,

$a_0 = 2[\{(\delta_i L_i d_i C_i) + (\delta_j L_j d_j C_j)\}(TCR)^{-1}\gamma_{crit} + (\delta_i L_i d_i L_f)]$,

$a_1 = 2[C_k\,\delta_k\,(TCR)^{-1}\gamma_{crit}]$ and

$a_2 = \rho_i\,[2 + \gamma_{crit}]$

L_e = length of metal line across which the voltage develops, taken as 1200 μm in this work.

L = thermal length of the metal lines, taken as 1100 μm in this work.

W = line width,

d = film thickness,

δ = density of the material,

ρ_i = resistivity of AlCu,

$\beta_{ox} = [4\{W + d_s + L\}.\,d_{ox}^2 + 2\{LW + Ld_s + Wd_s\}.\,d_{ox}]$ is the volume of the oxide sheath around the metal lines.

d_s = thickness of TiN+AlCu stack and

$d_{ox} = a_d\,.\,(\Delta t)^{1/2}$ where a_d is the heat diffusion constant extracted from Fig. 14.

Figure 15 is a plot of E_{crit} vs pulse width showing the correlation between the experimental values and the model. The critical energy increases with the pulse width as expected.

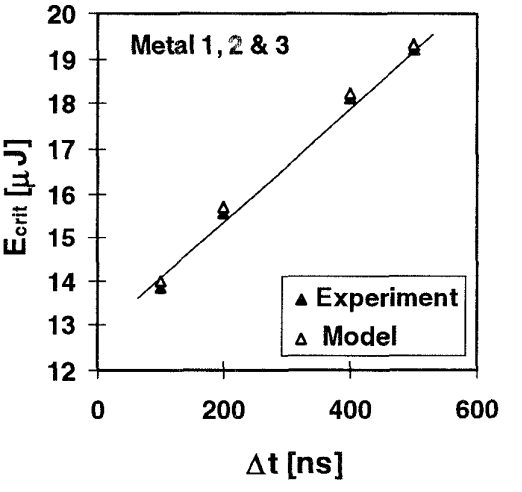

Figure 15. The critical energy of the pulse as a function of the pulse width as observed in experiment and extracted from the model.

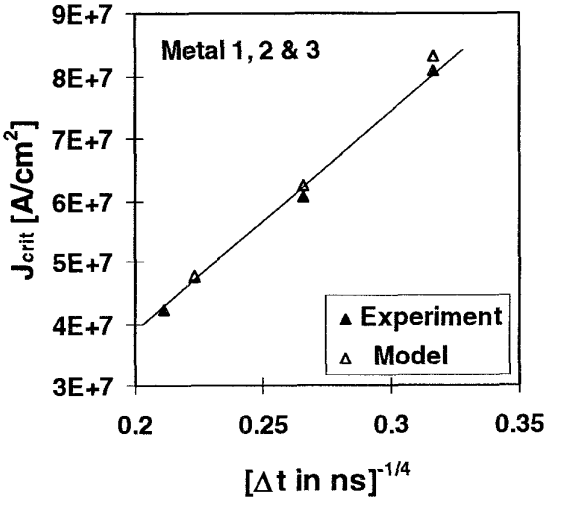

Figure 16. A plot of J_{crit} vs $(\Delta t)^{-1/4}$ depicting the correlation between the data and the model as predicted by equation (6).

Figure 16 shows the variation of the critical current density with $(\Delta t)^{-1/4}$. Once again, the critical current density values

obtained using the model are in excellent agreement with the experimentally observed values.

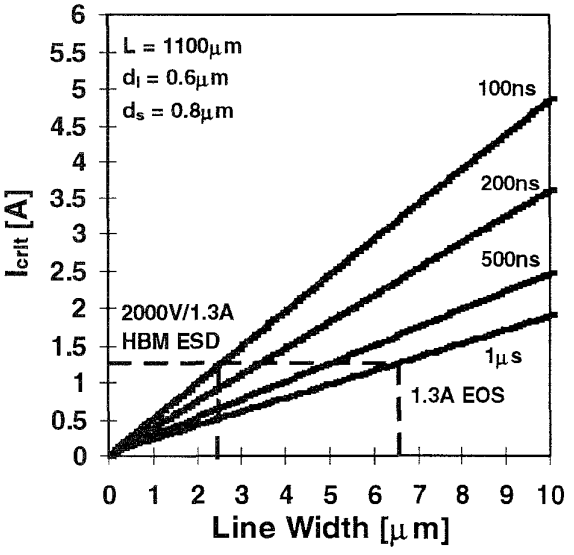

Figure 17. Relation between critical current, pulse width and line width that can be used for designing ESD protection circuit interconnects.

Finally the analytical model developed in the form of equation (6) relating the critical current or maximum allowable current without causing open circuit metal failure, the pulse width and the line width is shown in Fig. 17. While using equation (6) the specific heats of AlCu, TiN and oxide were taken to be independent of temperature due to their small increase in value with temperature [16]. A mean value was therefore used in all the calculations. The critical current values for various pulse widths and a 3 μm wide line agree very well with the critical current values obtained in our experiment.

This figure can be used to extract various design guidelines for ESD/EOS protection circuit interconnects. For example, a typical Human Body Model (HBD) ESD pulse, which can be described as a ~100 ns/1.3 A event [1,2] would require the width of the metal line to be greater than 2.5 μm. Similarly for an electrical overstress (EOS) event of 1 μs the minimum linewidth should be more than 6.5 μm. Hence a safe design guideline for these stress conditions would be ~10 μm.

Latent ESD Damage: Effect on Microstructure and Electromigration Performance

A potential reliability hazard has been identified that significantly degrades interconnect lifetime due to enhanced electromigration in lines subjected to ESD stress conditions. This *"latent ESD damage"* is introduced by pulses that heat the metal lines past their highest equilibrium solid solution temperature. The adiabatically enclosed metal lines offer no visible clue of any damage. Furthermore, no change in line resistance can be observed, even with a Kelvin measurement after the pulse stressing. However, the heating during the ESD event is followed by quenching, since the thermal time constant is usually of the order of 1 μs. This rapid cooling from a molten or partially molten state after pulsing results in the formation of a large number of small grains throughout the line or in localized segments. This happens due to heterogeneous nucleation which introduces a high nucleation rate [17]. If the line is fully melted, then there is an uniform distribution of small grains throughout the entire length of the line. This results in the formation of a large number of grain boundaries throughout the line which aids the diffusion of metal atoms under an applied electric field. In the case of localized melting, segments of smaller grain sizes are created in the line. These introduce a gradient in the microstructure and the effect of electromigration under such a gradient becomes more severe [18]. This was verified by comparing electromigration lifetimes of pulsed and virgin AlCu metal 1 lines.

Accelerated wafer level EM tests were performed on virgin metal lines and then on two groups of pulsed lines. One group of lines were stressed by a 500 ns/750 mA ESD pulse that gave a value of $\gamma = 3.5$, which was just below $\gamma_{crit.}$ The other group was stressed by a 100 ns/1.34 A pulse that gave a γ of about 2.8. All the lines from both these groups showed no visible damage or any significant change in resistance after the pulsing. However the EM lifetime data revealed that the pulsed lines from the first group had lifetimes reduced by a factor of 3. The EM lifetime degradation was even more for the second group of pulsed lines and the MTTF (mean time to fail) was reduced by a factor of 4. This can be attributed to localized melting caused by the 100 ns/1.34 A pulses since the value of γ was well below the threshold value. The 500 ns/750 mA pulses heated the lines more strongly as indicated by the larger γ value. This was due to the uniform melting of the entire volume of the line which resulted in a more uniform grain size distribution. This accounts for the lower EM lifetime degradation factor since there are no microstructural gradients. This EM lifetime degradation effect on the reliability is significant and needs careful consideration.

CONCLUSION

We have characterized the effect of high current and ESD pulses on metal interconnects in a multi level VLSI metallization system. A model for interconnect heating under

ESD conditions has been presented. It has been shown that thermal breakdown of metal lines occur when the resistance rises past the factor of 3.6. At that point open circuit failure of metal lines is observed. Failure is caused by thermal stress generated due to the difference in the coefficient of thermal expansion of AlCu and the surrounding dielectric. A corresponding critical temperature value of 1000 ^{0}C is obtained by taking the metal resistivity to be a linear function of temperature. In reality, the resistivity is a complex function of temperature in the high temperature regime of >660 ^{o}C, and hence accurate calculation of the critical temperature is difficult. The critical failure current has been shown to be strongly influenced by the pulse width and the thermal capacity of the metal lines. A potential latent failure has been identified that needs careful consideration. It has been shown that for subthreshold current pulses the metal lines return to their original solid state without any significant change in their DC resistance. This *"latent ESD damage"* has been shown to significantly lower the electromigration lifetime of interconnects. The EM lifetime degradation results due to the formation of a large number of small grains which can be either uniformly distributed throughout the line or localized in segments, depending on the value of the resistance rise factor. The large number of small grains form due to heterogeneous nucleation that occurs during the solidification of the molten metal lines after an ESD type event. The model developed for the heating of interconnects has been applied to provide design guidelines for ESD and I/O buffer interconnects.

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REFERENCES

[1] C. Duvvury and A. Amerasekera, "ESD: A Pervasive Reliability Concern for IC Technologies", *Proceedings of the IEEE*, Vol. 81, No. 5, pp. 690-702, May 1993.

[2] A. Amerasekera and J. Verwey, "ESD in integrated circuits", *Quality and Reliability Engineering International*, Vol. 8, 259-272, 1992.

[3] A. Amerasekera and C. Duvvury, "The Impact of Technology scaling on ESD Robustness and Protection Circuit Design", *EOS/ESD Symposium Proceedings*, pp. 237-245, 1994.

[4] S. Ramaswamy, C. Duvvury and S. Kang, "EOS/ESD Reliability of Deep Sub-Micron NMOS Protection Devices", *Proceedings of the IEEE International Reliability Physics Symposium*, pp. 284-291, 1995.

[5] N. Khurana, T. Maloney, W. Yeh, "ESD on CHMOS Devices--Equivalent Circuits, Physical Models and Failure Mechanisms", *Proceedings of the IEEE International Reliability Physics Symposium*, p. 212, 1985.

[6] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena", *EOS/ESD Symposium Proceedings*, pp. 49-54, 1985.

[7] T. J. Maloney, "Integrated Circuit Metal in the Charged Device Model: Bootstrap Heating, Melt Damage and Scaling Laws", *EOS/ESD Sypmposium Proceedings*, pp. 129-134, 1992.

[8] H. Zheng, *"Accelerated Stress Testing for High Reliability Metallization Lines"*, Masters Thesis, Clemson University, 1990, Chapter II, pp. 24-32.

[9] E. A. Brandes and G. B. Brook, editors, *Smithells Metals Reference Book*, Butterworth-Heinemann Ltd., 1992, 7th Ed.

[10] C. Li and J. Yamanis, Super Tough Silicon Nitride with R-Curve Behavior, *Ceram. Eng. Sci. Proc.*, pp. 632-645, 1989.

[11] J. Schweitz, Mechanical Characterization of Thin Films by Micromechanical Techniques, *MRS Bulletin*, pp. 34-45, July 1992.

[12] M. A. Korhonen, P. Borgesen and Che-Yu Li, Mechanisms of Stress-Induced and Electromigration-Induced Damage in Passivated Narrow Metallizations on Rigid Substrates, *MRS Bulletin*, pp. 61-68, July 1992.

[13] P. Shewmon, *Diffusion in solids*, TMS, 1989, ch. 1, pp. 14-19.

[14] H. S. Carslaw and J. C. Jaeger, *Conduction of Heat in Solids*, Oxford University Press, 1993, ch. 10, pp. 261-263.

[15] H. S. Carslaw and J. C. Jaeger, *Conduction of Heat in Solids*, Oxford University Press, 1993, ch. 1, pp. 8-10.

[16] Y. S. Touloukian et al, *Thermophysical properties of Matter*, IFI/Plenum, 1970, Vol. 4.

[17] D. A. Porter and K. E. Easterling, *Phase Transformations in Metals and Alloys*, Van Nostrand Reinhold Company Ltd., 1981, ch. 4, pp. 186-262.

[18] J. M. Poate, K. N. Tu and J. W. Mayer, *Thin Films - Interdiffusion and Reactions*, Wiley-Interscience Publication, 1978, New York, (ch. 8 by F. M. d'Heurle and P. S. Ho, *Electromigration in Thin Films*), pp. 243-303.