Quantitative Projections of Reliability and Performance for Low-k/Cu Interconnect Systems

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ABSTRACT

This paper presents a methodology for quantitative analysis of the role of electromigration (EM) reliability and interconnect performance in determining the optimal interconnect design in low-k/Cu interconnect systems. It is demonstrated that EM design limits for *signal lines* are satisfied once interconnect performance is optimized.

INTRODUCTION

In current VLSI interconnect designs, current density design rules are typically based on EM lifetimes [1]. However, the actual current densities are determined by the interconnect parameters (resistance and capacitance per unit length and the length of the interconnect) and the strength of the buffer which is driving the interconnect length. In a typical design, long interconnects, which can potentially have large current densities, are usually split into buffered segments to improve performance (signal slew and delay) [2]. The signal line length and buffer sizes are optimized to give maximum performance for a given technology. Signal lines longer than the optimum length would increase interconnect delay while buffer sizes larger than the optimum would result in an increase in buffer delay. Moreover, increasing buffer size would increase the current density of the signal line connected to the output and may also cause excessive power dissipation. However, it is not known whether the associated current densities in signal lines optimized for maximum performance also meet the EM design limits.

In current technologies, low-k materials are being introduced as inter-layer dielectrics in an attempt to reduce the interconnect delay [3-5]. However, these dielectrics invariably have poor thermal properties and therefore the use of such materials can significantly impact the EM design limits. On the other hand, the use of Copper, which has lower resistivity, alleviates the problem to some extent. It is therefore important to quantify whether EM reliability or performance is the dominant factor determining the optimal signal line length in various low-k/Cu based interconnect systems.

In this work a methodology for quantitative comparison of the impact of EM and performance on the optimization of the signal line length is presented. The methodology is applied to various low-k/Cu interconnect systems. For the purpose of reliability analysis we used interconnect data (line geometry, insulator thickness etc.) from NTRS [6] for two different technology nodes (0.25-μm and 0.1-μm) and the self-consistent approach proposed in [7-8], which comprehends Joule heating (or self-heating) and EM simultaneously. Once a self-consistent temperature (T_m) is obtained using this approach, the maximum allowed values of j_{rms} and j_{peak} can be obtained [7-8].

In the next section, effect of self-heating on EM is briefly discussed followed by an analysis of the self-consistent design approach that takes quasi-2D heat conduction into consideration. The modified self-consistent approach is then used to quantify the impact of new interconnect materials (Cu and low-k dielectrics) on allowed current density limits. The last section introduces a methodology for computing the current densities from performance considerations only, and then provides a direct comparison between the reliability and performance based current density design limits.

INTERCONNECT RELIABILITY

Influence of Self-Heating on Electromigration

EM lifetime reliability of metal interconnects is modeled by the well known Black's equation [9] given by,

$$TTF = A\, j^{-n} \exp\left(\frac{Q}{k_B T_m}\right) \tag{1}$$

where TTF is the time-to-fail (typically for 0.1% cumulative failure). A is a constant that is dependent on the geometry and microstructure of the interconnect, j is the DC or average current density. The exponent n is typically 2 under normal use conditions, Q is the activation energy for grain-boundary diffusion and equals ~ 0.7 eV for Al-Cu, k_B is the Boltzmann's constant, and T_m is the metal temperature. The typical goal is to achieve 10 year lifetime at 100 ^{0}C, for which equation (1) and accelerated testing data produce a design rule value for the acceptable current density, j_0, at the reference temperature T_{ref}. However, this design rule value does not comprehend self-heating.

The effect of self-heating can be analyzed from the following: The metal temperature, T_m in equation (1) is given by,

$$T_m = T_{ref} + \Delta T_{self-heating} \tag{2}$$

and,

$$\Delta T_{self-heating} = \left(T_m - T_{ref}\right) = I_{rms}^2 R R_\theta \tag{3}$$

where T_{ref} is typically taken as ~100 ^{0}C, $\Delta T_{self\text{-}heating}$ is the temperature rise of the metal interconnect due to the flow of current, R is the interconnect resistance, and R_θ is the effective thermal impedance of the interconnect line to the chip. I_{rms} is the RMS current for a time varying current waveform, or the DC current for a constant current stress. It can be observed from equations (1) and (2), that as self-heating increases, the metal temperature increases, and hence the EM lifetime decreases exponentially. Therefore, it is important to accurately account for self-heating in equation (1).

Self-Consistent Interconnect Design Analysis

In this sub-section the formulation of the self-consistent solutions [7] for allowed interconnect current density is summarized, and then applied to analyze low-k/Cu interconnects in the next sub-section. The $\Delta T_{self\text{-}heating}$ in interconnects given by equation (3) can be written in terms of the RMS current density as,

$$j_{rms}^2 = \frac{\left(T_m - T_{ref}\right) K_{ins} W_{eff}}{t_{ins}\, t_m\, W_m\, \rho_m(T_m)} \tag{4}$$

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Here t_m and W_m are the thickness and width of interconnect metal line, and $\rho_m(T_m)$ is the metal resistivity at temperature T_m. Note that the thermal impedance R_θ in equation (3) has been expressed as,

$$R_\theta = \frac{t_{ins}}{K_{ins}\, L\, W_{eff}} \tag{5}$$

Here t_{ins} is the total thickness of the underlying dielectric, K_{ins} is the thermal conductivity normal to the plane of the dielectric, and L is the length of the interconnect. In this expression for the thermal impedance, W_{eff} has been modeled as the effective width of the metal line taking quasi-2D heat conduction [10] into consideration from experimental data for high aspect ratio lines.

Now, in order to achieve an EM reliability lifetime goal mentioned earlier, we must have the lifetime at any (j_{avg}) current density and metal temperature T_m, equal to or larger than the lifetime value (eg. 10 year) under the design rule current density stress j_0, at the temperature T_{ref}. This value of j_0 is dependent on the specific interconnect metal technology. Therefore we have,

$$\frac{\exp\left(\frac{Q}{k_B T_m}\right)}{j_{avg}^2} \geq \frac{\exp\left(\frac{Q}{k_B T_{ref}}\right)}{j_0^2} \tag{6}$$

Using the relationship between j_{avg}, j_{peak}, j_{rms}, and r for a rectangular unipolar pulse, ($j_{avg} = r\, j_{peak}$, & $j_{rms} = r^{0.5}\, j_{peak}$) we have after eliminating j_{peak},

$$\frac{j_{avg}^2}{j_{rms}^2} = r \tag{7}$$

Substituting for j_{rms}^2 from equation (4) and j_{avg}^2 from equation (6) in (7) we get the self-consistent equation given by,

$$r = j_0^2 \left(\frac{\exp\left(\frac{Q}{k_B T_m}\right)}{\exp\left(\frac{Q}{k_B T_{ref}}\right)} \right) \frac{t_{ins}\, t_m\, W_m\, \rho_m(T_m)}{(T_m - T_{ref}) K_{ins}\, W_{eff}} \tag{8}$$

Note that this is a single equation in the single unknown temperature T_m. Once this self-consistent temperature is obtained from equation (8), the corresponding maximum allowed j_{peak} and j_{rms} can be calculated from equation (4). The self-consistent equation given by equation (8) for unipolar pulses is also valid for more general time varying waveforms with an effective duty cycle r_{eff} [8].

Impact of Self-Heating and New Materials

Allowed interconnect current densities are expected to be strongly influenced by low-k materials, which cause increased Joule-heating due to their lower thermal conductivity [11,12]. Therefore we begin by analyzing the effect of introducing new interconnect and dielectric materials on allowable current density limits. In Figure 1 the self-consistent values of j_{rms} and j_{peak} are plotted as a function of the duty cycle r, for different dielectrics. It can be observed that j_{rms} and j_{peak} decrease significantly as dielectrics with lower thermal conductivity are introduced. For small values of r, j_{rms} varies very slowly with r. This is due to increased Joule-heating. In Figure 2 we plot j_{peak} and T_m as a function of r for SiO_2 and air as the dielectric for different values of the design current density, j_{avg}. It can be observed that j_{avg} does not change j_{peak} appreciably, and as r reduces, the increase in j_{peak} with j_{avg} becomes negligible. Furthermore, for a dielectric material with low thermal

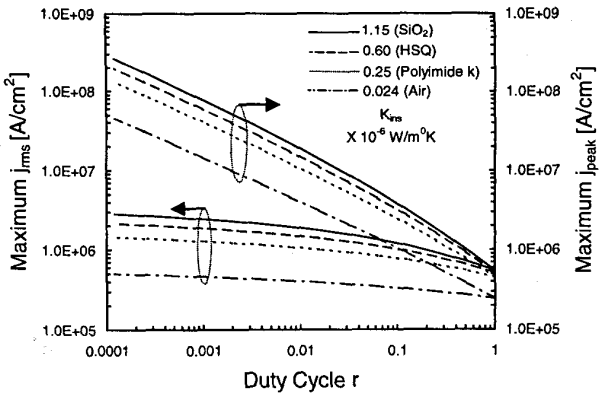

Figure 1. Self-consistent solutions for maximum allowed values of j_{rms} and j_{peak} for Metal 6 in 0.25-μm technology for different values of j_{avg} (or j_0). Interconnect metal is Cu with $\rho_m(T_m) = 1.67 \times 10^{-6}$ [1 +6.8 x 10^{-3} $^0C^{-1}$ (T_m - T_{ref})] Ω-cm. The activation energy is assumed to be same as that for AlCu.

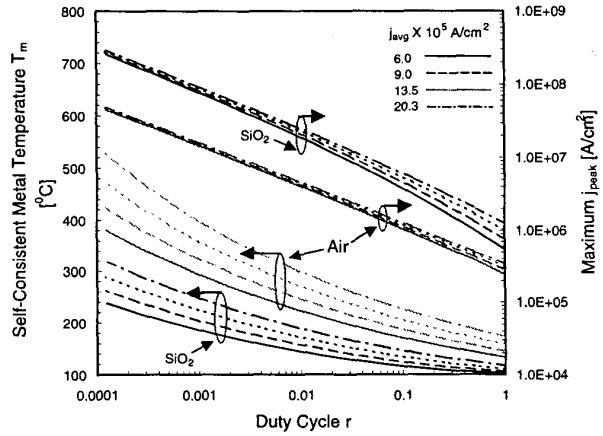

Figure 2. Self-consistent metal temperature and the maximum allowed j_{peak} for Metal 6 in a 0.25-μm Cu technology, as a function of duty cycle for different values of j_{avg} (or j_0) for SiO_2 and air as the dielectric.

conductivity such as air, j_{peak} is almost independent of j_{avg}. This indicates that introduction of better interconnect materials becomes increasingly ineffective in increasing j_{peak} for dielectrics with poor thermal properties.

Figure 3 summarizes the impact of low-k dielectrics on allowed j_{peak} for both Cu and AlCu interconnect systems. It can be observed that the difference between the maximum allowed j_{peak} for AlCu and Cu interconnects reduces as dielectric materials with poor thermal properties are introduced. For the specific case of air as the dielectric, the j_{peak} values are very similar for AlCu and Cu. This is demonstrated for two different values of j_{avg} for Cu, one value identical to that of AlCu and the other three times higher than this value, which accounts for the improved EM performance in Cu. We have also compared current carrying capabilities of signal and power lines and the results are shown in Figure 4. Consistent with Figure 1, it can be observed that the j_{peak} values are about an order of magnitude lower for the power lines due to increased thermal effects.

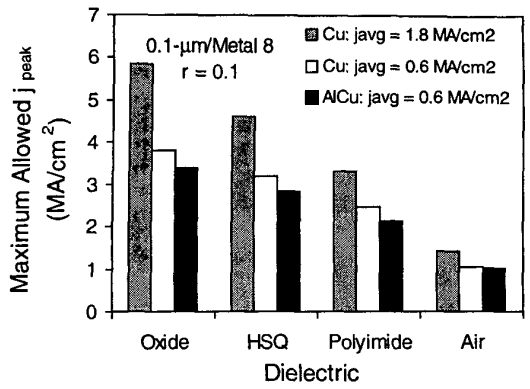

Figure 3. Comparison of the maximum allowed j_{peak} values for AlCu and Cu lines with two different j_{avg} values for Metal 8 of a 0.10-µm technology shown for different dielectric materials.

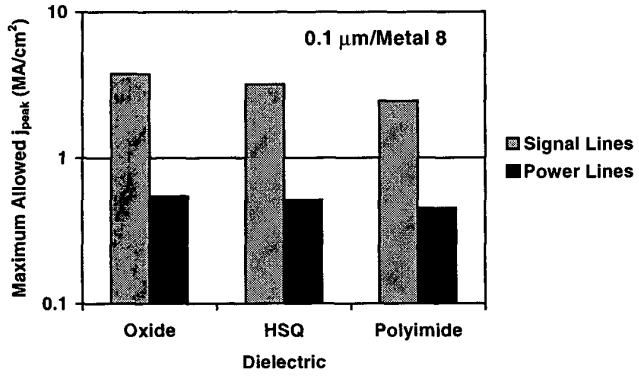

Figure 4. Comparison of the maximum allowed j_{peak} values for signal (r = 0.1) and power lines (r = 1.0) for Metal 8 of a 0.10 µm technology shown for different dielectric materials. The lower values of j_{peak} in power lines is because of their higher temperature rise resulting from carrying DC current.

INTERCONNECT PERFORMANCE

Implications of Optimizing Buffer Size and Signal Line Length

As a next step we demonstrate a methodology for computing current density from performance considerations only. Consider an interconnect of length l between two buffers. The schematic representation is shown in Figure 5(a). Figure 5(b) shows an equivalent RC circuit for the system. The voltage source (V_{tr}) is assumed to switch instantaneously when voltage at the input capacitor (V_{st}) reaches a fraction x, $0 \le x \le 1$ of the total swing. Hence the overall delay of one segment is given by:

$$\tau = b(x)R_{tr}(C_L + C_P) + b(x)(cR_{tr} + rC_L)l + a(x)rcl^2 \quad (9)$$

where $a(x)$ and $b(x)$ only depend on the switching model, i.e., x. For instance, for x=0.5, a=0.4 and b=0.7 [13]. If r_0, c_0 and c_p are the resistance, input and parasitic output capacitances of a minimum sized inverter respectively then R_{tr} can be written as r_0/s where s is size of the inverter in multiples of minimum sized inverters. Similarly $C_P = s\,c_p$ and $C_L = s\,c_0$.

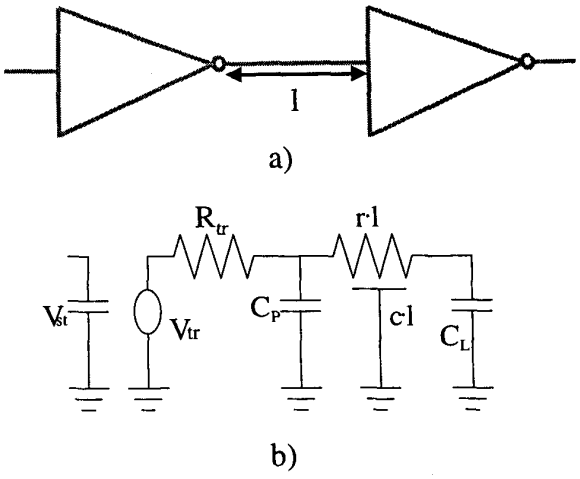

Figure 5. (a) An interconnect of length l between two buffers (b) The equivalent RC circuit. V_{st} is the voltage at the input capacitance that controls the voltage source V_{tr}. R_{tr} is the driver transistor resistance, C_p is the output parasitic capacitance and C_L is the load capacitance of the next stage, r and c are the interconnect resistance and capacitance per unit length respectively.

If the total interconnect of length L is divided into n segments of length $l = L/n$, then the overall delay is given by

$$T_{delay} = n\tau = \frac{L}{l}b(x)r_0(c_0 + c_p) + b(x)\left(c\frac{r_0}{s} + src_0\right)L + a(x)rclL \quad (10)$$

It should be noted in the above equation that s and l appear separately and therefore T_{delay} can be optimized separately for s and l. The optimum values of l and s are given as:

$$l_{opt} = \sqrt{\frac{b(x)r_0(c_0 + c_p)}{a(x)rc}} \quad (11)$$

$$s_{opt} = \sqrt{\frac{r_0 c}{r c_0}} \quad (12)$$

Note that s_{opt} is independent of the switching model, i.e., x.

Since, for deep sub-micron technologies, a significant fraction of interconnect capacitance, c, is contributed by coupling and fringing capacitances to neighboring lines as shown in Figure 6, we performed a full 3D-capacitance extraction using SPACE3D [14] for signal lines at various metal levels to obtain the values of c for SPICE simulations.

This inverter-interconnect structure is used as a delay stage in a multi-stage ring oscillator and the current waveforms and current densities along the interconnect are be obtained. In practice, the input capacitance C_L of the inverter is almost constant but the output resistance R_{tr} and output parasitic capacitance C_P are bias dependent and therefore change during the output transition. Therefore accurate values of optimal interconnect length and buffer size need to be determined by SPICE simulation. For this, we take advantage of the fact that the optimal interconnect length does not depend on the buffer size. Therefore, we first set the buffer size to an appropriate value and sweep the interconnect length and find the optimum length which minimizes the ratio of the ring oscillator stage delay and interconnect length.

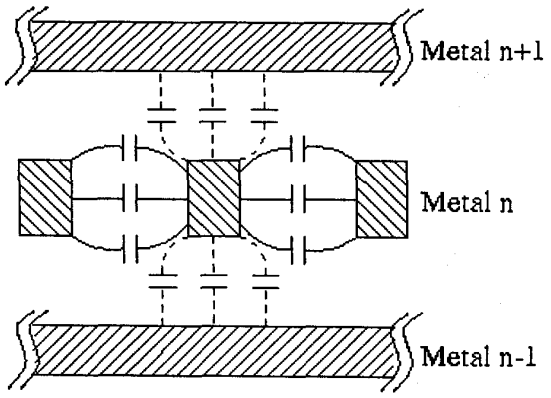

Figure 6. Typical Interconnect Structure.

Using this optimum length, we subsequently sweep buffer sizes and find the optimum buffer size which minimizes the stage delay. This allows us to obtain the values of l_{opt} and s_{opt} taking into account the bias dependence of transistor resistances and capacitances and the switching model. This analysis is carried out for every metal layer in the two technologies under study.

Note that due to the distributed nature of the interconnect, the maximum current density occurs close to the buffer output. Hence, we need to verify whether this maximum current density, which is obtained from performance considerations ($j_{\text{-performance}}$) only, also meets the EM current density limits ($j_{\text{-reliability}}$) obtained earlier using the self-consistent approach.

The interconnect current waveform in the metal lines for 0.25-μm and 0.1-μm technologies, as obtained from SPICE simulations, were found to be bipolar as expected. It should be noted that equation (1) represents the EM lifetime reliability equation for a unipolar pulse or dc current. The EM lifetime under bipolar stress conditions is known to be higher than that under the unipolar case. In this work, the unipolar EM lifetime reliability equation is used as a worst case limit.

Also, the relative rise and fall skew was found to be same across both technologies. From our simulations it was observed that drivers and interconnects optimized using equation (11) and equation (12), maintain good slew rates for rising and falling transitions for all the metal layers and across both technologies with an effective duty cycle ($r_{eff} = j_{avg}^2 / j_{rms}^2$) of 0.12 ± 0.01 as shown in Table 1. Since for the signal lines the current waveform is symmetric and bipolar, j_{avg} and j_{rms} are computed over half the time-period to obtain r_{eff}. Table 1 also lists the maximum values of the average and peak current densities.

In the above analysis it was assumed that the line capacitance per unit length is constant. In an actual design this is not necessarily the case. Consider the interconnect structure shown in Figure 6. The total interconnect capacitance C_{total} can be viewed as a sum of capacitance to lines on the same metal layer $C_{neighbor}$ and lines on other metal layers C_{other} (shown by solid and dashed lines respectively in Figure 6.) $C_{neighbor}$ and C_{other} consist of both parallel plate and fringing capacitances. Lines on adjacent metal layers are typically routed orthogonal to each other. Hence the total capacitance between metal lines at two adjacent layers is very small. On the other hand the capacitance to neighboring lines is large. This is specially the case for deep sub-micron technologies where the aspect ratio of the lines is greater than 1 and as a result, $C_{neighbor} / C_{total}$ is very high (0.7 to 0.9). The effective capacitance of the line ranges from 2 $C_{neighbor}$ + C_{other} to C_{other} depending upon whether the neighboring line signals are switching in the opposite direction or the same direction.

Layer	l_{opt} (mm)	s_{opt}	j_{avg} (x10^{5}A/cm^2)	j_{peak} (x10^{5}A/cm^2)	r_{eff}
1	2.51	75	3.06	27.02	0.11
2	2.41	80	2.91	26.38	0.11
3	4.79	157	1.67	14.69	0.11
4	5.48	148	1.32	13.48	0.10
5	12.5	494	0.61	5.18	0.12
6	13.9	454	0.52	4.69	0.11

(a)

Layer	l_{opt} (mm)	s_{opt}	j_{avg} (x10^{5}A/cm^2)	j_{peak} (x10^{5}A/cm^2)	r_{eff}
1	0.85	36	5.13	38.99	0.13
2	0.9	40	5.10	39.48	0.13
3	1.57	97	2.73	20.93	0.13
4	1.79	85	2.39	18.27	0.13
5	4.47	276	1.28	9.78	0.13
6	4.68	249	1.21	9.00	0.13
7	8.8	500	0.49	3.67	0.13
8	9.58	522	0.44	3.5	0.12

(b)

Table 1. Optimized interconnect length (l_{opt}), buffer size (s_{opt}), corresponding average and peak current densities and duty cycle (r) for (a) 0.25-μm Cu technology with insulator dielectric constant = 3.3 and (b) 0.1-μm Cu technology with insulator dielectric constant = 2.0. The optimum repeater size given by s_{opt} means that the width of the NMOS and PMOS for this inverter are obtained by scaling the width of the corresponding transistors in a minimum sized inverter by a factor of s_{opt}.

Furthermore, it is observed from simulation and can be shown that the interconnect current remains almost the same if the load capacitance of a buffer changes. The rise and fall time will get affected significantly but the interconnect current does not change appreciably if the buffer drive strength is unchanged. However, for the slower transition, r increases and for the faster transition, r decreases (typical values observed in simulation are 0.2 for slower transition and 0.05 for the faster transition).

Quantitative Comparisons between Reliability and Performance

Figure 7 shows the comparison of $j_{avg\text{-}performance}$ with the values of $j_{avg\text{-}reliability}$ for a 0.25-μm technology. It can be observed that $j_{avg\text{-}performance}$ is always lower than $j_{avg\text{-}reliability}$ for all the dielectrics. However, for low-k dielectric materials we find that the difference between $j_{avg\text{-}reliability}$ and $j_{avg\text{-}performance}$ reduces. This is due to the fact that these dielectrics have lower thermal conductivity than oxide which leads to greater interconnect Joule-heating and therefore lower allowable current densities.

Finally, it should be noted that the $j_{avg\text{-}reliability}$ values generated above were for an isolated line. In real ICs with multiple layers of interconnect, the Joule-heating of interconnect lines is known to be significantly more severe due to thermal coupling between neighboring lines [15]. Figure 8 shows comparison of $j_{avg\text{-}performance}$ with the values of $j_{avg\text{-}reliability}$ for a 0.1-μm technology including the $j_{avg\text{-}reliability}$ values for realistic interconnect structures using finite element simulations to demonstrate an optimistic scenario of thermal coupling using various dielectrics.

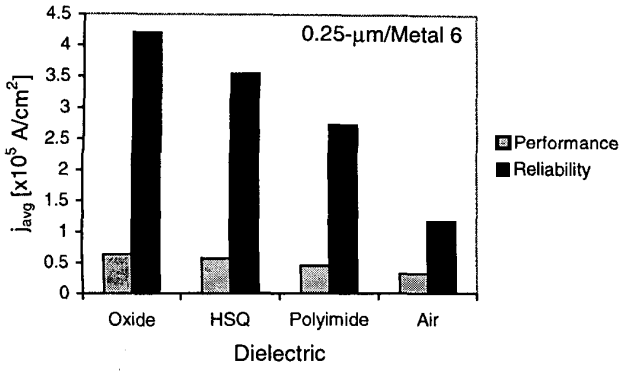

Figure 7. Comparison of j_{avg} values obtained from reliability and electrical performance considerations for Metal 6 of a 0.25-µm Cu technology. $r_{eff} = 0.11$.

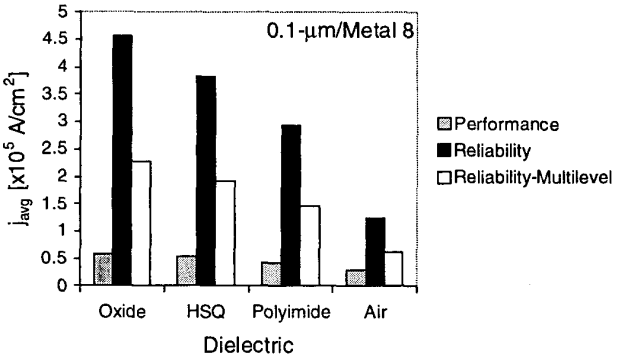

Figure 8. Comparison of j_{avg} values obtained from reliability and performance considerations for Metal 8 of a 0.1-µm Cu technology. $r_{eff} = 0.12$. The effect of thermal coupling in realistic multilevel interconnect arrays on the j_{avg} values is also shown here for various dielectric materials.

It can be observed that the $j_{avg\text{-}performance}$ values remain lower than the $j_{avg\text{-}reliability}$ values even after thermal coupling in realistic structures is taken into account. However, in this simulation it is assumed that $r_{eff} = 0.12$ at all times, which can actually increase (to ~ 0.2), if neighboring lines switch in the opposite direction as discussed earlier. This increase in r_{eff} will further lower $j_{avg\text{-}reliability}$. Hence, impact of switching states of signal lines on allowed current density design rules should also be considered.

CONCLUSIONS

In conclusion, we have demonstrated a methodology which compares the effect of interconnect reliability and performance in determining the optimal signal line length. It should be noted that we use a self-consistent approach for determining the maximum allowed current density limit. It is overly pessimistic to use the DC EM current density as this limit, and overly optimistic to use the AC EM current density as this limit without accounting for self-heating. For the low-k/Cu systems studied here, it has been shown that as long as point-to-point interconnect performance is optimized, EM design limits for those signal lines will be satisfied.

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