# Modeling and Analysis of Via Hot Spots and Implications for ULSI Interconnect Reliability

Sungjun Im, Kaustav Banerjee and Kenneth E. Goodson
Center for Integrated Systems, Stanford University, CA 94305
Phone: 650-736-0044; Fax: 650-723-7657; E-mail: sjim@stanford.edu

## ABSTRACT

The prediction of hot spot temperatures and positions in interconnect and via systems is necessary for improved thermal design to minimize electromigration, stress migration, and high-current failures. While some thermal models are available for multilevel interconnect systems, the effects of vias are either neglected or treated very approximately. This paper derives an accurate analytical model for estimating interconnect and via temperatures, and also verifies the model using finite-element simulations. The model shows that hot spot locations and the overall temperature field in the interconnect structure are strongly affected by via and line dimensions. A critical condition for hot spot formation within the vias has been presented for the first time. Additionally, a new analytical model for estimating the temperature rise in a multilevel interconnect system has also been derived, which incorporates the effect of via self-heating. This work provides the basis for constitutive design rules considering hot spot locations and temperature profiles in interconnect systems.

## INTRODUCTION

In advanced ULSI systems, interconnect Joule heating becomes more severe due to aggressive technology scaling. It has been shown that the global interconnect temperatures will significantly increase despite negligible changes in the chip power density [1]. Accurate estimates of interconnect temperature rise must consider heat conduction and generation by the densely embedded vias. Recently, the effect of vias on reducing the interconnect temperature has been addressed assuming isothermal vias at a reference temperature [2, 3]. However, more accurate modeling must consider the heat generation and temperature rise within the via. Previous works on the thermal analysis of vias relied mostly on finite element simulations for a specific modeling geometry and boundary conditions [4-7]. These simulations are accurate for a given geometry but do not lead to generalized design guidelines. In this paper, a new analytical model is presented to evaluate the temperature rise within the via structure coupled with the interconnect line as a boundary condition using extended surface analysis. The predictions can be used for investigating via hot spot effects of stacked vias, high aspect ratio DRAM contacts and vertical inter-layer interconnects (VILICs) in 3-D ICs [8] as well as conventional multilevel VLSI interconnects.

## ANALYTICAL MODELING

In this section, the steady-state temperature fields of interconnects and vias embedded in a dielectric medium are derived using one-dimensional extended surface analysis [9]. The generalized governing equation is modified for the simple interconnect and via configuration. In addition, the shape factors for various model geometries and boundary conditions are discussed.

### *Modeling Methodology*

Consider a cylindrical thermal conductor in Fig. 1 (a). Although a non-zero temperature gradient exists along the radial (r) direction [10], the temperature change is dominant in the longitudinal (x) direction for a long metal conductor with a small cross section and high thermal conductivity. The error induced by using one-dimensional solutions for extended surface analysis is less than 1 % even for relatively large cross sections [11].

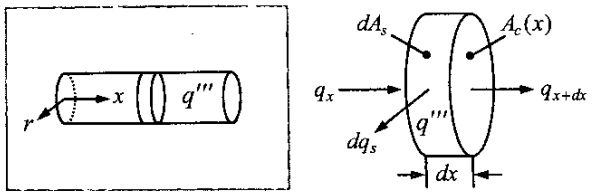



FIGURE 1. Schematic of (a) a conducting wire embedded in a dielectric medium and (b) a control volume showing energy balance.

The conservation of energy requires that the net heat flow into the control volume ($q_x - q_{x+dx}$) plus the volumetric rate of the thermal energy generation ($q'''$) must equal the rate of energy transfer out of the control volume ($dq_s$) as shown in Fig. 1 (b). The differential heat rate $dq_s$ can be expressed as

$$dq_s = S' dx k_d (T - T_\infty) \ , \qquad (1)$$

where $S'$ is the shape factor per unit length of the wire, $k_d$ is the thermal conductivity of the dielectric, and $T_\infty$ is the temperature of the surroundings far from the metal surface. It should be noted that $S'$ is a function of only geometric parameters, which describes the multi-dimensional conduction heat flow from the metal surface into the medium. It can be extracted from numerical simulations using finite element methods (FEM) [12], the superposition of temperature fields [13], experimental data [14], and the quasi-analytical modeling using Schwarz-Christoffel transformations [15-17] for the specific geometry and boundary conditions. Assuming one-dimensional steady-state conduction in the x direction, uniform volumetric heat generation ($q'''$), and negligible radiation heat loss, the conservation of energy on the control volume combined with *Fourier's law* results in

$$\frac{d}{dx}\left(k_m A_c \frac{dT}{dx}\right) - S' k_d (T - T_\infty) + q''' A_c = 0 \ , \qquad (2)$$

where $k_m$ is the metal conductor thermal conductivity and $A_c$ is the cross-sectional area, which may be spatially varying as for the tapered vias. In order to solve (2), two appropriate boundary conditions must be applied at both ends of the wire. For constant $k_m$ and $A_c$, (2) can be further simplified. For a single line and vias in Fig. 2, heat conduction within the interconnect and the via can be assumed to be one-dimensional in the x and y directions respectively. The governing equations for the line and the via are

$$\frac{d^2\theta_m(x)}{dx^2} - m_m^2 \theta_m(x) = -\frac{q'''_m}{k_m} \ , \qquad (3)$$

$$\frac{d^2\theta_v(y)}{dx^2} - m_v^2 \theta_v(y) = -\frac{q'''_v}{k_v} \ , \qquad (4)$$

0-7803-7352-9/02/$17.00 ©2002 IEEE



IEEE 02CH37320. 40th Annual International Reliability Physics Symposium, Dallas, Texas, 2002

where $\theta_m(x)$ and $\theta_v(y)$ are the temperature rises of the interconnect and the via with respect to the reference temperature, $T_0$, defined as $\theta_m(x) \equiv T_m(x)-T_0$ and $\theta_v(y) \equiv T_v(y)-T_0$, respectively. The thermal conductivity $k_m$ is that of the interconnect, and $k_v$ is the via thermal conductivity. The quantities $m_m$ and $m_v$ are the reciprocals of healing lengths for the interconnect and the via, respectively,

$$m_m \equiv \sqrt{\frac{S_m' k_d}{A_m k_m}} = \sqrt{\frac{S_m' k_d}{w \cdot h_m k_m}} , \quad (5)$$

$$m_v \equiv \sqrt{\frac{S_v' k_d}{A_v k_v}} = \sqrt{\frac{4 S_v' k_d}{\pi D^2 k_v}} , \quad (6)$$

where $S_m'$ and $S_v'$ are the shape factors per unit length of the interconnect and the via, respectively, $A_m$ is the cross-sectional area of the interconnect, $A_v$ is the cross-sectional area of the via, $w$ is the interconnect width, $h_m$ is the interconnect height, and $D$ is the via diameter. The quantities $q_m'''$ and $q_v'''$ are volumetric heat generations due to Joule heating in the line and the via, respectively,

$$q_m''' \equiv \frac{I^2 \rho_m}{(w \cdot h_m)^2} , \qquad q_v''' \equiv \frac{16 I^2 \rho_v}{\pi^2 D^4} , \quad (7)$$

where $\rho_m$ is the interconnect electrical resistivity and $\rho_v$ is the via electrical resistivity. Although the current flow ($I$) through the interconnect and the via is the same, $q_m'''$ and $q_v'''$ are different due to the difference in their cross-sectional areas and resistivities. Two boundary conditions for solving (3) are the adiabatic boundary condition at the center of the line ($x$=0) due to symmetry, and the constant temperature rise at the end of the line ($x$=$L$/2) which corresponds to the temperature rise at the junction between the line and the via, $\theta_J$,

$$\left.\frac{d\theta_m}{dx}\right|_{x=0} = 0 , \qquad \theta_m\left(x=\frac{L}{2}\right) = \theta_J . \quad (8)$$

The boundary conditions for solving (4) are the constant temperature rise ($\theta_J$) at the top ($y$=0), and zero temperature rise ($\theta$=0) at the bottom ($y$=$h_v$) of the via,

$$\theta_v(y=0) = \theta_J , \qquad \theta_v(y=h_v) = 0 . \quad (9)$$

The solutions to (3) and (4) with the boundary conditions (8) and (9) are

$$\theta_m(x) = \theta_J\left[\frac{\cosh(m_m x)}{\cosh(m_m L/2)}\right] + \left(\frac{q_m'''}{k_m m_m^2}\right)\left[1-\frac{\cosh(m_m x)}{\cosh(m_m L/2)}\right] , \quad (10)$$

$$\theta_v(y) = \theta_J\left\{\frac{\sinh[m_v(h_v-y)]}{\sinh(m_v h_v)}\right\} + \left(\frac{q_v'''}{k_v m_v^2}\right)\left\{1-\frac{\sinh[m_v(h_v-y)+\sinh(m_v y)]}{\sinh(m_v h_v)}\right\} . \quad (11)$$

The second terms in the expressions for $\theta_m(x)$ and $\theta_v(y)$ account for the additional Joule heating effects due to current flowing through the interconnect and the via, respectively. It is important to note that $\theta_m(x)$ and $\theta_v(y)$ are no longer independent of each other, but closely linked by $\theta_J$. Therefore, in order to completely describe $\theta_m(x)$ and $\theta_v(y)$, $\theta_J$ must be determined by solving the heat flow continuity equation at the junction between the interconnect and the via,

$$-k_m A_m \left.\frac{d\theta_m(x)}{dx}\right|_{x=L/2} = -k_v A_v \left.\frac{d\theta_v(y)}{dy}\right|_{y=0} . \quad (12)$$

Substituting (10) and (11) into (12) yields

$$\theta_J = \frac{A_m\left(\frac{q_m'''}{m_m}\right)\tanh\left(\frac{m_m L}{2}\right)}{k_m A_m m_m \tanh\left(\frac{m_m L}{2}\right) + k_v A_v m_v \coth(m_v h_v)} + \frac{A_v\left(\frac{q_v'''}{m_v}\right)\left[\coth(m_v h_v) - \operatorname{csch}(m_v h_v)\right]}{k_m A_m m_m \tanh\left(\frac{m_m L}{2}\right) + k_v A_v m_v \coth(m_v h_v)} . \quad (13)$$

This approach neglects the 3D conduction effect existing at the ends of the interconnect, although this is relatively unimportant when the interconnect thermal conductivity is high, as in the case of Cu. In addition, the one-dimensional assumption becomes more reasonable for the long global wires. These analytical expressions for the interconnect and via temperature fields can be used for both semi-infinite media and finite thickness media simply by modifying $m_m$ in (5) with relevant $S_m'$ from the Appendix. This methodology can be applied to more complicated multilevel interconnect and via configurations with thermal coupling effects by establishing and solving simultaneous equations similar to (10), (11) and (13) for the whole system.

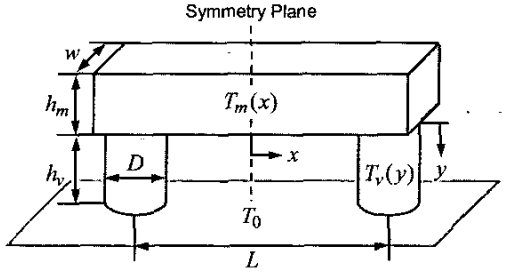



FIGURE 2. Modeling geometry representing a single line and vias in a dielectric medium. The bottom surfaces of the vias are attached to the constant temperature ($T_0$) surface.

### *Shape Factors*

The accurate determination of $S'$ is the most important step for using previously derived analytical models. The shape factor for a single isolated line in a semi-infinite medium can be calculated from [12-15], and it can be shown that [12] provides the best agreements with finite element simulation results. For a single line in a finite thickness medium, $S'$ can be obtained from [16]. The shape factor for the uniformly separated infinite number of parallel lines was proposed in [2], where heat dissipation from the top and side surfaces were ignored. The shape factors for a vertical cylinder in a semi-infinite medium, which are required for calculating via temperature fields, can be found in [9, 18]. The various embedded structures and their shape factors are shown in Table 1 in the Appendix.

Figure 3 plots shape factors for a single line and multiple lines subject to different boundary conditions as a function of $t_i/w$, where $t_i$ is the underlying insulator thickness. The predictions based on [12], [16] and [2] reveal good agreements with finite element simulations for all three cases; a single line in a semi-infinite medium (case 1), a

single line in a finite medium (case 2), and infinite number of horizontally placed parallel lines in a finite medium (case 3). For the simulations of case 3, the metal spacing, $d$, is assumed to be same as the metal width, $w$. For a single isolated line (case 1, 2), it can be observed that the effect of finite thickness medium is negligible. The shape factor for case 3 shows a dramatic decrease due to thermal coupling. For very small $t_i$, the presence of neighboring wires does not affect the temperature rise and the shape factors of adjacent lines. As $t_i$ increases, the heat flux from adjacent wires overlaps, which increases the temperature of the neighboring wires. Therefore, $S'$ decreases for a given heat generation of a line. Although the shape factor based on [2] neglects the heat loss from the top and side surfaces of the line, it shows a good agreement with simulation results for a finite thickness medium with the passivation layer of 2 μm. In this paper, case 1 and 3 are used and the corresponding shape factors are based on [12] and [2] respectively. The shape factors for vias are adopted from [9].

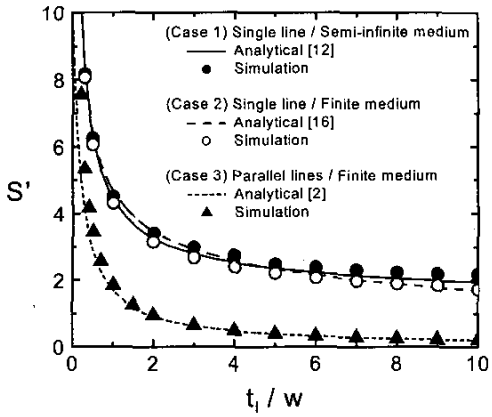



FIGURE 3. Comparison of shape factors based on analytical predictions ( [2], [12] and [16] ) with finite element simulations for three difference cases. The simulation parameters are $w$=0.5 μm, $h_m$=1 μm, q'''=$2\times10^{12}$ W/m$^3$ ($j_{rms}$= $9.53\times10^5$ A/cm$^2$, $\rho_m$=$2.2\times10^{-8}$ Ω-m), $k_m$=400 W/m-K, and $k_d$=0.25 W/m-K. The variable is $t_i$ for all cases, and passivation thickness of 2 μm is assumed for a finite medium.

## RESULTS AND DISCUSSION

### *Via Self-Heating*

The via self-heating effect is investigated for a single interconnect and vias in a semi-infinite medium shown in Fig. 2. The temperature profiles of the interconnect and the via are predicted based on our analytical models and verified by FEM simulations. Among various interconnect and via dimensions affecting their temperature fields, the effects of via diameter variations are considered first. The via diameter ($D$) might be equal to or smaller than the line width ($w$) due to different line widths of adjacent levels and fabrication processes. Therefore, the effects of via diameter variations are considered with the fixed via height ($h_v$=0.8 μm) and the metal width ($w$=0.3 μm). All simulation parameters in this work are based on the global lines of a 100 nm technology node and a worst-case current density, $j_{rms}$, of $1.4\times10^6$ A/cm$^2$ is assumed for the interconnect line according to ITRS [19]. The current flow ($I$) of 3.36 mA, calculated from this current density and the metal cross-section, is applied as an excitation load for electro-thermal FEM simulations. The via separation is assumed to be 100 μm.

Figure 4 (a) shows the predictions of temperature distributions along the interconnect for different via diameters. The temperature distributions are shown for half of the line due to symmetric temperature profiles across the center of the line (x=0). A comparison reveals good agreement with the simulation result for $D/w$=0.2 ($D$=0.06 μm, $w$=0.3 μm). Despite a small via height ($h_v$=0.8 μm), the hot spots occur within the via for $D/w$ < 0.38. As the via diameter decreases, via Joule heating significantly increases due to its fourth order dependence on $D$ as shown in (7). The interconnect temperature profiles significantly change with via diameters despite fixed parameters of interconnects. For large via diameters, via self-heating is negligible. Vias act as efficient heat conduits rather than heat sources. They contribute to lowering the average temperature of the interconnect due to their high thermal conductivities. In this case, the maximum temperature occurs at the center of the line (x=0). However, for small via diameters below a certain critical value (0.11 μm in this case), the temperature at the end of the line (x=50 μm) is higher than that at the center. This situation implies that a hot spot is formed within the via in order to satisfy the heat flow continuity requirement. As shown in Fig. 4 (b), below this critical via diameter, the hot spot for the overall interconnect and via structure is actually located within the via. The via temperatures rapidly increase with decreased $D/w$ ratios. The maximum via temperature can reach more than twice the maximum line temperature for the $D/w$ ratio of 0.15. The prediction of via temperature profile is verified by the FEM simulation for $D/w$=0.2 ($D$=0.06 μm, $w$=0.3 μm). Figure 5 shows a temperature contour plot for $D/w$=0.2 where a hot spot is formed 0.32 μm below the top of the via.

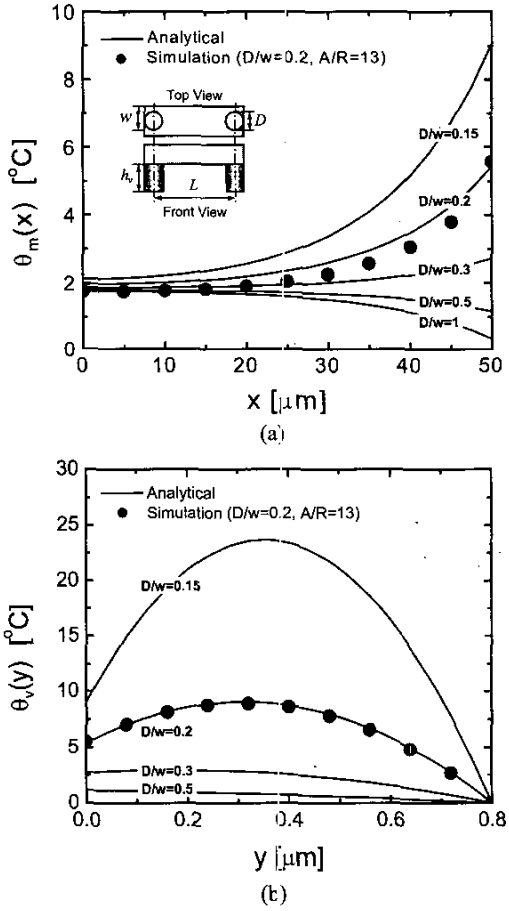



FIGURE 4. Temperature distributions along (a) the single interconnect and (b) the via in a semi-infinite medium for various $D/w$ ratios. The line width ($w$) is fixed at 0.3 μm and the via diameters ($D$) are varied ($D$=0.045-0.3 μm, A/R=2.7-17.8). The simulation parameters are $L$=100 μm, $h_m$=$h_v$=0.8 μm, $k_d$=0.19 W/m-K, $\rho_m$=$2.2\times10^{-8}$ Ω-m, $j_{rms}$(line)=$1.4\times10^6$ A/cm$^2$, and $j_{rms}$(via)= $4.75\times10^6$ – $2.11\times10^8$ A/cm$^2$.

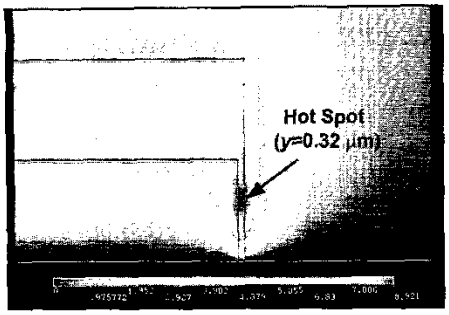
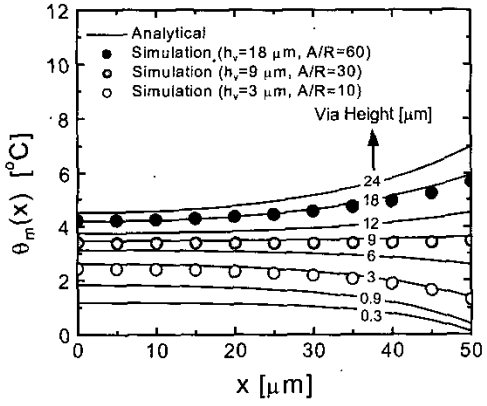
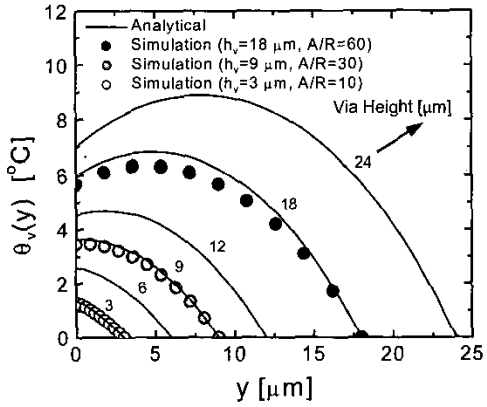



FIGURE 5. Temperature contour plot for $D/w$=0.2 ($D$=0.06 μm, $w$=0.3 μm). The via height is fixed at 0.8 μm and other parameters are same as in FIG. 4. The entire line ($L$=100 μm) is not shown here.

For conventional multilevel interconnects in 2-D ICs, the via heights range from 0.1 to 1.3 μm depending on metal levels and technology nodes, which yield via aspect ratios varying from 1.5 to 3 [1]. However, for vertical inter-layer interconnects (VILICs) in 3-D ICs, the via heights need to be larger than 15 μm to connect two chip layers across a thinned Si layer (~10-15 μm) and some dielectric layers [8]. The 3-D ICs fabricated by wafer bonding using polymer adhesives [20] require even larger VILIC heights compared to the Cu pad thermocompression method [21]. Therefore, the investigation of via height variation effects on hot spot positions is an important issue.




(a)

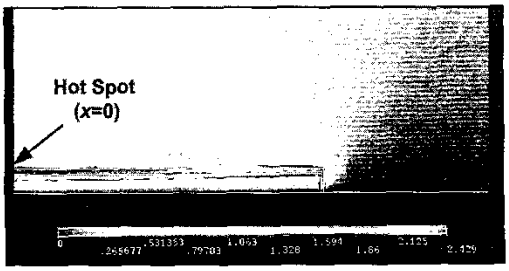



(b)

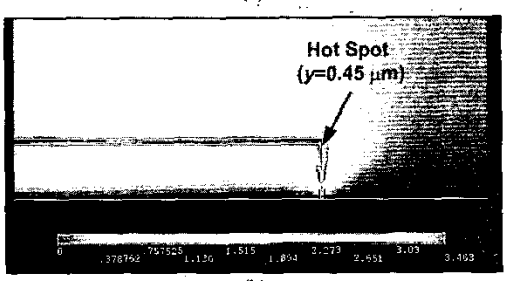
FIGURE 6. Temperature distributions along (a) the single interconnect, and (b) the vertical via in a semi-infinite medium for various via heights, $h_v$=0.3-24 μm (A/R=1-80). The simulation parameters are $D$=$w$=0.3 μm, $j_{rms}$(line) =1.4×10$^6$ A/cm$^2$, and $j_{rms}$(via)= 4.75×10$^6$ A/cm$^2$. Note that $D/w$=1 is assumed and other parameters are same as in FIG. 4.

Figure 6 (a) shows the predictions of temperature distributions along the interconnect for various via heights with fixed via diameter of 0.3 μm. The via diameter ($D$) is assumed to be same as the metal width ($w$) and the via aspect ratios are varied from 1 to 80. The predictions show good agreements with simulation results for three different via heights. For small via heights, via self-heating is negligible. However, as shown in Fig. 6 (b), beyond a critical via height (8.4 μm in this case), the hot spot for the overall interconnect and via structure is formed within the via. This hot spot position continues to move into the via (positive y direction) as the via height increases. The predictions of via temperature profiles are verified by simulations for three different via heights.

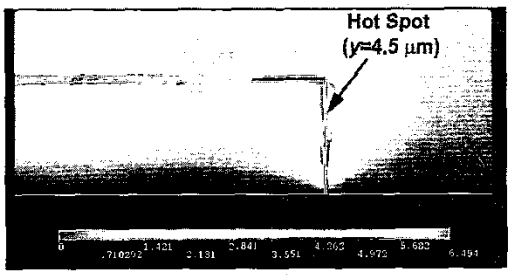
Figure 7 shows temperature contour plots with hot spot positions for three different via heights which are used for verifying the analytical predictions in Fig. 6. The hot spot positions significantly change depending on the via heights. A nearly constant interconnect temperature observed in Fig. 7 (b) is a characteristic of the hot spot transition regime. If the via height further increases, the hot spot is formed within the via as shown in Fig. 7 (c). The effects of via heights on the via temperatures and hot spot positions will be useful for investigating high aspect ratio vias such as DRAM contacts and stacked vias. The hot spots formed within the VILICs in 3-D ICs will significantly affect the reliability of adjacent bonding layers and interfaces.




(a)




(b)




(c)

FIGURE 7. Temperature contour plots from 3-D FEM electro-thermal simulations for three different via heights; (a) $h_v$=3 μm, $D$=0.3 μm (A/R=10), hot spot position: x=0, (b) $h_v$=9 μm, $D$=0.3 μm (A/R=30), hot spot position: y=0.45 μm, and (c) $h_v$=18 μm, $D$=0.3 μm (A/R=60), hot spot position: y=4.5 μm. Contour plots are shown for half of the line (0<x<50 μm). Other parameters are same as in FIG. 4.

*Hot Spot Positions*

For arbitrary interconnect and via dimensions, the via hot spot positions can be predicted by finding the value of y which satisfies the relation $d\theta_v(y)/dy=0$. The differential equation $d\theta_v(y)/dy=0$ can be solved numerically. The critical condition for which hot spots are formed within the via is dictated by $\theta_m(x=0) < \theta_J$, which gives rise to

$$\left[1-\left(\frac{q_m'''}{q_v'''}\right)\left(\frac{k_m}{k_v}\right)\left(\frac{m_v}{m_m}\right)^2\right]\cosh(m_v h_v) > 1 \quad . \qquad (14)$$

This is a transcendental inequality in $m_v$ with various coefficients ($q_m'''$, $q_v'''$, $k_m$, $k_v$, $m_m$, and $h_v$), which should be solved by numerical methods. Substituting expressions for $q_m'''$, $q_v'''$, $m_v$ and $m_m$ given by (5), (6) and (7) results in

$$\left[1-\left(\frac{\rho_m}{\rho_v}\right)\left(\frac{k_m}{k_v}\right)^2\left(\frac{\pi D^2}{4w\cdot h_m}\right)\left(\frac{S_v'}{S_m'}\right)^2\right]\cosh\left(\sqrt{\frac{4S_v' k_d}{\pi D^2 k_v}}\right) > 1 \quad . \qquad (15)$$

If the same material is used for interconnects and vias as in copper dual damascene processes, (15) can be further simplified to

$$\left[1-\left(\frac{A_v}{A_m}\right)\left(\frac{S_v'}{S_m'}\right)^2\right]\cosh\left[\sqrt{\left(\frac{S_v'}{A_v}\right)\left(\frac{k_d}{k_v}\right)}\right] > 1 \quad . \qquad (16)$$

It should be noted that (16) is not a function of via separation, $L$.

Figure 8 (a) shows the predictions of $\theta_J/\theta_m(x=0)$ as a function of $D/w$ with varying via separations for a single line in a semi-infinite medium. The $D/w$ ratios are varied by changing via diameters ($D$) for a fixed line width ($w$=0.3 μm). It shows two distinct regimes for hot spot positions. If $\theta_J/\theta_m(x=0) < 1$, hot spots occur at the center of the line, and if $\theta_J/\theta_m(x=0) > 1$, hot spots will be found within the via. For small $D/w$ ratios (< 0.38), $\theta_J/\theta_m(x=0) > 1$ and hot spots appear within the via despite a small via height ($h_v$=0.8 μm). It is shown that hot spots will not appear within the short via ($h_v$=0.8 μm) for $D/w$=1 as predicted in Fig. 4. The critical via diameter (0.11 μm in this case) for the hot spot transition is independent of $L$. If thermal coupling between adjacent wires are considered, the critical condition changes due to decreased $S_m'$. Figure 8 (b) shows the thermal coupling effects on the hot spot positions for various $D/w$ ratios and via separations. The critical $D/w$ ratio shifts to the lower values ($D/w$=0.28, $D$=0.084 μm) as thermal coupling between adjacent lines is taken into account.

The $D/w$ ratio can also be varied by increasing the line widths for a fixed via diameter ($D$=0.3 μm). If the line widths are varied, the critical $D/w$ ratio for the via hot spot formation is different from the case of varying $D$ as expected from (15). As shown in Fig. 9 (a), if the line width is greater than 4.62 μm ($w/D$=15.38, $D/w$=0.065), hot spots will be formed within the via for a single line in a semi-infinite medium. For the parallel line arrays, the critical line width shifts to the higher value as shown in Fig. 9 (b) ($w$=6.67 μm, $w/D$=22.2, $D/w$=0.045). These predictions imply that the closely spaced parallel interconnect arrays are less susceptible to the via hot spot formation at a given via diameter and a line width.

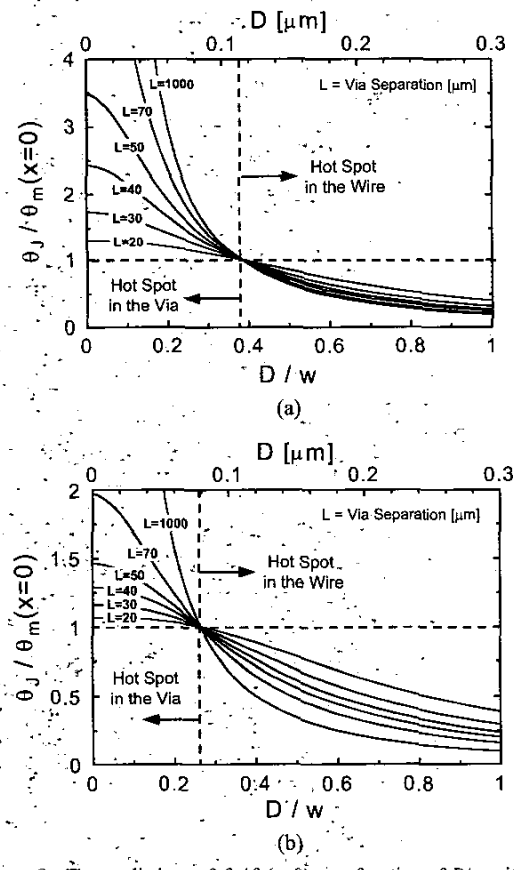



FIGURE 8. The predictions of $\theta_J/\theta_m(x=0)$ as a function of $D/w$ with varying via separations ($L$) for (a) a single line in a semi-infinite medium, and (b) infinite number of parallel lines in a confined medium. The $D/w$ ratios are varied by changing via diameters ($D$) for a fixed line width ($w$=0.3 μm). The via height ($h_v$) is 0.8 μm and other parameters are same as in FIG. 4.

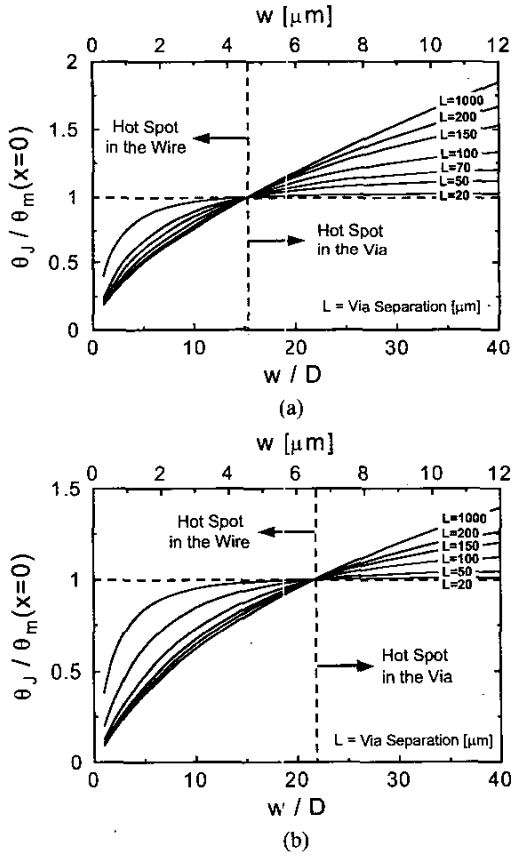



FIGURE 9. The predictions of $\theta_J/\theta_m(x=0)$ as a function of $w/D$ with varying via separations ($L$) for (a) a single line in a semi-infinite medium, and (b) infinite number of parallel lines in a confined medium. The $w/D$ ratios are varied by changing line widths ($w$) for a fixed via diameter ($D$=0.3 μm). The via height ($h_v$) is 0.8 μm and other parameters are same as in FIG. 4.

Since the hot spot positions are affected by via diameters, via heights, line widths and line heights, their correlations should be considered at the same time for more accurate predictions. Figure 10 shows the predictions of $\theta_J / \theta_m(x=0)$ with varying via heights for a single line in a semi-infinite medium. In Fig. 10 (a), the via diameters and the via heights are changed and other dimensions are fixed. The predictions are plotted as a function of the ratio of the via cross section to the line cross section ($A_v/A_m$). The critical cross sectional ratios and corresponding via diameters significantly change depending on the via heights. As the via height increases, the critical via diameters shift to the larger values. Figure 10 (b) shows the predictions of $\theta_J / \theta_m(x=0)$ as a function of $A_m/A_v$ with varying both the line width and the via height. It can be observed that the critical line width beyond which via hot spots are formed rapidly decreases as the via height increases. Figure 10 (c) shows the predictions of $\theta_J / \theta_m(x=0)$ as a function of $A_m/A_v$ with varying both the line height and the via height. As the via height increases, the critical line height decreases. Although the variations of line widths and heights linearly change the metal cross section in the same manner, their effects on critical conditions for hot spot formations are different. For example, at the same $A_m/A_v$ of 60, via hot spots occur for the wide line with the via height of 0.8 μm in Fig. 10 (b), but hot spots will not be formed within the via for the tall line even with a larger via height of 0.9 μm in Fig. 10 (c). The variations of line widths and heights change both $A_m$ and $S_m'$ in (16). However, $S_m'$ is a weak function of the line height and the effects of line height variations are less significant than those of line width variations, as can be seen from [2] in the Appendix.

Figure 11 shows the predictions of $\theta_J / \theta_m(x=0)$ with varying via heights for infinite number of parallel line arrays in a semi-infinite medium. Figure 11 (a) plots the predictions of $\theta_J / \theta_m(x=0)$ as a function of $A_v/A_m$ with varying via diameters and via heights. Figure 11 (b) and 11 (c) show the predictions of $\theta_J / \theta_m(x=0)$ as a function of $A_m/A_v$. In Fig. 11 (b), the line width and the via height are varied. In Fig. 11 (c), the variables are line heights and via heights. For all three cases, the predictions are similar to the cases of a single line in a semi-infinite medium shown in Fig. 10. The major difference is that the critical conditions shift for a given via height. In Fig. 11 (a), the critical via diameter moves to the lower value than that of Fig. 10 (a) for a given via height. In addition, the range of variations of critical via diameters decreases if thermal coupling is considered. As shown in Fig. 11 (c), the thermal coupling effects are significant for the variation in line heights. The hot spots will not be formed within the via even for the large values of line heights and via heights. The parametric analyses show that the critical condition for via hot spot formations is strongly dependent on interconnect and via dimensions and their complex correlations, which has significant implications for interconnect and via reliability issues induced by local hot spots.

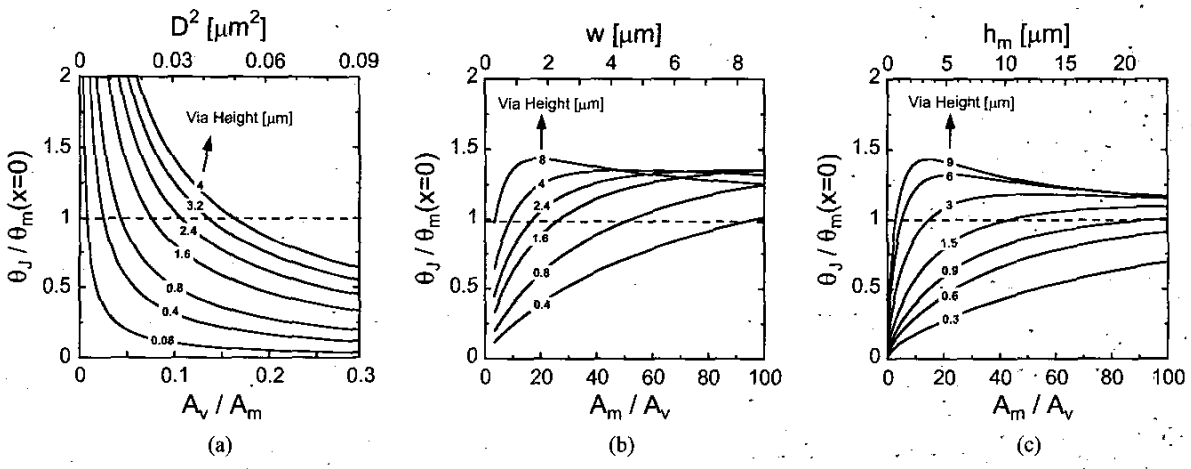



FIGURE 10. The predictions of $\theta_J / \theta_m(x=0)$ with varying via heights for a single line in a semi-infinite medium. (a) The via diameter ($D$) is a variable ($w$=0.3 μm, $h_m$=0.8 μm). (b) The line width ($w$) is a variable ($D$=0.3 μm, $h_m$=0.8 μm). (c) The line height ($h_m$) is a variable ($D$=$w$=0.3 μm). For all cases, $L$=100 μm and the current flow ($I$) of 3.36 mA are assumed. The current densities, $j_{rms}$(line) and $j_{rms}$(via), are calculated from this current flow.

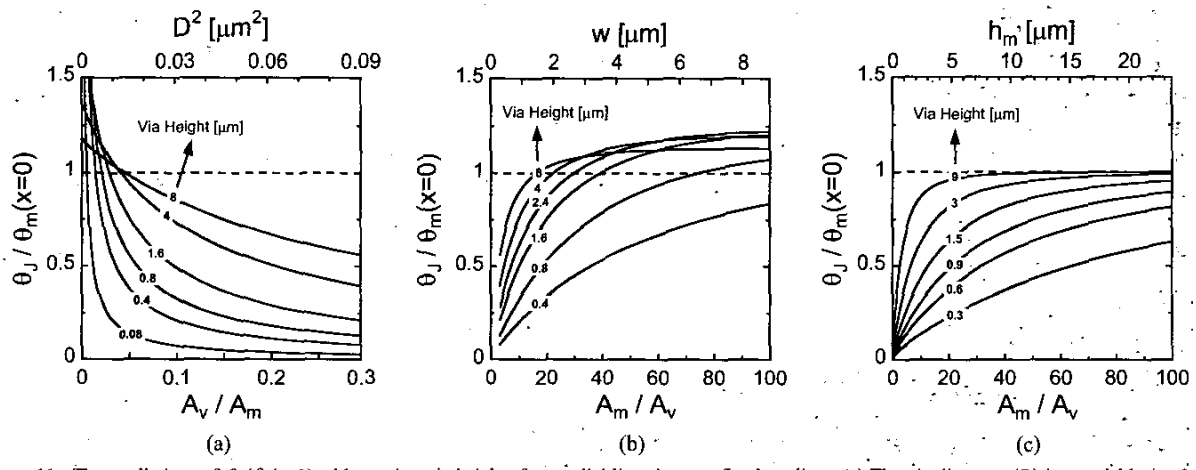



FIGURE 11. The predictions of $\theta_J / \theta_m(x=0)$ with varying via heights for parallel lines in a confined medium. (a) The via diameter ($D$) is a variable ($w$=0.3 μm, $h_m$=0.8 μm). (b) The line width ($w$) is a variable ($D$=0.3 μm, $h_m$=0.8 μm). (c) The line height ($h_m$) is a variable ($D$=$w$=0.3 μm). The spacing between the parallel lines is assumed same as the line width, and vias are attached to only one of these parallel lines. Other parameters are same as in FIG. 10.

*ILD Thermal Conductivity*

In addition to geometric dimensions and boundary conditions, material properties of line, via and inter-layer dielectrics (ILD) also affect the hot spot positions as can be expected from (15). Figure 12 shows the predictions of $\theta_J / \theta_m(x=0)$ as a function of ILD thermal conductivity for various via filling materials. Infinite numbers of parallel Cu lines are considered and two different $D/w$ ratios are compared. Use of Tungsten (W) via results in larger values of $\theta_J / \theta_m(x=0)$ compared to Al and Cu vias. This is due to its lower thermal conductivity and higher electrical resistivity, which yield more via self-heating and higher via temperature rise. For a large $D/w$ ratio ($D/w$=1), the effects of ILD and via thermal conductivities are negligible and hot spots will be formed at the center of the line. However, for a small $D/w$ ratio ($D/w$=0.3), hot spots can be formed in the via. The critical ILD thermal conductivity for via hot spots depends on the via filling materials. For W via with $D/w$=0.3, via hot spots occur for almost all the range of ILD thermal conductivity. However, for Cu vias with $D/w$=0.3, via hot spots appear for ILD thermal conductivities greater than 0.32 W/m-K.

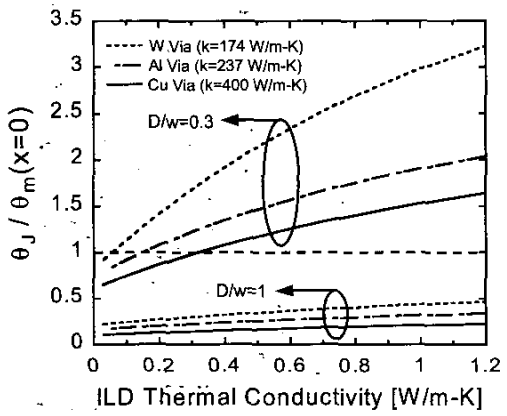



FIGURE 12. The predictions of $\theta_J / \theta_m(x=0)$ as a function of thermal conductivity of ILD materials for three different via filling materials (Cu, Al and W). Two different $D/w$ ratios are compared with varying via diameter ($D$). $w$=0.3 μm, $h_v$=0.8 μm, $L$=100 μm, $\rho_{Cu}$=2.2×10$^{-8}$ Ω-m, $\rho_{Al}$= 2.74×10$^{-8}$ Ω-m, $\rho_W$=5.3×10$^{-8}$ Ω-m. The analysis is based on infinite number of parallel Cu lines in a finite medium are considered. Other parameters are same as in FIG. 4.

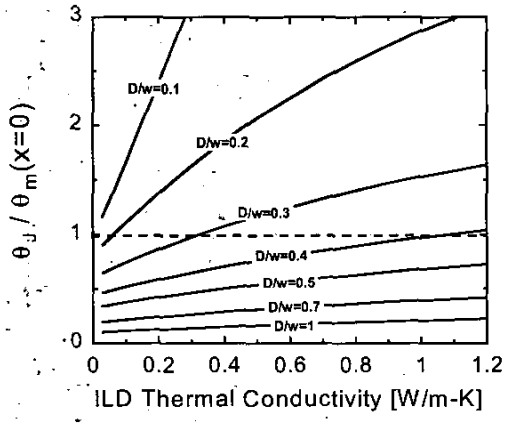



FIGURE 13. The predictions of $\theta_J / \theta_m(x=0)$ as a function of thermal conductivity of ILD materials for Cu vias with different $D/w$ ratios. The via diameters are varied ($w$=0.3 μm) and infinite number of parallel Cu lines in a finite medium are considered. Other parameters are same as in FIG. 4.

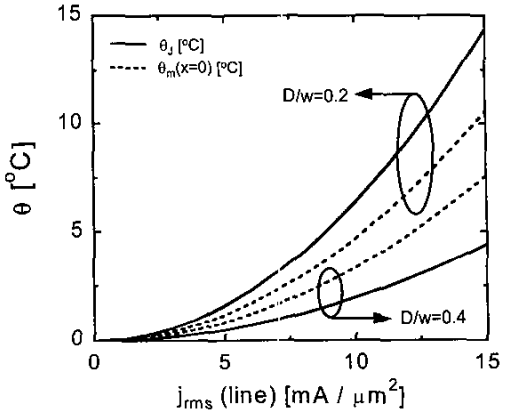



FIGURE 14. The predictions of $\theta_J$ and $\theta_m(x=0)$ as a function of $j_{rms}$(line) for two different $D/w$ ratios. The via diameters are varied ($w$=0.3 μm). The analysis is based on infinite number of parallel Cu lines in a finite medium are considered. Other parameters are same as in FIG. 4.

Furthermore, electromigration failure arising from void nucleation in Cu vias is an important reliability concern. Additionally, vias can also suffer from thermally-induced damage (due to melting) under high-current stress conditions such as electrostatic discharge [22]. Therefore, the investigation of the temperature rise within the via and the detection of via hot spots are useful for analyzing temperature dependent via failures. The accurate predictions of hot spot positions with respect to the bottom of the via are also important for Cu vias fabricated by dual damascene processes. Figure 13 shows the predictions of $\theta_J / \theta_m(x=0)$ as a function of ILD thermal conductivity for Cu vias with various $D/w$ ratios. The thermal coupling between adjacent wires is considered. Within the range of typical low-k dielectric material thermal conductivities (k<1 W/m-K), Cu vias with small $D/w$ ratios are exposed to the possibility of via hot spot formation.

Finally, Fig. 14 compares the temperature rises at the top of the via ($\theta_J$) and the center of the line ($\theta_m(x=0)$) as a function of current density in the line for two different $D/w$ ratios. The current density values cover the range of typical stress current densities. The configuration of an infinite number of parallel Cu lines is considered to include the thermal coupling effect. The critical condition for via hot spots is not a function of current as expected from (14-16). For $D/w$=0.2, $\theta_J > \theta_m(x=0)$ for the whole range of $j_{rms}$(line) and hot spots will be formed within the via. For $D/w$=0.4, $\theta_J < \theta_m(x=0)$ for the whole range of $j_{rms}$(line) and hot spots will be located at the center of the line. It should be noted that increasing current for the fixed line and via dimensions only contributes to increasing the absolute values of $\theta_J$ and $\theta_m(x=0)$. The ratio of $\theta_J / \theta_m(x=0)$ remains constant independent of current stress.

## MULTILEVEL INTERCONNECTS

The analytical models derived earlier for a single level of metal and vias can be modified to estimate the line and via temperature fields in multilevel interconnect systems in advanced high performance ICs. For closely spaced metal lines in the same level, the lateral temperature variations are negligible. Therefore, the temperature at the bottom of the via in the $n^{th}$ level can be assumed to be the average temperature of the line in the $(n\text{-}1)^{th}$ level as shown in Fig. 15. The solutions derived for a single level of lines and vias (10, 11 and 13) can be used for multilevel systems by calculating the average temperature rise of the $n^{th}$ line incorporating via self-heating effects. The temperature rise of the $n^{th}$ metal line with respect to the average temperature of the interconnects in the $(n\text{-}1)^{th}$ level is

$$\theta_n(x) \equiv T_n(x) - \overline{T_{n-1}} = \theta_{J,n}\left[\frac{\cosh(M_n x)}{\cosh(M_n L_n/2)}\right] + \left(\frac{Q_n'''}{k_m M_n^2}\right)\left[1 - \frac{\cosh(M_n x)}{\cosh(M_n L_n/2)}\right] \quad (17)$$

$$(n=1, 2, 3, \cdots, N),$$

where $T_{n-1}$ is the average line temperature in the $(n\text{-}1)^{th}$ level, $M_n$ is the reciprocal of the healing length, $L_n$ is the via separation, $Q_n'''$ is the volumetric heat generation due to interconnect Joule heating in the $n^{th}$ level, $k_m$ is the interconnect thermal conductivity, and $N$ is the total number of the metal levels. The average temperature rise of the $n^{th}$ line ($\theta_n$) with respect to $T_{n-1}$ can be obtained from (17) as

$$\overline{\theta_n} \equiv \overline{T_n} - \overline{T_{n-1}} = \theta_{J,n}\left[\frac{\tanh(M_n L_n/2)}{(M_n L_n/2)}\right] + \left(\frac{Q_n'''}{k_m M_n^2}\right)\left[1 - \frac{\tanh(M_n L_n/2)}{(M_n L_n/2)}\right] \quad (18)$$

$$(n=1, 2, 3, \cdots, N),$$

where $\theta_{J,n}$ is the temperature rise at the junction between the $n^{th}$ line and the $n^{th}$ via with respect to $T_{n-1}$ ($\theta_{J,n} \equiv T_{J,n} - T_{n-1}$),

$$\theta_{J,n} = \frac{A_n\left(\frac{Q_n'''}{M_n}\right)\tanh\left(\frac{M_n L_n}{2}\right)}{k_m A_n M_n \tanh\left(\frac{M_n L_n}{2}\right) + k_v a_n m_n \coth(m_n h_n)} + \frac{a_n\left(\frac{q_n'''}{m_n}\right)\left[\coth(m_n h_n) - \operatorname{csch}(m_n h_n)\right]}{k_m A_n M_n \tanh\left(\frac{M_n L_n}{2}\right) + k_v a_n m_n \coth(m_n h_n)} \quad (19)$$

$$(n=1, 2, 3, \cdots, N),$$

where $A_n$ is the cross-sectional area of the interconnect, $a_n$ is the cross-sectional area of the via, $m_n$ is the reciprocal of the via healing length of the via, $h_n$ is the via height, $q_n'''$ is the volumetric heat generation due to via self-heating for the $n^{th}$ level, and $k_v$ is the via thermal conductivity. The quantities $M_n$ and $m_n$ are given by

$$M_n \equiv \sqrt{\frac{S_n' k_d}{A_n k_m}} = \sqrt{\frac{S_n' k_d}{w_n \cdot H_n k_m}}, \quad (20)$$

$$m_n \equiv \sqrt{\frac{s_n' k_d}{a_n k_v}} = \sqrt{\frac{4 s_n' k_d}{\pi D_n^2 k_v}} \quad (21)$$

$$(n=1, 2, 3, \cdots, N),$$

where $S_n'$ and $s_n'$ are the shape factors per unit length of the interconnect line and the via in the $n^{th}$ level with respect to the $(n\text{-}1)^{th}$ level, respectively, $w_n$ is the line width, $H_n$ is the line height, and $D_n$ is the via diameter for the $n^{th}$ level. If the heat dissipations from the upper levels are considered by using relevant shape factors ($S_n'$) for a given level, the average line temperature rise in the $n^{th}$ level with respect to the substrate temperature ($T_0$), $\Theta_n$, can be obtained by adding $\theta_n$ for all levels, $n$,

$$\overline{\Theta_n} \equiv \overline{T_n} - T_0 = \sum_{n=1}^{N} \overline{\theta_n}. \quad (22)$$

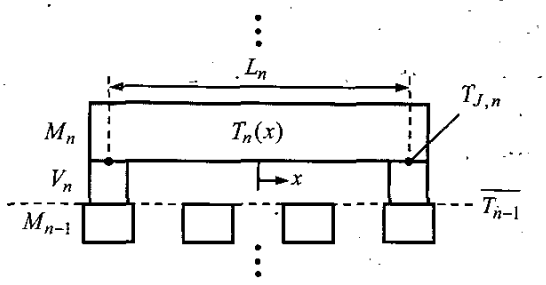



FIGURE 15. Modeling geometry representing lines in the $n^{th}$ level ($M_n$) and the $(n\text{-}1)^{th}$ level ($M_{n-1}$) with vias ($V_n$) connecting $M_n$ and $M_{n-1}$. Metal lines in adjacent levels are orthogonal to each other.

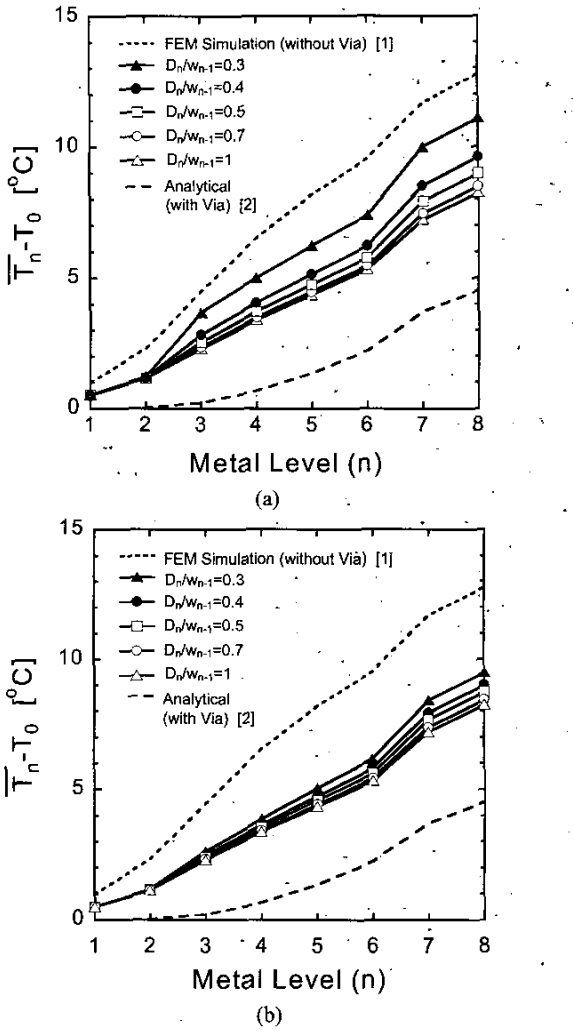



FIGURE 16. The predictions of temperature rises of the interconnect lines at the $n^{th}$ level as a function of metal levels for various via diameters. (a) The current flows in the $n^{th}$ vias are assumed to be the same as in the $n^{th}$ lines for all levels. (b) No current flow in the via is assumed. The via separations are 1, 5, 15, 30, 50, 100, 250, and 500 μm, for $n$=1 through $n$=8, respectively. The values of $S_n'$ are 0.05, 0.04, 0.1, 0.11, 0.13, 0.16, 0.3, and 0.6, for $n$=1 through $n$=8, respectively.

Figure 16 shows the predictions of average temperature rises of the lines at the $n^{th}$ level with varying via diameters. All parameters are based on 100 nm technology node proposed by ITRS [19]. For via separations, the values proposed in [2] are used for each of the metal layers. For estimating the interconnect and via Joule heating,

the RMS current density, $j_{rms}$, of $4.85\times10^5$ A/cm$^2$ is calculated from the value of $J_{max}$ ($1.4\times10^6$ A/cm$^2$) assuming $J_{max}=J_{peak}$ and a duty factor of 0.12. This value of $j_{rms}$ is applied to all the wires and corresponding current ($I$) at each level are calculated from wire cross sections. The diameter of the $n^{th}$ level via, $D_n$, is assumed to be smaller than the line width at the $(n\text{-}1)^{th}$ level by defining a scaling factor, $\alpha$, expressed as $D_n \equiv \alpha \times w_{n-1}$ $(0 < \alpha < 1)$. In practice, since all the vias do not carry the same amount of current as in the wires, two extreme cases are considered. In Fig. 16 (a), it is assumed that the current flow in the $n^{th}$ via is the same as that of the $n^{th}$ lines. In Fig. 16 (b), it is assumed that there is no current flow within the via for all levels. The values of $S_n'$ are extracted from FEM simulation results based on [1], which account for complex thermal coupling in the three dimensional arrays of interconnects. The values of $s_n'$ for the vias are calculated using [9] in the Appendix.

Figure 16 (a) shows the predictions of the temperature rises as a function of metal level with varying via diameters ($D_n/w_{n-1}=\alpha$). It also compares the FEM simulation results where no vias were included [1], and the predictions based on the simple analytical model proposed in [2] that approximates all vias as perfect heat sinks and completely ignores via self-heating effects. It can be observed that the predictions based on the new analytical model derived in this study exhibit intermediate values between the two cases analyzed in [1] and [2]. The main reason for this difference is caused by the use of more accurate shape factors to account for complex three-dimensional heat conduction in the multilevel systems, and due to the inclusion of via self-heating effects. It is also shown that as the via diameters are scaled down with respect to the connected line widths, the estimated values of the temperature rise approach the conservative worst case values [1], where the vias were not included.

Figure 16 (b) shows the predicted values of the temperature rise when vias are assumed to carry no current. In this case, there is no via self-heating and the vias only contribute to conducting the heat generated in the upper levels of metal wires. It is instructive to note that even though there is no heat generation within the vias, the estimated values of the interconnect temperature rise are still significantly higher than the ones predicted based on [2]. Hence, temperature predictions in multilevel ULSI interconnect systems based on overly simplified assumptions can lead to underestimation of the interconnect temperature rise, and to aggressive current density design rules, that can seriously degrade interconnect reliability.

## CONCLUSIONS

In conclusion, an accurate analytical model for estimating interconnect and via temperatures has been derived using extended surface analysis, and the model predictions have been verified by 3-D electro-thermal finite element simulations. In addition, a critical condition for hot spot formation within the vias has been presented for the first time. Finally, a new analytical model for estimating the temperature rise in a multilevel interconnect system has also been derived, which incorporates the effect of via self-heating. It has been shown that hot spot locations and resultant temperature fields of interconnect and via structures are strongly affected by via and line dimensions, and by ILD thermal conductivities. It has also been shown that the via self-heating significantly affects the temperature distribution in high performance multilevel ULSI interconnects with significant implications for reliability.

## ACKNOWLEDGEMENTS

This work was supported by the MARCO Interconnect Focus Center. The authors would like to acknowledge Dr. Timothy D. Sullivan from IBM for his valuable comments.

## REFERENCES

[1] S. Im and K. Banerjee, "Full Chip Thermal Analysis of Planar (2-D) and Vertically Integrated (3-D) High Performance ICs," *Tech. Dig. IEDM*, 2000, pp. 727-730.

[2] T-Y Chiang, K. Banerjee and K. C. Saraswat, "Analytical Thermal Model for Multilevel VLSI Interconnects Incorporating Via Effect," *IEEE Electron Device Letters*, Vol. 23, Jan. 2002, pp. 31-33.

[3] T-Y Chiang and K. C. Saraswat, "Impact of Vias on the Thermal Effect of Deep Sub-Micron Cu/low-k Interconnects," *Symp. VLSI Tech.*, 2001, pp. 141-142.

[4] T. Kwok, T. Nguyen, P. Ho and S. Yip, "Current Density and Temperature Distributions in Multilevel Interconnection with Studs and Vias," *Proc. IRPS*, 1987, pp. 130-135.

[5] A. Enver and J. J. Clement, "Finite Element Numerical Modeling of Currents in VLSI Interconnects," *VMIC*, 1990, pp. 149-156.

[6] K. Weide and W. Hasse, "3-Dimensional Simulations of Temperature and Current Density Distribution in a Via Structure," *Proc. IRPS*, 1992, pp. 361-365.

[7] J. T. Trattles, A. G. O'Neill and B. C. Mecrow, "Three-Dimensional Finite-Element Investigation of Current Crowding and Peak Temperatures in VLSI Multilevel Interconnects," *IEEE Trans. Electron Dev.*, Vol. 40, No. 7, 1993, pp. 1344-1347.

[8] K. Banerjee, S. J. Souri, P. Kapur, and K. C. Saraswat, "3-D ICs: A Novel Chip Design for Improving Deep Submicrometer Interconnect Performance and Systems-on-Chip Integration," *Proc. IEEE*, Vol. 89, No. 5, May 2001, pp. 602-633.

[9] F. P. Incropera and D. P. DeWitt, *Fundamentals of Heat and Mass Transfer*. New York: John Wiley & Sons, 1996, ch. 3, pp. 110-134.

[10] K. Banerjee, G. Wu, M. Igeta, A. Amerasekera, A. Majumdar and C. Hu, "Investigation of Self-Heating Phenomenon in Small Geometry Vias Using Scanning Joule Expansion Microscopy," *Proc. IRPS*, 1999, pp. 297-302.

[11] K. A. Gardner, "Efficiency of Extended Surfaces," *Trans. ASME*, Vol. 67, 1945, pp. 621-631.

[12] D. Chen, E. Li, E. Rosenbaum and S. Kang, "Interconnect Thermal Modeling for Accurate Simulation of Circuit Timing and Reliability," *IEEE Trans. CAD*, Vol. 19, No. 2, Feb. 2000, pp. 197-205.

[13] S. S. Kutateladze, *Fundamentals of Heat Transfer*, Academic Press, New York, 1963.

[14] R. V. Andrews, "Solving Conductive Heat Transfer Problems with Electrical-analogue Shape Factor," *Chem. Eng. Prog.*, Vol. 51, No. 2, Feb. 1955, pp. 67-71.

[15] D. Harmon, J. Gill, and T. Sullivan, "Thermal Conductance of IC Interconnects Embedded in Dielectrics," *IRW Final Report*, 1998, pp. 1-9.

[16] J. Gill, D. Harmon, J. Furukawa, and T. Sullivan, "Predicting Thermal Behavior of Interconnects," *IRW Final Report*, 1999, pp. 54-60.

[17] A. A. Bilotti, "Static Temperature Distribution in IC Chips with Isothermal Heat Sources," *IEEE Trans. Electron Dev.*, Vol. ED-21, Mar. 1974, pp. 217-226.

[18] General Electric Co. (Corporate Research and Development), Heat Transfer Data Book, Section 502, General Electric Company, Schenectady, New York, 1973.

[19] International Technology Roadmap for Semiconductors, 1999.

[20] P. Ramm et al., "Three Dimensional Metallization for Vertically Integrated Circuits," Microelectronic Engineering, 37/38, pp. 39-47, 1997.

[21] A. Fan, A. Rahman, and R. Reif, "Copper Wafer Bonding," Electrochemical and Solid-State Letters, Vol. 2 (10), pp. 534-536, 1999.

[22] K. Banerjee, A. Amerasekera, G. Dixit, N. Cheung, and C. Hu, "Characterization of Contact and Via Failure under Short Duration High Pulsed Current Stress," *Proc. IRPS*, 1997, pp. 216-220.

## APPENDIX

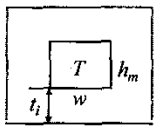
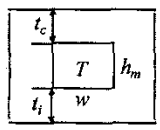
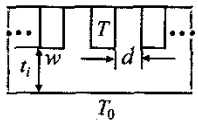
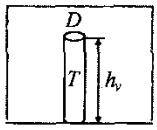
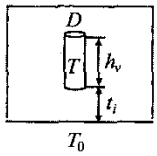
| System | Schematic | Shape factor per unit length, $S'$ |
|---|---|---|
| (Case 1)<br>Long parallelepiped in a semi-infinite medium |  | $S' = 1.86\left[\log\left(1+\frac{ti}{w}\right)\right]^{-0.66}\left(\frac{w}{h_m}\right)^{-0.1}$ [12]<br>$S' = \left(5.7+\frac{w}{2h_m}\right)\left\{\ln\left[3.5w^{-0.25}h_m^{-0.75}\left(t_i+\frac{h_m}{2}\right)\right]\right\}^{-1}$ [13]<br>$S' = 1.685\left[\log\left(1+\frac{t_i}{w}\right)\right]^{-0.59}\left(\frac{t_i}{h_m}\right)^{-0.078}$ [14]<br>$S' = \left(\frac{2}{\pi}\right)\ln\left[-1+C^2+2C(C^2-1)^{1/2}\right]$<br>$+\left(\frac{2}{\pi}\right)\ln\left[\frac{1}{3}+\frac{2}{3}\cosh\left(1+3^{-3/2}\pi+\frac{\pi w}{2t_i}\right)\right]$<br>$+\left(\frac{2}{\pi}\right)\ln\left\{1+\frac{\pi w}{2(t_i+h_m)}+\ln\left[1+\frac{\pi w}{2(t_i+h_m)}\right]\right\}$<br>where $C = 1+(h_m/t_i)$ [15] |
| (Case 2)<br>Long parallelepiped in a confined medium |  | $S' = \left(\frac{2}{\pi}\right)\ln\left[-1+C^2+2C(C^2-1)^{1/2}\right]$<br>$+\left(\frac{2}{\pi}\right)\ln\left[\frac{1}{3}+\frac{2}{3}\cosh\left(1+3^{-3/2}\pi+\frac{\pi w}{2t_i}\right)\right]$<br>$+\left(\frac{2}{\pi}\right)\ln\left(\left\lvert\frac{1+\sqrt{1+(t_i+h_m)/t_c}}{1-\sqrt{1+(t_i+h_m)/t_c}}\right\rvert\right)$<br>where $C = 1+(h_m/t_i)$ [16] |
| (Case 3)<br>Infinite number of parallel lines in a confined medium |  | $S' = \left[\frac{1}{2}\ln\left(1+\frac{d}{w}\right)+\frac{\left(\frac{t_i}{w}\right)-\frac{1}{2}\left(\frac{d}{w}\right)}{1+\left(\frac{d}{w}\right)}\right]^{-1}$ [2] |
| (Case 4)<br>Long vertical cylinder in a semi-infinite medium attached to the constant temperature surface |  | $S' = \frac{2\pi}{\ln(4h_v/D)}$ $(h_v \gg D)$ [9] |
| (Case 5)<br>Long vertical cylinder in a semi-infinite medium |  | $S' = \frac{2\pi}{\ln\left[\left(\frac{2h_v}{D}\right)\sqrt{\frac{2t_i+h_v}{2t_i+3h_v}}\right]}$ $(h_v \gg D)$ [18] |

TABLE 1. Shape factors for long parallelepipeds and cylinders embedded in a dielectric medium. The shape factor per unit length of the conductor, $S'$, is defined as $q=Sk_i(T-T_0)=S'Lk_i(T-T_0)$ for parallelepipeds (Case 1-3), and $q=Sk_i(T-T_0)=S'h_vk_i(T-T_0)$ for cylinders (Case 4 and 5) where $k_i$ is the insulator thermal conductivity. Note that case 3 ignores heat dissipation from the top and side surfaces of the conductors.