Investigation of Gate to Contact Spacing Effect on ESD Robustness of Salicided Deep Submicron Single Finger NMOS Transistors

Kwang-Hoon Oh, Charvaka Duvvury*, Kaustav Banerjee, and Robert W. Dutton
Center for Integrated Systems, Stanford University, CA 94305
*Silicon Technology Development, Texas Instruments, Dallas, TX 75243
Phone: 650-723-9484; Fax: 650-725-7731; e-mail: okhoon@gloworm.stanford.edu

ABSTRACT

ESD failure threshold of NMOS transistors is known to degrade with the use of silicided diffusions owing to insufficient *ballast resistance*, making them susceptible to current localization, which leads to early ESD failure. It is commonly believed that the gate-to-contact spacing of silicided devices has no impact on the ESD strength. However, experimental results presented in this paper show that the ESD strength depends on the gate-to-contact spacing independent of the silicided process. This paper also presents results of a detailed investigation of the influence of gate-to-source and gate-to-drain contact spacings for a salicided 0.13 μm technology and provides new insight into the behavior of ESD protection devices. It is shown that the reduction in current localization and increase in the power dissipating volume with increase in the gate-to-contact spacings are root causes of this improvement, which implies that even for silicided processes, the gate-to-contact spacing should be carefully considered for efficient and robust ESD protection designs.

[*Keywords:* gate-to-contact spacing, ballast resistance, power dissipating volume, ESD robustness, and salicided NMOS transistor.]

INTRODUCTION

It is well known that for non-silicided or silicide-blocked NMOS transistors, the second breakdown triggering current (It_2), which is widely used as an ESD strength monitor, can be increased with larger drain contact spacings because of more uniform triggering of the lateral NPN structure, due to ballast resistance effects. In addition, it is also well established that effectiveness is reduced in the case of devices with silicided diffusions [1], since the ballast resistance is negligible. In silicided CMOS processes, the primary cause of the degradation of ESD failure threshold is known to be non-uniform lateral bipolar conduction, which is attributed to insufficient ballasting resistance in the fully silicided source/drain structures [2]. This decrease in ESD strength imposes severe restrictions on the efficient design of ESD protection. Therefore, to avoid localized current conduction and improve It_2, device structures with sufficient ballasting resistance are realized by introducing the silicide blocking option, implementing well resistors on the drain side, or by inserting local interconnect layers [3, 4, 5]. However, these options either require an extra mask or more process complexity and result in increased process cost and chip area. Hence, in this regard, cost effective measures are required for advanced ESD protections.

Unlike conventional understanding, for an advanced deep submicron technology with a shallow trench isolation (STI), the gate-to-drain contact spacing has been observed to have an impact on It_2 even with the silicide present. Moreover, it has been observed that the gate-to-source contact spacing affects It_2. These observations have significant implications for ESD performance improvement simply through optimization of the device layout, even without introducing expensive process options.

However, the impact of the gate-to-contact spacing of a salicided NMOS transistor on the ESD failure strength has not been fully explored. In addition, the physical mechanism causing It_2 improvement with increased gate-to-contact spacing is not clearly understood. This work investigates the above new phenomenon in advanced salicided transistors and describes the different mechanisms that are observed at the source and drain sides, respectively. Furthermore, it is shown that the ESD strength of the protection device becomes independent of the gate-to-contact spacing when adequate substrate bias is applied.

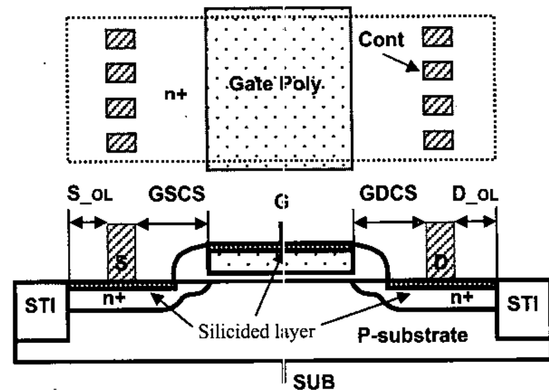


FIGURE 1. The schematic of a silicided NMOS transistor indicating the gate to source/drain contact spacing (GSCS/GDCS) and the n^+ overlap of the source/drain contact (S_{OL}/D_{OL}). For the 1.5V NMOS, the S/D contact opening (S/D) = 0.15μm and $S_{OL} = D_{OL}$ = 0.1μm. For the 3.3V NMOS, the S/D contact opening (S/D) = 0.15μm and $S_{OL} = D_{OL}$ = 0.125μm. In the test structures, the S/D contact opening and n^+ overlap of S/D contact (S_{OL}/D_{OL}) remain unchanged despite the variations of GSCS/GDCS.

EXPERIMENTS

A. It_2 Dependence on Contact Spacing

In this work, the dependence of second breakdown triggering current (It_2) is investigated as a function of the gate-to-source/drain salicided ($CoSi_2$) contact spacing (GSCS/GDCS) for various test structures with grounded gates. Test structures were fabricated using a 0.13 μm technology. Two types of transistors are investigated in this study - low (1.5V) and high (3.3V) voltage NMOS transistors with different gate oxide thickness and drawn channel lengths. The 1.5V NMOS transistor has a 27 Å thick gate oxide and 0.175 μm long gate poly, while the 3.3V NMOS transistor has a 70 Å gate oxide and 0.5 μm long gate poly. However, the finger width for both transistors is 20 μm. Fig. 1 shows the schematic cross section of the ESD NMOS transistor used in this study. The contact spacing is measured from the gate poly edge to the near edge of contact opening and the contact opening width is fixed at 0.15 μm for all the test structures. Since the test structure uses a shallow trench isolation (STI) with constant n^+ overlap with the source and drain contact (S_{OL}/D_{OL}) for a given device rating, the total size of the source and drain structures are

changed proportional to the variation of the GSCS and GDCS. The second breakdown triggering current (It_2) was measured using the transmission line pulsing (TLP) method for a voltage pulse width of 200 ns. As expected, since the resistance of silicided region is relatively small compared to other parasitic resistances in the source/drain structure, a change in resistance proportional to the GDCS/GSCS is not apparent from the DC I-V measurements. The drive current (I_{drive}) of the 1.5V NMOS transistor was tested with GDCS/GSCS variations. As shown in Fig. 2, the measured drive currents show that the difference in the resistance due to increased gate-to-contact spacing with the salicided diffusion is hardly apparent. In addition, Fig.3 shows a sample of TLP curves for the 1.5V transistor with two different GDCS and GSCS. It can be clearly seen that the It_2 value is about doubled with an increase in GDCS/GSCS from 0.1μm to 0.5μm. However, the slope of the high current regions is nearly identical for the two different test structures, which implies that the on-resistance of the test structures is nearly the same despite the different gate-to-contact spacings.

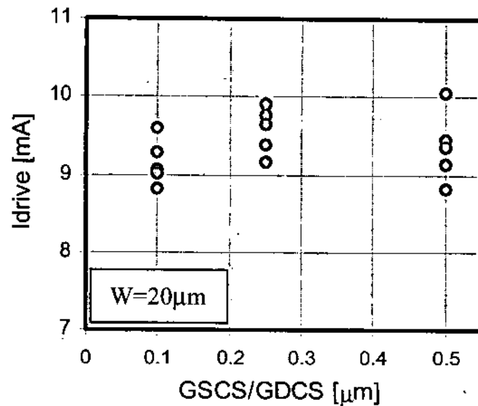


FIGURE 2. The measured drive currents for the 1.5V NMOS transistors with different gate-to-contact spacings show no apparent differences, where $V_{gs}=V_{ds}=1.5V$.

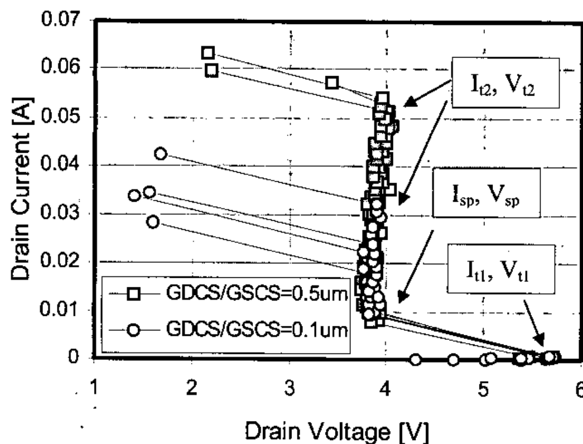


FIGURE 3. High current TLP curves for the 1.5V NMOS transistor with two different GDCS/GSCS (0.1μm and 0.5μm), which clearly show the impact of the gate-to-contact spacings on It_2 despite the silicided diffusion.

For the TLP measurements of the 1.5V and 3.3V transistors as shown in Fig. 4, It_2 of both the devices surprisingly improves with the GSCS/GDCS. Compared with It_2 values of the transistor with the minimum gate-to-contact spacing (0.1μm for 1.5V NMOS and 0.225μm for 3.3V NMOS), the improvement of It_2 ranges from approximately 100 % and 40 % for the low voltage and high voltage transistors, respectively. This implies that the gate-to-contact spacing is an important design parameter determining ESD strength for the gate grounded ESD protection devices. It also suggests the possibility for achieving increased ESD robustness through optimizing the layout of the silicided protection devices without any extra processing steps or structure options. However, the primary cause of this improvement of It_2 has not been explored and needs comprehensive modeling and analysis in order to improve understanding of the device physics involved in this effect. This will also enable the establishment of robust ESD protection design approaches through proper design of the devices.

As shown in Fig. 4, for the 1.5V NMOS transistors, the It_2 dependence on the gate-to-contact spacing is more apparent than that for the 3.3V devices. In general, for advanced devices with salicided diffusion, the improvement of It_2 is not easily achieved due to early failure caused by current localization. In this regard, any amount of improvement in It_2 for salicided technology with no process changes has significant implications. As can be seen in Fig. 5, It_2 values are influenced by both GDCS and GSCS within the scatter of data.

Despite the salicided process, the increasing trend of It_2 is obvious as GDCS and GSCS increase. For the minimum gate-to-contact spacing of 0.1μm, It_2 ranges from 1 to 1.5mA/μm. However, with the increased GDCS=1μm and GSCS=0.5μm, It_2 values are clustered around 3.5mA/μm. The data clearly show that for a given spacing (GDCS), increase in GSCS strongly affects the ESD hardness. This experimental result implies that the impact of gate-to-source contact spacing is as significant as that of the gate-to-drain contact spacing for a salicided technology.

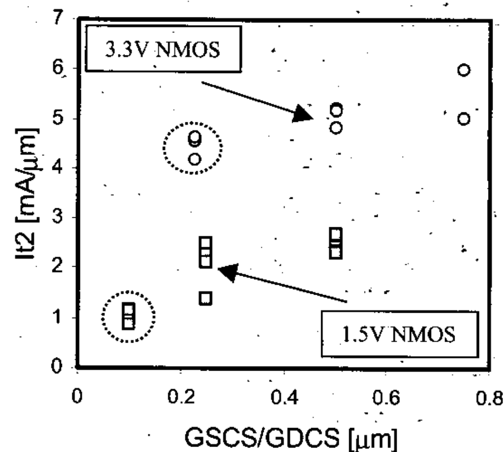


FIGURE 4. The second breakdown triggering current (It_2) with the gate-to-source/drain contact spacing for two different silicided NMOS transistors. The two dashed circles indicate It_2 for each device with minimum contact spacing (0.1μm and 0.225μm for the 1.5V NMOS and 3.3V NMOS, respectively). Squares represent the 1.5V NMOS transistors (W/L_{poly} = 20/0.175 μm), and circles represent the 3.3V NMOS transistors (W/L_{poly} = 20/0.5 μm).

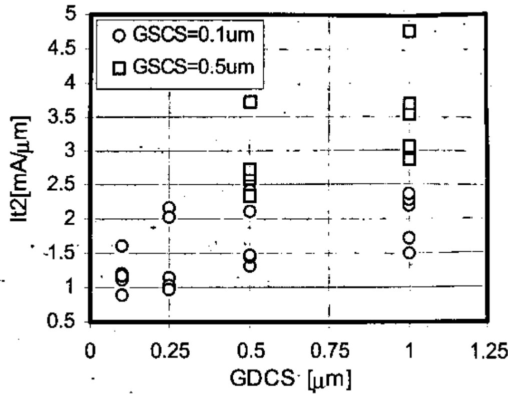


FIGURE 5. It_2 values for the 1.5V NMOS transistors with various GDCS and GSCS. It_2 depends on both GDCS and GSCS within the scatter of data.

B. Effect of Substrate Bias

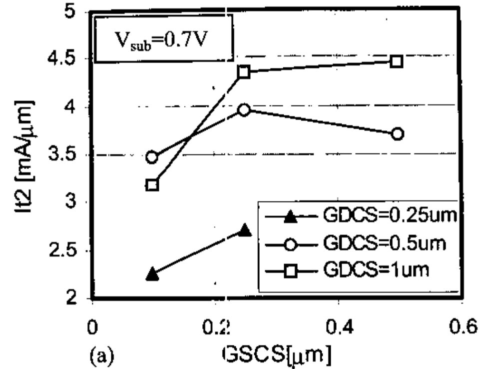
For silicided devices, it has been reported that It_2 improves with a forward substrate bias by enlarging the turn-on finger width of the devices. With sufficient external substrate bias (V_{sub} > 0.7V), the It_2 dependence on the gate-to-contact spacing disappears as the emitter-base junction of the lateral bipolar transistor fully turns on (Fig. 6). This means that the phenomenon of It_2 improvement is associated with the extent of uniformity of the lateral current distribution, since the ESD current becomes more uniform along the channel width with increased external substrate bias [2]. In addition, it should be noted that the It_2 dependence on the gate-to-contact spacing for the 1.5V transistor is stronger, since the extent of uniformity of the lateral current distribution of the two devices varies (see Fig. 8). It is believed that the devices with shorter channel length and shallower junction depth experience non-uniform bipolar conduction more strongly since the relative sensitivity to the statistical random variation is higher for given process conditions. In order to identify the underlying physical mechanisms for the drain side and source side contact spacing effects respectively, the following effects were investigated: 1) the influence of the ballasting ESD current distribution, 2) the improvement of the current driving capability of the lateral NPN transistor and 3) the increase in thermal capacity due to the enlargement of power dissipating volume along with the increase in GSCS/GDCS. Each of these effects has been investigated in detail in the next section.

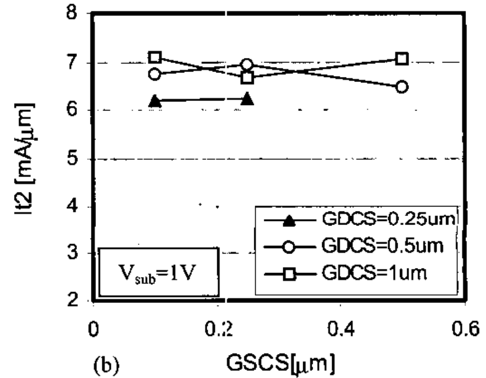
ANALYSIS AND DISCUSSION

A. Ballasting Current Distribution

As shown in Figs 2 and 3, from the DC and TLP measurements for 1.5V NMOS transistors, the drive current and the on-resistance show no differences between the structures with the minimum gate-to-contact spacing and the ones with increased gate-to-contact spacing as expected.

First, to analyze the impact of the GDCS above, for a fixed GSCS of 0.1 μm, It_2 was measured for the structures with GDCS of 0.1μm and 1μm, respectively. As can be observed from Fig. 7, consistent with Fig. 3, even with further increase in GDCS, the on-resistance remains unaffected. However, It_2 is nearly doubled with GDCS=1 μm. Despite these empirical results, it can be conjectured that the increase of GDCS alleviates current localization and further expands the turned on portion of finger width, which appears only for devices with strongly non-uniform ESD current distributions under ESD stress. For devices with various finger widths, total failure threshold currents (IT_2) were measured for the low and high voltage transistors. As can be seen in Fig. 8, the total failure threshold current (IT_2) doesn't scale with the drawn finger width for the 1.5V transistor; only for a limited range of widths does IT_2 scale for the 3.3V transistor. This implies that the ESD current distribution for 1.5V NMOS devices is highly non-uniform while it is nearly uniform for the narrow 3.3V NMOS transistors (W ≤ 20μm).





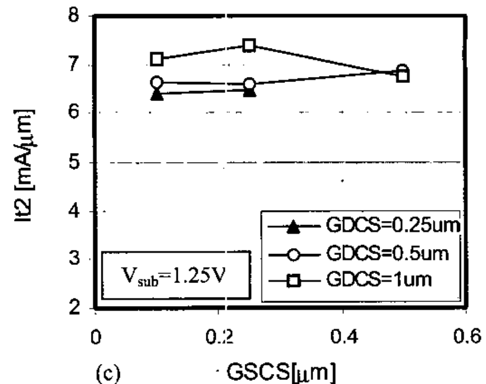


FIGURE 6. (a) It_2 of the 1.5V NMOS transistors is dependent on GSCS and GDCS with an external substrate bias of 0.7V, and is nearly independent of GSCS and GDCS with sufficient external substrate bias of (b) 1V and (c) 1.25V.

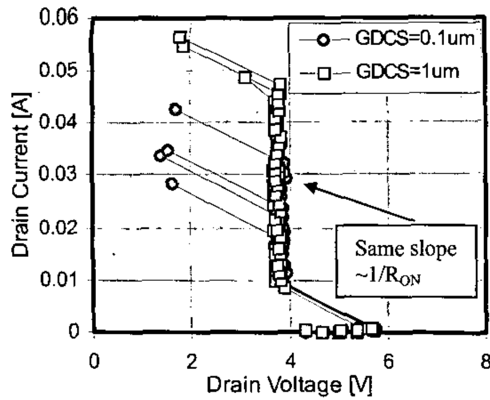
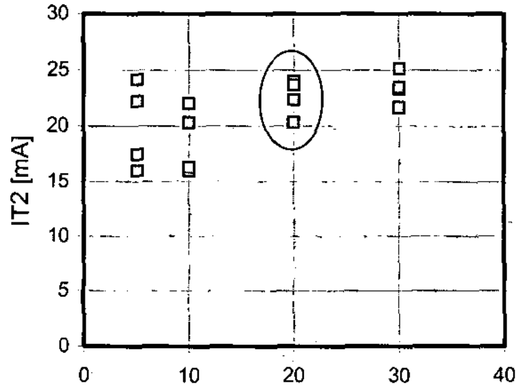


FIGURE 7. High current TLP curves for the 1.5V NMOS transistor with two different GDCS of 0.1μm and 1μm where GSCS is 0.1 μm. The slope of high current regions is almost identical, but the failure threshold current (It_2) is nearly doubled with the increased GDCS.



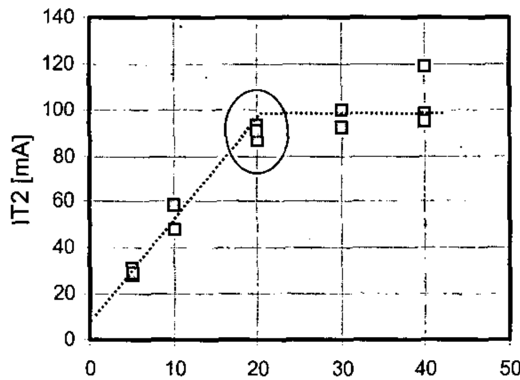


FIGURE 8. Total failure threshold current (IT_2) with the finger width for (a) 1.5V NMOS transistors and (b) 3.3V NMOS transistors where GDCS/GSCS=0.1 μm. The total failure current can be scaled with finger width within only a limited finger width ($W \leq 20$ μm) for the 3.3V devices. The overall data show the strong current localization for the salicided devices under ESD stress.

The data shown in Fig. 9 support the observation that only devices with uniform ESD current distribution don't show dependence on GDCS. Thus, it can be concluded that the increase in GDCS helps spread out the ESD current more uniformly along the finger width, which leads to improvement in the effective value of It_2, though the increase in the ballasting resistance with the GDCS is hardly noticeable. This is apparent from the total failure threshold current (IT_2) data in Fig. 8 (a) for the 1.5V NMOS devices where the ESD current distribution is strongly non-uniform. In addition, for low voltage transistors, with adequate external substrate bias, the dependence of It_2 on GDCS disappears as shown in Fig. 6. This result also supports the argument that the increase in GDCS alleviates current localization for low voltage transistors. In other words, it seems that for the salicided devices, the shorter the gate-to-drain contact spacing is, the stronger the current localization. Therefore for the devices requiring higher ESD strength, minimum gate-to-contact spacing should be avoided unless substrate bias can be used in the protection circuit design [6].

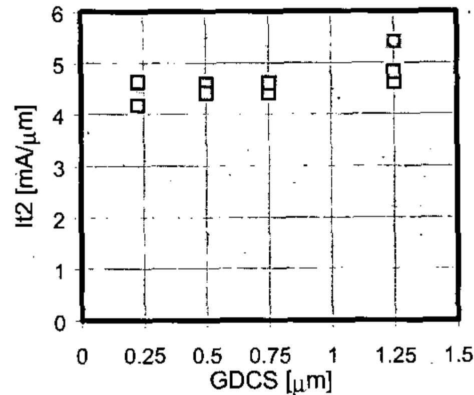


FIGURE 9. It_2 vs. GDCS for the 3.3V NMOS transistors (W=20 μm and L_{poly}=0.5 μm). The 3.3V device with nearly uniform current conduction shows negligible dependence of It_2 on GDCS.

B. Characteristics of the Lateral NPN

In general, the ESD hardness of NMOS devices can be described in terms of the primary device parameters of the parasitic lateral NPN transistors, such as the current gain (β), avalanche multiplication factor (M), and effective substrate resistance (R_{sub}) [7, 8, 9].

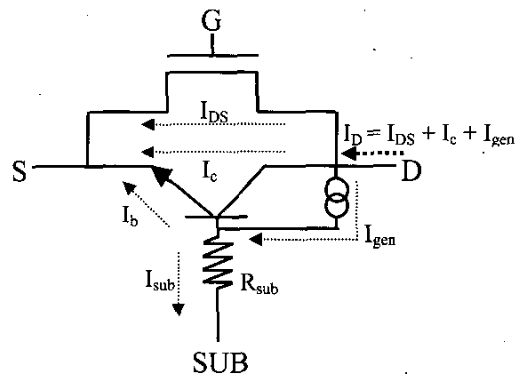


FIGURE 10. Equivalent circuit of the NMOS including the parasitic lateral NPN bipolar transistor when the LNPN is on.

When the lateral NPN turns on (see Fig. 10), the M, β, and R_{sub} are given by [8]

$$M = \frac{(\beta+1)I_D}{\beta(I_D - I_{sub})} \quad (1)$$

$$\beta = \frac{1}{(M-1) - M({I_{sub}}/{I_D})} \quad (2)$$

$$R_{sub} \approx {0.8}/{I_{sub}} \quad (3)$$

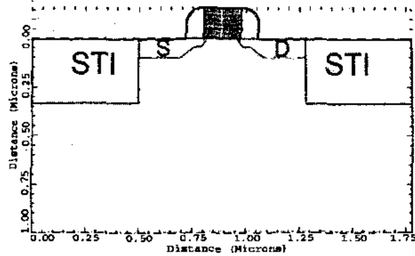


FIGURE 11. The cross sectional view of the simulated structure including the shallow trench isolation (STI) where the silicide layers are treated as virtual electrodes.

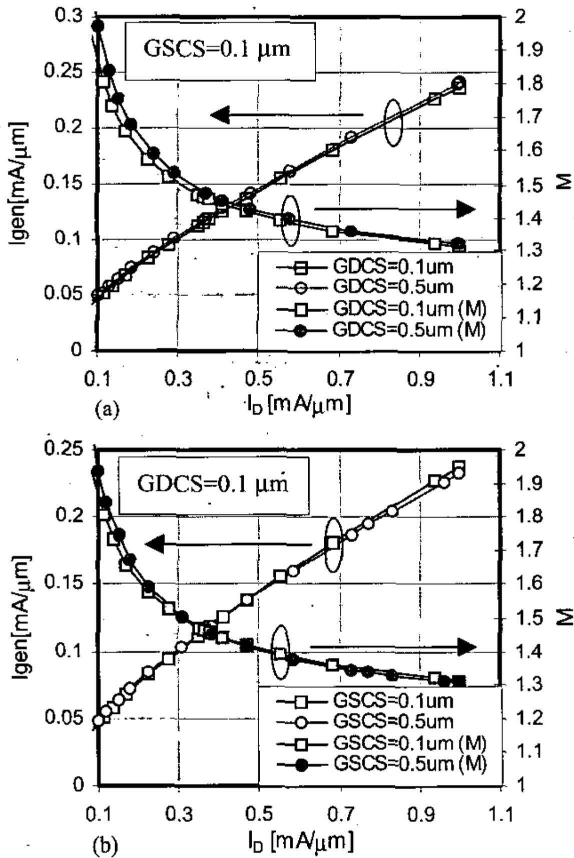


FIGURE 12. The avalanche-generation current (I_{gen}) and multiplication factor (M) for the variation of (a) the GDCS and (b) GSCS.

Despite variation of the GSCS/GDCS, R_{sub} can be assumed to remain constant since the substrate doping concentration and the location of the substrate contact are dominant factors in determining R_{sub}. Therefore, the current gain and avalanche multiplication are of primary interest for studying the impact of variations of gate-to-contact spacing on It_2. The lateral NPN operation depends on a combination of M, β, and R_{sub} for a given power dissipation. For a given ESD current, less avalanche multiplication and higher current gain are preferable for higher ESD strength, since strong avalanche multiplication results from high fields which in turn, leads to locally higher temperatures. The variation of the avalanche multiplication for the test structures can be observed by employing 2D device (*MEDICI*) simulation. Fig. 11 shows the simulation structure including the STI regions. It should be noted that in the test structures used in this study, as the contact spacing is increased, the source or drain area did not remain constant since the STI boundary also simultaneously moved (see Fig. 1). In addition, in the simulations, the silicide layers are treated as virtual electrodes and the effective substrate resistance of 5KΩ/µm is attached to the bottom substrate contact. Furthermore, from the thermal point of view, the size of the simulation structure should be fixed, otherwise the thermal boundary conditions change. Using the DC current sweep simulation mode, high current characteristics were reproduced for the structures with minimum gate-to-contact spacings (GSCS/GDCS=0.1 µm) and also for longer GDCS (=0.5 µm) or GSCS (=0.5 µm).

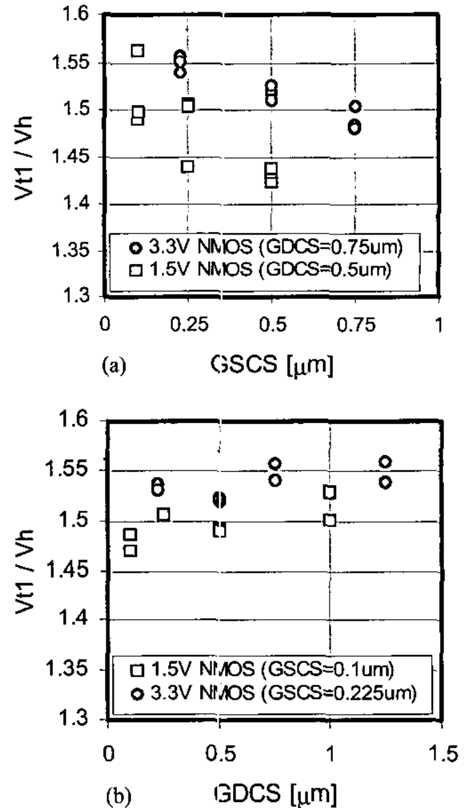


FIGURE 13. To track the current gain of a lateral NPN transistor, the triggering voltage (V_{t1}) and holding voltage (V_h) are measured for the 1.5V and 3.3V NMOS transistors. The data clearly show that the current gain is reduced by increase in GSCS (a), while remains nearly constant with GDCS (b).

As shown in Fig. 12, the avalanche-generated current (I_{gen}) and multiplication factor (M) are compared for the three cases. As the drain current increases, the generation current (I_{gen}) increases while the multiplication factor decreases rapidly, regardless of the gate-to-contact spacing. Based on the simulation results, variations of the gate-to-contact spacing appear to have no impact on the avalanche process. The increase in the current gain of the lateral NPN transistor results in an improvement of It_2 by conducting more current for a given ESD stress. Since the current gain of a lateral NPN transistor (for a gate grounded NMOS) in a self-biasing mode is proportional to the ratio of the triggering voltage (Vt_1) and holding voltage (V_h) [10], to track the current gain of a lateral NPN transistor with the variation of GSCS and GDCS, the Vt_1/V_h is monitored for various test structures as shown in Fig. 13. For a constant GDCS of both the low and high voltage devices, the ratio of Vt_1 and V_h decreases with increase in GSCS. However, compared with the Vt_1/V_h values for GSCS variations, the Vt_1/V_h values are nearly independent of the GDCS. As described earlier, for the test structures, size of the source/drain is increased as the GSCS/GDCS increases. Therefore, the effective area of the emitter (source) of the lateral NPN is enlarged with increases in the GSCS, and in turn, the effective current path is also increased. As shown in Figs. 14 and 15, for a given collector current, with the increased effective size of the emitter, more base current (hole current component) flows into the emitter for a given generation current (see Fig. 14), which results in a slight decrease in the current gain (β) (see Fig. 15). Additional supporting results are shown in Fig. 16. It can be observed that for a constant GDCS of 1μm, the on-resistance, R_{on}, increases with GSCS, which results from a reduction in bipolar current gain as mentioned earlier.

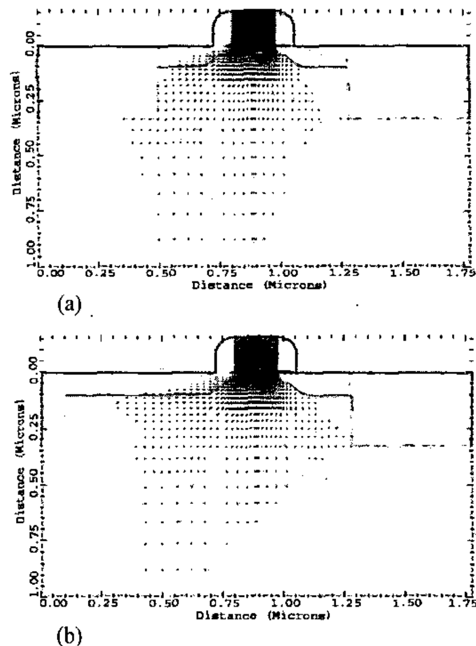
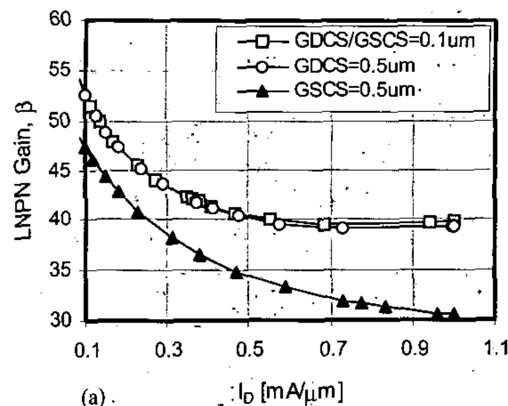


FIGURE 14. The base current (hole current) density vector at I_D=1mA/μm for the device with (a) the minimum gate-to-contact spacing, GSCS/GDCS=0.1 μm and (b) the increased gate-to-source contact spacing, GSCS=0.5 μm. As GSCS increases, wider emitter and base junction is utilized for the current conduction and this results in a drop in the current gain due to the increase in base current for a given collector current.

However, despite the decreased current gain with GSCS, improvement in It_2 is observed with GSCS. Consequently, the increase of It_2 with the GSCS is not attributed to the lateral NPN current gain. These results suggest that the device mechanism for improvement of It_2 with the gate-to-source contact spacing variations is not dependent on the efficiency of lateral parasitic NPN transistor.



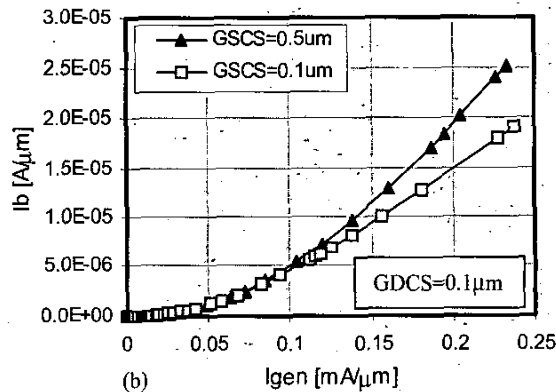


FIGURE 15. (a) The current gain (β) vs. the drain current and (b) the base current vs. the generation current for the device with different gate-to-contact spacings.

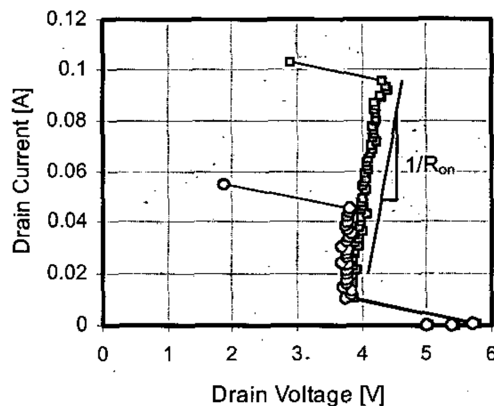


FIGURE 16. TLP curve for the 1.5V NMOS transistor shows increase in R_{on} due to the reduction in current gain with GSCS (circle: GSCS=0.1μm and square: GSCS=0.5μm), where GDCS is 1 μm.

The efficiency of the lateral NPN for conducting ESD current seems to be degraded or unchanged with increases in gate-to-source contact spacing. Therefore the main cause of the improvement in It_2 due to increase in GSCS is still unclear. For better insight into the physical behavior and thermal effects involved in the gate-to-contact spacing, electro-thermal simulations have also been performed.

C. Thermal Effects

In order to investigate any increase in thermal capacity due to enlargement of power dissipating volume along with the increase in GSCS/GDCS, the temperature distributions in the device have been compared. Current flowlines and temperature distribution contours for a drain current of 1mA/μm in the three different structures are shown in Fig. 17. According to the simulation results, the location of the maximum temperature in the device remains the same, despite differences in the maximum temperature value itself. Due to the higher thermal resistance of STI structures and reduced thermal conductivity in upper passivated layers, the heat generated in the device under the ESD stress is confined and mostly dissipated through the substrate. Therefore, changes in the STI boundary associated with variations of GSCS/GDCS influence the overall temperature distribution and the peak temperature in the device as well. In Fig. 18, we show the effect of the gate-to-contact spacings on the temperature distribution. The temperature for the device with longer GSCS (= 0.5 μm) is significantly lower than that of the two other structures with GDCS of 0.1 μm and 0.5 μm.

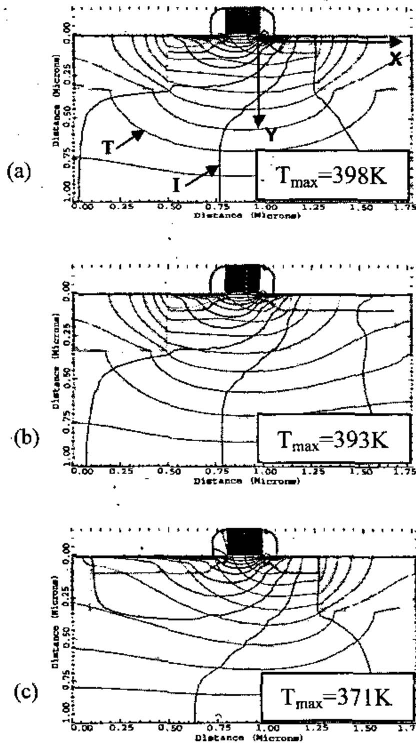


FIGURE 17. The current flowline and temperature distribution contours at the drain current of 1mA/μm for the three different structures are shown. (a) GSCS=0.1μm and GDCS=0.1 μm, (b) GSCS=0.1 μm and GDCS=0.5 μm, and (c) GSCS=0.5 μm and GDCS=0.1 μm

The augmented power dissipating volume for the larger GSCS results in a lower peak temperature for a given drain current. Thus for the device with larger GSCS, a higher ESD failure threshold can be obtained by reducing the peak temperature. Therefore, under ESD conditions, the maximum temperature of the device for a given drain current is higher with commensurate reduction in the effective source size due to smaller GSCS for the devices with STI. The simulated maximum temperature with the drain current is also plotted in Fig. 19. The maximum temperature increases more rapidly with drain current as the power dissipating volume decreases for the shorter gate-to-source contact spacing; a significant difference in the maximum temperature can be expected at higher drain currents.

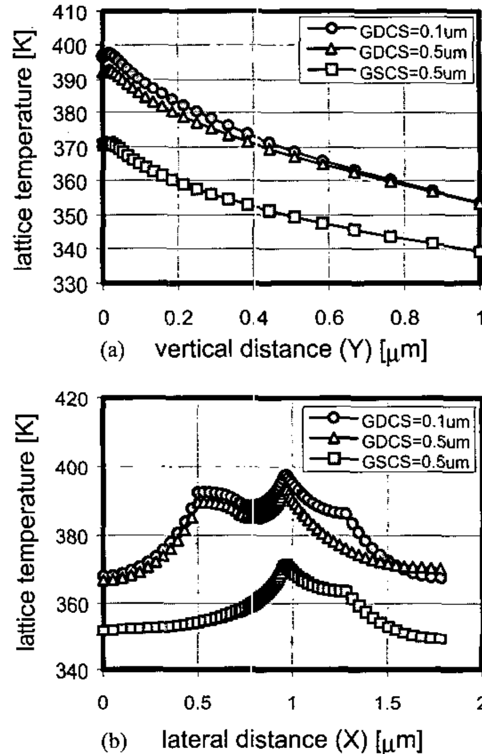


FIGURE 18. The temperature distribution along the x and y direction (as indicated in Fig. 17 (a)) at the drain current of 1mA/μm for the three different structures: (a) lateral temperature distribution and (b) vertical temperature distribution

To provide further support for the thermal effect involved in the gate-to-contact spacing, the total failure threshold currents (IT_2) of the 1.5V test devices having two different power dissipating volumes (arising due to increased n^+ overlap length of S/D contacts) are shown in Fig. 20. Results clearly show the dependence of IT_2 on the size of the power dissipating volume. For the device with $S_{_OL}/D_{_OL}$ of 0.1 μm, the total failure current IT2 is less than 25mA. However, with increase in the power dissipating volume due to the extension of $S_{_OL}/D_{_OL}$, significant improvement in the failure current can be obtained. This experimental result agrees with the predictions based on simulation; both sets of data provide increased confidence that thermal effects are the root causes of It_2 improvement with increase in GSCS. Finally, the overall physical mechanisms involved in the gate-to-contact spacing can be summarized. The increase in the gate-to-drain contact spacing improves It_2 for devices with non-uniform ESD current distributions, primarily the low voltage (1.5V) transistors used in this work.

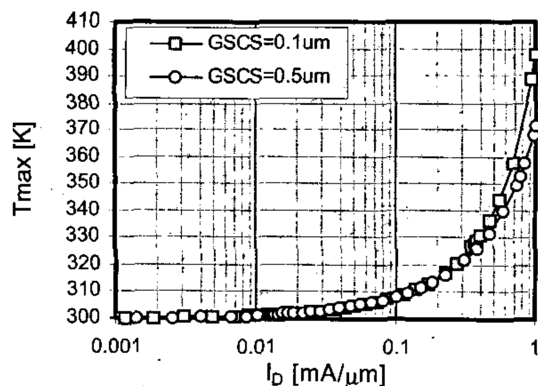
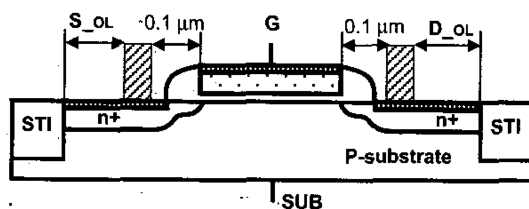
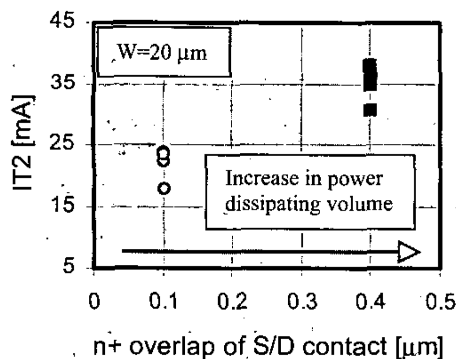


FIGURE 19. The simulated maximum temperature for the two different test structures with injected drain current. The maximum temperature increases more rapidly as the power dissipating volume decreases for the shorter gate-to-source contact spacing.



(a)



(b)

FIGURE 20. Total failure current for the two different test structures having different n^+ overlap lengths of S/D contact of 0.1μm and 0.4μm ($D_{_OL}$ and $S_{_OL}$). (a) The schematic of the test structure and (b) the measured total failure threshold current (IT_2).

Although the changes in ballast resistance cannot be observed directly, increases in GDCS are effective in mitigating severe non-uniform ESD current conduction. Despite reduction in current gain of the lateral NPN transistor, increases in GSCS lead to higher It_2 by increasing the power dissipation volume. This implies that It_2 for salicided deep sub-micron devices with STI is sensitive to the power dissipating volume; the LNPN model is not sufficient for describing the device behavior of these devices under ESD conditions. Therefore, analysis of ESD behavior of advanced devices should consider both thermal effects and non-uniform bipolar conduction. Based on this study, it is recommended that the minimum contact spacing should be avoided for the design of protection devices. However, the minimum contact spacing can be used if sufficient substrate bias is supplied to the device under ESD conditions, because the substrate triggered device is independent of this effect as confirmed experimentally. Further experimental data also show that the results obtained from the single finger structure correlate with the results from multi-finger structures as long as the multi-fingers are uniformly triggered with adequate substrate bias.

CONCLUSIONS

In conclusion, improvement of ESD failure threshold with the gate-to-contact spacing for fully silicided NMOS transistors have been investigated; the results provide new insight into ESD design rules for deep submicron technology, based on detailed experimental and simulation results. It has been shown that the reduction in current localization and increase in the power dissipation volume with increases in the gate-to-contact spacing are the primary factors effecting improvement of ESD performance. It has also been established that substrate biasing can help eliminate the impact of the gate-to-contact spacing; results from this work suggest that even for silicided processes, the gate-to-contact spacing should be carefully considered to achieve efficient and robust ESD protection designs.

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