A Comprehensive Analytical Capacitance Model of a Two Dimensional Nanodot Array

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Abstract

This paper introduces a new comprehensive analytical capacitance model for nanoscale architectures based on nanoscale metallic/semiconducting dots. The model takes into account a detailed charge interaction of the components and shows their implications on power and performance with reference to a nanoscale cellular neural network (CNN) without any loss of generality. Our proposed model, as opposed to a numerical simulator, provides an analytical technique to perform a quick but an accurate estimate of the functional capacitances and thereby evaluate some key performance parameters such as switching delay, power dissipation and energy-delay product of a CNN, or in general a nanodot based circuit. Moreover, this model can be used as a guideline to determine the boundary of transition from continuous charge to discrete charge regimes in nanodot based electronic implementations.

1. Introduction

A lot of next generation nanoelectronic device based circuits, such as logic, memories and image processors are being proposed on the basis of functional novelties achievable by two dimensional nanodot arrays of metallic islands [1-4]. Almost all nanodot-based architectures are predicted on collective computation models, where the cooperative interaction of numerous nanodots, working in unison, elicits useful computational behavior. Therefore, a circuit realization requires a collection of nanodots placed close to each other in a 2-D matrix with other structural complexities, such as substrate layout and inter-dot linkage. A dense arrangement of nanoscale dots necessarily evokes the need of critical analysis of their capacitance by which they are coupled to each other. Accurate estimation of various coupling capacitance has significant bearing in predicting performance of the circuit thus realized out of nanodots. Apart from that, values of these capacitances determine the validity of continuous charge model that is used to illustrate most logic and memory circuits realized with nanodots.

We choose a nanoscale cellular network that can be used to implement Boolean logic to explain the different associative capacitances and model them. The reason we choose this implementation is because of its structural intricacies, which involve various capacitance coupling among its components and hence, require a rigorous treatment. It should be stressed here that applicability of our model is not necessarily limited to only this kind of implementation but can be extended to any paradigm that involves nanoscale dots. The physical treatment used to derive the model enables it to be used for a wide range of dimensions and arrangements of dots and hence, enables us to use it for a cellular network without any loss of generality.

In a Boolean logic implementation by cellular neural network, each computational cell contains nanoscale metallic dots formed into regimented, two-dimensional (2-D) arrays on an active substrate, which possesses a nonlinear, non-monotonic current-voltage characteristic. The substrate can either be consisted of nanometer scale Esaki or resonant tunnel diodes. The computing architecture of the cellular neural network (or CNN) is based on the complex charge interactions between the tunnel diodes and the logic functionality is achieved through charge exchange between the metallic dots [1, 2]. **Fig. 1** is a schematic diagram of how a basic CNN architecture looks like.

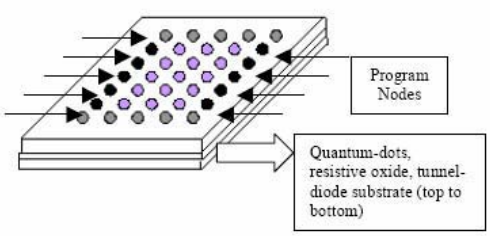

Fig. 1 The basic computational block for our logic scheme can be realized by assembling a 2-D periodic array of nanometer-sized metallic islands (quantum dots) with resistive nearest neighbor interconnections, on a substrate whose current-voltage characteristic has a *nonmonotonic* nonlinearity.

The architecture, ideal for nanoelectronics in many respects, is based on neuromorphic principles and has been shown to have capabilities of functioning as classical Boolean logic, associative memory, image processors and combinatorial optimizers surpassing some of the scaling and power dissipation difficulties of conventional CMOS [2, 3]. Also, within a classical circuit theoretical model (where electric charge is considered a continuous variable) non-linearity of the substrate conduction can yield global associative memory effects and lead to image processing capabilities [1-4]. Interestingly, the interpretation of charge continuity remains valid even when granularity of charge (or single-electron effects) comes into play, provided that the effective capacitance of the islands is not too small. Therefore, an accurate estimation of the capacitance of an island has to be made in analyzing any circuit based on this architecture. The

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first step in formulating the problem of capacitance estimation consists of identifying all components followed by their accurate evaluation. Apart from the self-capacitance of the islands, each island is capacitively coupled to the substrate and to each other. Based on this idea we propose a capacitance modeling of the nanodots, which takes into account the capacitive coupling of all dots in the 2-D matrix as opposed to only nearest neighbor couplings considered in the recent past [5].

Though charging of metal dots with radius of few nanometer is governed by single electronics, the functioning of the present architecture as Boolean logic or memory is based on continuity-of-charge rather than discrete electron-charging phenomenon. The charge continuous model seems to work when a closely packed 2-D array of metal dots is formed. Hence, it follows intuitively that besides the island's coupling capacitance with the substrate and its self-capacitance, the other crucial factor is its interaction with other dots in the matrix. This underscores the necessity of a model for inter-dot capacitance not only to evaluate performance but also to verify the validity of continuous charge model. Accuracy in estimating the inter dot capacitance determines the accuracy in performance evaluation. Unlike other proposed models using nearest neighbor approximation, which is not appropriate as field lines originating from one quantum dot are not really confined

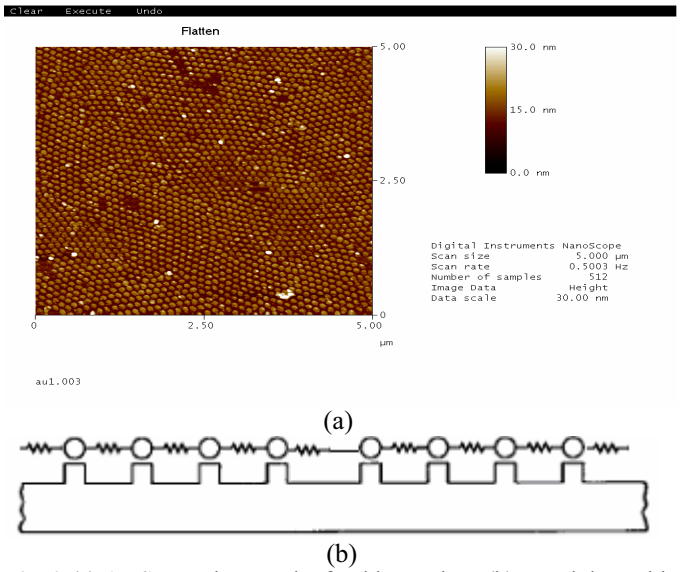

Fig. 2 (a) An STM micrograph of gold nanodots. (b) Metal dots with inter dot resistive link. This resistance, along with the total dot capacitance, determines delay of switching operation.

and can reach out to dots that are much further apart, we estimate the capacitance between dots by considering *all-dot interactions*.

A picture of physically fabricated two-dimensional arrays of gold nanodots is shown in **Fig. 2(a)** [2, 3]. Fig. 2(a) is actually an STM micrograph of self-organized deposition of arrays of nanometer scale metallic islands in patterned core regions, in other words semiconductor mesas, realized by chemical self-assembly followed by etching with metallic islands as "natural" masks. **Fig. 2(b)** shows inter-node resistive link model just to emphasis the existence of an interdot resistance that should be taken into consideration during performance evaluation**.** The basic unit implementation, of the logic scheme, along with operation has been illustrated in **Fig. 3 and Fig. 4** [1]. We use these logic implementations in evaluating switching delay and energy delay product in Section 3.

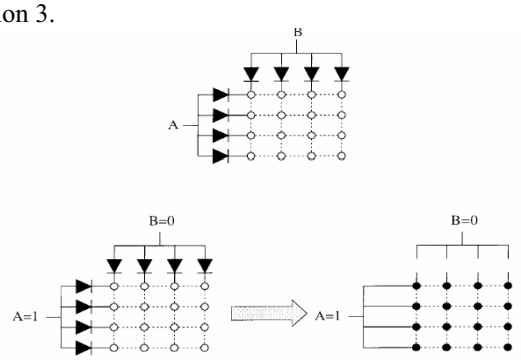

Fig. 3 A schematic description of the realization of a two-input OR gate using arrays of metallic dots deposited on a non-ohmic layer. The metallic dots are interconnected with each other by resistive links and to the inputs by *rectifier* (or *diode*) links. The computation starts by initializing the individual dots to a *low* state, and if any of the inputs is a logical 1, then all the dots will switch to a *high* state.

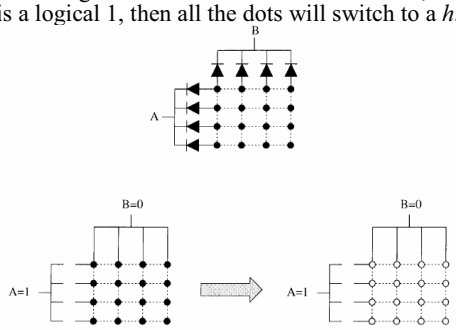

Fig. 4 A schematic description of the realization of a two-input AND gate. Consistent with many current logic implementations, such as programmable logic arrays (PLA's), we can assume that for every binary input, its inverted value is also available as an input. The inversion of the inputs can be done at the boundaries of our computational block using nanoscale single electron transistors. With the input variables and their complements, a two-level OR/AND circuit is universal.

This paper is organized as follows. Section 2 is devoted to discussion of capacitance modeling of the dots and explanation of the analytical equations. Section 3 discusses the effect of capacitance calculated by our model on performance parameters with reference to the Boolean logic shown in Fig. 3 and Fig. 4. Section 4 consists of concluding remarks.

2. Analytical Model of Dot Capacitance Matrix

We define C_{sub} as the capacitance associated with the substrate, C_{link} as the full-capacitance matrix of 2-D dot array and C_{island} as the self-capacitance of the metallic island.

Island-substrate coupling capacitance:

C_{sub} is estimated by modeling the spherical-to-conducting-plane (where the conducting plane is a tunnel diode substrate) capacitance of the nanodot:

$$C_{sub}=2\pi\varepsilon\sqrt{(d^2-4a^2)}\sum_{j=0}^{\infty}(\coth[(j+\frac{1}{2})\operatorname{arcosh}(d/2a)]-1) \qquad (1)$$

where a is the dot radius, d is the distance of the center of the dot from the plane and ε being the dielectric constant of the resistive oxide between dots and the plane.

Inter-dot capacitance:

C_{link} is computed using all-dot interaction consideration, which makes our model more precise than the ones use only nearest neighbor approximation.

To calculate the capacitance of an arbitrary arrangement of non-intersecting conducting spheres with different diameters we start with a charge on the sphere for which the total capacitance is to be obtained. Then compensation charges are placed in all other spheres, so that these spheres stay zero equipotential surfaces. In case an infinite conducting plane is present, all charges so far calculated have to be mirrored on this plane to make it a zero equipotential [6]. But every placed compensation charge will disturb the before compensated potentials. Hence, the compensation charges have to be recursively compensated themselves. For more than two conductors the number of

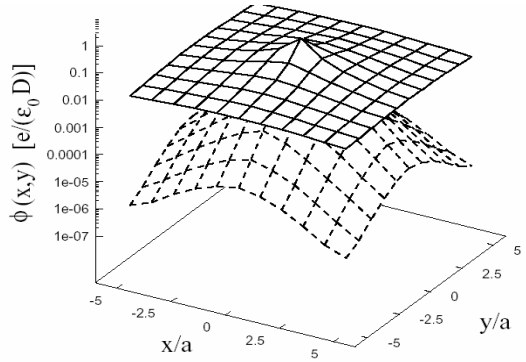

Fig. 5 Potential distribution for full-capacitance matrix (solid-line) and for nearest-neighbor approximation (dashed-line).

compensation charges grows exponentially for every level of recursion. For N spheres the number of charges progress as:

$1 \longrightarrow (N\text{-}1) \longrightarrow (N\text{-}1)^2 \longrightarrow (N\text{-}1)^3 \ldots$.

In order to assure convergence of the successive approximation the magnitudes of compensation charges have to decrease sufficiently. For a large number of spheres, even if the sum of image charges stays bounded, the method can fail due to exponential growth of image charges. The problem can be avoided by placing two charges with a sum of zero in each sphere. One charge is the usual image charge and the other one is positioned at the center of the sphere with the same magnitude but opposite sign thereby forming a dipole. Thus, for one sphere two charges are created, and this does not alter the fact that the sphere surface is an equipotential surface. Only the absolute potential of the sphere is changed. The advantage of using dipoles instead of single charge is that potential of dipoles ($1/x^2$) decay faster compared to that of single charge ($1/x$) hence making the algorithm converge faster [6].

We base our modeling as follows:

$$\varphi_{ij} = \tfrac{1}{2}(\sum_{i=1}^{N}\sum_{j=1}^{N} P_{ij}q_iq_j) + \varphi_f \qquad (2)$$

where P_{ij} is the inverse of the capacitance matrix, φ_{ij} is electrostatic energy and φ_f is the Fermi energy that accounts for electron-electron interaction in sufficiently small islands, and is given by:

$\varphi_f = (kT)\operatorname{arcsinh}\{(n-p)/2n_i\}$ for semiconductors, and

$\varphi_f = \frac{\hbar^2}{2m^*}\left(3\pi^2 n_m\right)^{2/3}$ for metals, where n_m is the concentration of free electrons in metal and other symbols having usual meaning. [Note: For islands of bigger size

$\varphi_{ij} = \tfrac{1}{2}(\sum_{i=1}^{N}\sum_{j=1}^{N} P_{ij}q_iq_j)$ only is sufficient to describe the electron interaction model.]

$P_{ij} = C_{ij}^{-1}$, where

$$C_{ij}=\pi\varepsilon\sum_{i=1}^{N}\{\sqrt{(b_i^2-4a^2)}\sum_{j=0}^{\infty}(\coth[(j+\tfrac{1}{2})\operatorname{arcosh}(b_i/2a)]-1)\} \quad (3)$$

where b_i is the distance of the ith dot from the center of the dot under consideration and a is dot radius. There is an underlying assumption in this equation that the dot radii are constant. The validity of the assumption will be apparent as we show in section III that the effective capacitance is somewhat insensitive to small variations that may be present.

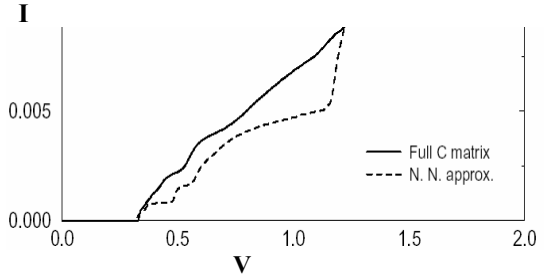

Fig. 6 The differences in current-voltage characteristics of the same array of nanodots as in Fig. 5, the full capacitance matrix (solid line) and the nearest neighbor approximation (dashed line). V and I are in arbitrary units.

Finally, we can write $[\varphi] = [P]\,[q]$, where $[P]$ is the inverse matrix of C_{link}. Our idea is reinforced by FASTCAP simulations showing differences in potential (**Fig. 5**) and I-V characteristics (**Fig. 6**), for an array of quantum dots, computed by nearest-neighbor approximation [7, 8] and full-capacitance matrix. **Fig. 7** shows how our model compares with simulation data for 1-D array of quantum dots of size 2nm and having an average separation of 1 nm.

Calculation of self-capacitance:

Even if the islands are spherical, mere calculation of capacitance for a sphere in classical limits will not yield the correct result for self-capacitance. For very small dot sizes the

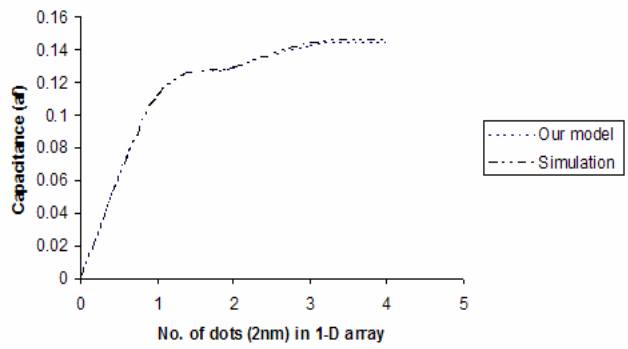

Fig. 7 Capacitance of a no. of quantum dots of size 2nm diameter arranged in a 1-D array with 1 nm separation calculated with our model and compared with FASTCAP simulation.

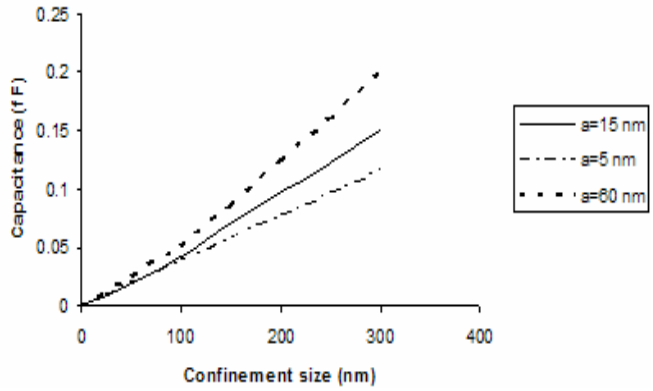

Fig. 8 Self-Capacitance vs dot radius for a quantum dot.

size of an island is not determined by the physical radius but by its potential confinement in which the electrons are bound. Moreover, the self-capacitance of such a dot fluctuates due to various reasons *e.g.* form of wave function (quantization) [9]. Since, any addition or removal of charge from the dot increases or decreases the chemical potential of the dot, it is natural to associate a differential capacitance with the dots and hence, C_{island} can be computed straight from the electro-chemical potential [9, 10]:

$$C_{island} = q^2/\{\mu(N+1)-\mu(N)\} \quad (4)$$

$\mu(N)$ is calculated by Slater's transition rule yielding:
$\mu(N) = E(N) - E(N-1) = E(N-0.5)$. $E(N)$ is estimated from a model quantum dot with a quasi-parabolic confining potential. The exchange and correlation energies are also considered in the model.
$E(N)$ is given by:

$$E(N) = \sum_{i=1}^{N} \varepsilon_i - \frac{1}{2} \iint \frac{q2}{4\pi\varepsilon_o\varepsilon_r} \frac{n(\mathbf{r})n(\boldsymbol{\rho})}{|\mathbf{r}-\boldsymbol{\rho}|} d\mathbf{r}d\boldsymbol{\rho} + \int n(\mathbf{r})\{E_{ex}[n(\mathbf{r})] + E_{corr}[n(\mathbf{r})] - V_{ex}[n(\mathbf{r})] - V_{corr}[n(\mathbf{r})]\}d\mathbf{r}$$

ε_i are the energy eigenvalues for each electron, E_{ex}, E_{corr}, V_{ex}, V_{corr} are the exchange and correlation energies and potentials, respectively and other terms have usual meaning. E_{ex}, E_{corr}, V_{ex} and V_{corr} can be derived from polynomial expression of Tanatar and Ceperley energy for two dimensional electron gas [11]. Appropriate modification (Hartree approximation [11]) should be made in calculating the exchange and correlation energies in presence of other strong electric fields such as any nearby biasing electrode. **Fig. 8** shows how the self-capacitance changes with confinement sizes for different diameter dots. This implies that in order to obtain a fixed capacitance with a larger number of electrons *i.e.* larger confinement, a smaller dot size would suffice. A dot of about 50 nm size associates 20aF approximately. In **Fig. 9** we report the variation of capacitance with the number of electrons in a potential confinement. An increase in number of electrons in a potential confinement should increase capacitance but we observe "dips" due the fact that self-capacitance is calculated from difference of chemical potential [refer to equation (4)] that varies with addition of electrons. The variation in capacitance results not only from coulomb interaction but also from increased quantum energy, which results in a "dip" each time an electron goes to fill an energy level created due to an increase in confinement size [12]. With decrease in dot size the dips get more pronounced as can be seen from **Fig. 10**, which is basically, enlarged section from Fig. 9 for small number of electrons.

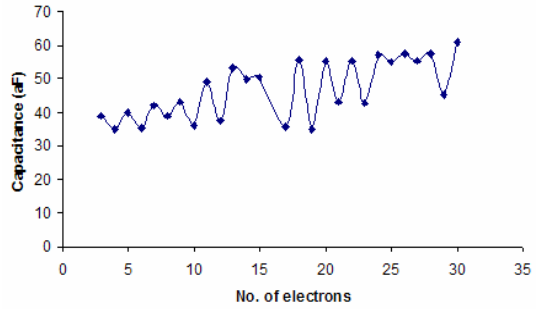

Fig. 9 Self-capacitance vs. no. of electrons for a quasi-parabolic confinement for a dot having radius about 50 nm.

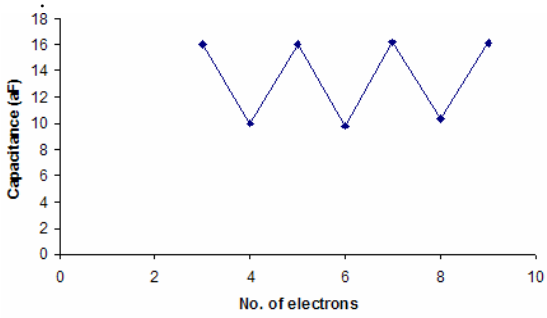

Fig. 10 Self-capacitance vs. no. of electrons in a smaller dot for a quasi-parabolic confinement.

3. Estimated Figures of Merit of the Cellular Architecture

Variation of capacitance coupling of the metallic island with the substrate is shown as a function of dot-radius in **Fig. 11.** It can be seen that the capacitance increases as the

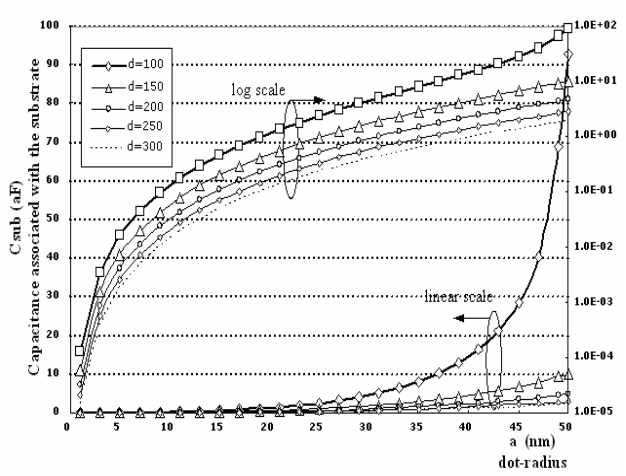

Fig. 11 Capacitance of metallic island with the conducting substrate.

distance'd' of the island from the substrate decreases. **Fig.12** shows the variation of C_{link} with dot diameter and inter-dot distance.

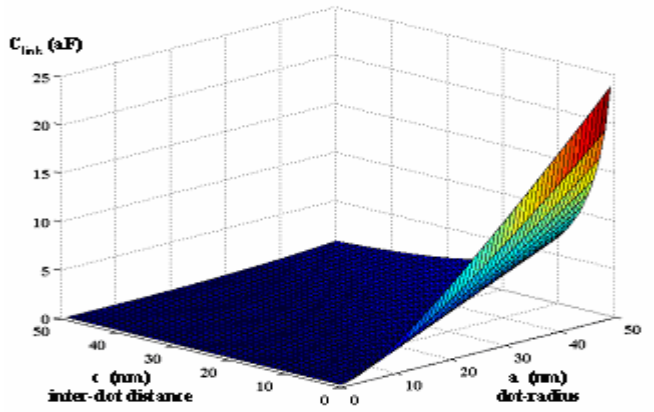

Fig. 12 Inter-dot capacitance variation with dot-radius and inter-dot distance.

Note that 'c' in the figure is the surface-to-surface separation between two dots along the line connecting their diameter. As the dot radius is increased, the increment in capacitance can be seen as also with decrease in spatial separation between the dots. At very low dot radius and large dot separation, almost negligible capacitance coupling is observed and therefore, nearest neighbor approximation can be applied in that regime. But with larger diameter and smaller separation, *all-dot interaction* model proposed in this paper is more relevant. **Fig. 13** shows a cumulative variation of C_{sub} and C_{link} with respect to dot-diameter with constant inter-dot spacing of about 120nm but variable distance from substrate. **Fig. 14** stresses the need for our all-dot interaction model as opposed to nearest neighbor consideration, for accurate estimation of capacitance, which will affect the further performance evaluation of the circuit. The values of capacitances we get from Fig. 8, Fig. 11 and Fig. 12 for 50 nm dots indicates the validity of the assumption of continuous charge model for the operation of cellular neural network.

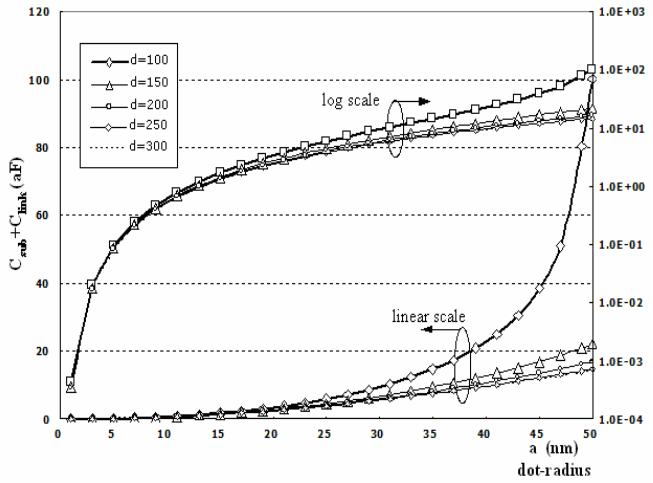

Fig. 13 Summation of inter-dot capacitance and capacitance with substrate for a constant inter-dot spacing of about 120nm.

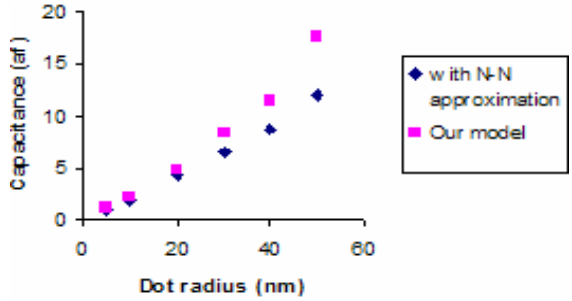

Fig. 14 A comparison of inter-dot capacitance calculated by N-N approximation and our model.

The switching delay for the Boolean circuit described in Fig. 3 and Fig. 4 can be written as:

$$\tau_{delay} = R_{link}\,(C_{sub} + C_{island} + C_{link}).$$

For dot diameters of the order of 50 nm, equations (1) to (4) yield, each of C_{sub}, C_{island}, C_{link} to the order of ~20aF approximately and taking R_{link} to be 100 kΩ (*Note:* Minimum R_{link} is fundamentally limited by: $R_{link} > h/e^2 = 25.8$ kΩ, where h is Planck's constant), we deduce $\tau_{delay} \sim$ 6ps. Time-delay with dot radius is compared in **Fig. 15** and the difference due to error in capacitance calculations by two different methods, is evident. The consideration of the full capacitance matrix projects more delay than is proposed by nearest neighbor approximation, which, therefore, gives over optimistic performance. The static power dissipation can be estimated from the static current and voltage states: $P_{static}=I_{static}V$. For a cell containing 5 nm diameter islands, the static power dissipated in the high voltage state is approximately 0.1 nW per island, while the static power in the low voltage state is approximately zero, as static current is negligibly small. This calculation assumes a peak current density of 10^4 A/cm^2, a peak to valley current ratio of 10:1 and a valley voltage of 0.5 V, all consistent with tunnel diode performance as reported in [2]. A computational cell containing hundred (100) islands

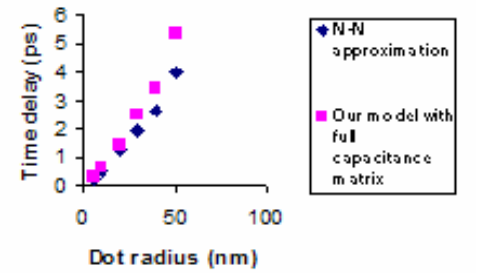

Fig. 15 Comparison of time-delay calculated by two methods, *Rlink = 100kΩ.*

would therefore dissipate 10 nW and would occupy about 10^{-2} cm^2. Therefore, the static power dissipation is estimated to be 25 W/cm^2 for a computational circuit with 10^{10} islands per cm^2 [a comparison is provided with CMOS based on ITRS projection [13] (**Fig. 16**) showing 600nW per computational cell with a cell density of $5x10^7$cells/cm^2, corresponding to 30 W/cm^2]. An upper limit for dynamic energy dissipation in single operation can be estimated as:
$E_{dynamic} = E_{H-L}+E_{L-H} \sim C_{island}V^2$, which is the total energy required for charging of an island, where V is power supply voltage. For C_{island} ~20aF and V=1 volt, the energy-delay product becomes $2x10^{-18}$ J-sec, and the dynamic power dissipated is about ~500 nW per island for bigger dot sizes.

Figures of merit	CMOS (65 nm)	CNN
Dissipation per computational cell	600 nanowatt	1-10 nanowatt
Cell density	5 x $10^7/cm^2$ (DRAM)	~ $10^8/cm^2$ (Logic)
Switching delay	Sub-ps	Sub-ps

Fig. 16 A comparison with ITRS' projected data for CMOS.

For CNN architectures with nanodots of radii about 20 nm single electron charging will not be observed during the room-temperature operation as the capacitance value is not commensurate for manifestation of single-electron effect. However, at very low values of C_{sub}, C_{island} and C_{link}, a little Coulomb blockade effect may become apparent [2]. For instance, for dot sizes less than 10 nm, capacitance values of 1aF are justified on the basis of our previous analysis, where signs of single electron charging starts showing up. Thus, to determine the accurate regime of onset of charge granularity, precise capacitance calculation methodology, as described above, is required.

Fig. 17 shows the variation of capacitance with random variation of dot-radius. It can be inferred that the effect of random size variation is not critical for an arbitrary arrangement of nanodots and this is a desirable property of nanoscale devices from the fault-tolerance point of view.

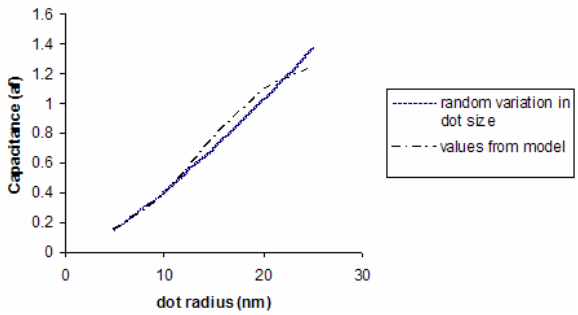

Fig. 17 Comparison shown for inter-dot capacitance of a 1-D array of dots with a dot separation of 5 nm from surface of one dot to another.

4. Conclusion

For the first time, a comprehensive analytical capacitance modeling of nanoscale cellular network components is presented for quick calculation of circuit performance with very high accuracy. This capacitance modeling, which is easily solvable by simple mathematical tools, not only produces a quick and accurate analysis but also can be used as a basis to decide about the regime of charge-continuity model or discrete/single electronics at nanoscale metallic/semiconducting dot structures. Overall this model is certainly an improvement over nearest neighbor approximation in terms of better understanding and evaluation of performance parameters. As this model is based on charge interaction between coupled components, its application is not limited to only neuromorphic architectures. The physical basis of the model is independent of the nature of circuit implementation and hence, with appropriate modifications, can be extended to study similar nano-structures and circuits.

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