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The dependence of W-plug via EM performance on via size

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Abstract. The electromigration (EM) performance of W-plug vias of different sizes, different capping layer types and electron flow directions in a multilevel metallization system was investigated. When the electron flow direction was from metal 2 to metal 1, with a TiN-capped metallization system, the time-to-failure dispersion (sigma) was greatly influenced by via size. However, when the electron flow direction was from metal 1 to metal 2, there was little dependence on via size. Similarly, the via EM performance of a metallization system with titanium as a part of the capping layer exhibited no dependence on via size.

1. Introduction

The electromigration (EM) phenomenon in VLSI multilevel interconnection systems is a reliability issue because of the increase in current density due to the ever-shrinking VLSI circuitry. The EM lifetime of multilevel metallization systems with W-plug vias has been reported to be much shorter than that of a single-level Al stripe [1] even after titanium layering was introduced to improve via EM performance [2]. Researchers have proposed different via failure mechanisms such as an atomic flux divergence due to material discontinuity, damages caused by via etch, current crowding, local depletion of dopants at the W/Al interface, etc [3–6]. Microstructurally, the position of Al grain boundaries relative to the via could have an impact on via EM performance [7]. All of these failure mechanisms are assumed to occur at the W-plug/Al interface which is believed to be the weakest link in a multilevel interconnect structure.

Recently, work conducted by several researchers suggests that time-to-failure (TF) of W-plug via depends on the current density in the servicing metal leads and not on the current density in the via [1, 8]. These claims would imply that via size may not be critically important. Nevertheless, they did not specify how different via sizes affected the time-to-failure dispersion and the range of via sizes for which their observations are valid; for example, as the via size shrinks to zero, their results would seem to become invalid due to excessive Joule heating.

In this paper, the EM results are reported from a series of experiments under various stressing conditions in order to understand how via size, electron flow direction and Ti layering affect via-induced EM failure. Different failure modes are discussed and scanning electron microscopy (SEM) results for failing vias are shown.

2. Experiment

2.1. Sample preparation

Via 1 structures (interconnection between metal 1 and metal 2) in a quadruple level metallization (QLM) system were used as the test structures in this study. Both metal 1 and metal 2 leads had the same structure, Ti/TiN/AlCu(0.5%)/TiN, referred to as a barrier/Al-alloy/cap stack. In one case, a thin Ti layer was deposited between the aluminium alloy and the TiN cap, and the vias were intentionally fabricated with high aspect ratio to produce a possible worst-case scenario. The via plugs were fabricated by dry via etching, *in situ* sputter deposition of a Ti/TiN liner, chemical vapour deposited tungsten (CVD-W) and etch back. The via etching tended to stop inside the aluminium alloy or on the TiN capping layer as shown in figures 1 and 2. The interlevel dielectric consisted of a 11 000 Å plasma enhanced tetraethyl orthosilicate/sub-atmospheric chemical vapour deposition O3 TEOS/spin-on glass/plasma enhanced tetraethyl orthosilicate (PETEOS/SACVD/SOG/PETEOS) stack. The passivation layer was a combination of tensile oxide and compressive nitride.

The EM test structure was chosen to be the 0.5 μm and 0.6 μm single Van der Pauw W-plug vias serviced by 3 μm wide and 270 μm long metal leads so as to avoid the short-length EM effect (or back-flow effect). The width of the metal lead (3 μm) was about two Al grains wide, yielding a worst-case estimate for EM lifetime. The

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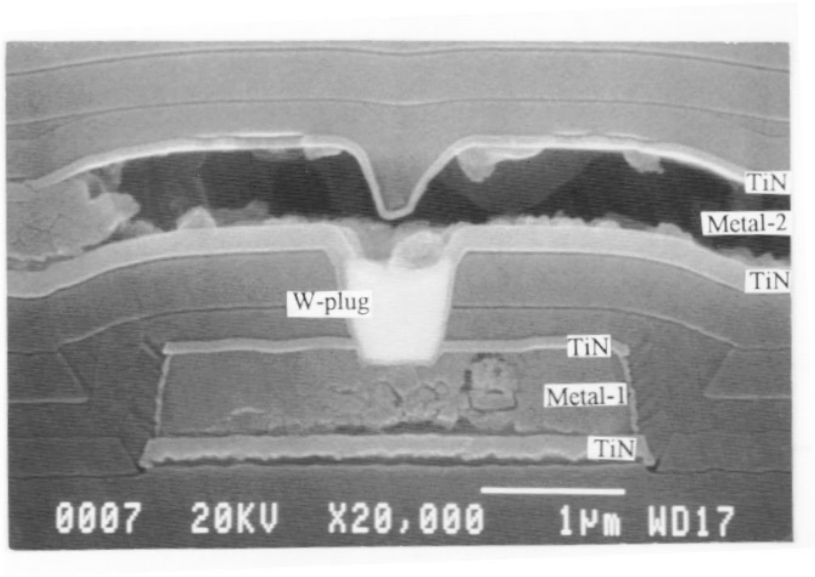

Figure 1. Via etch stopped inside the metal 1 aluminium alloy.

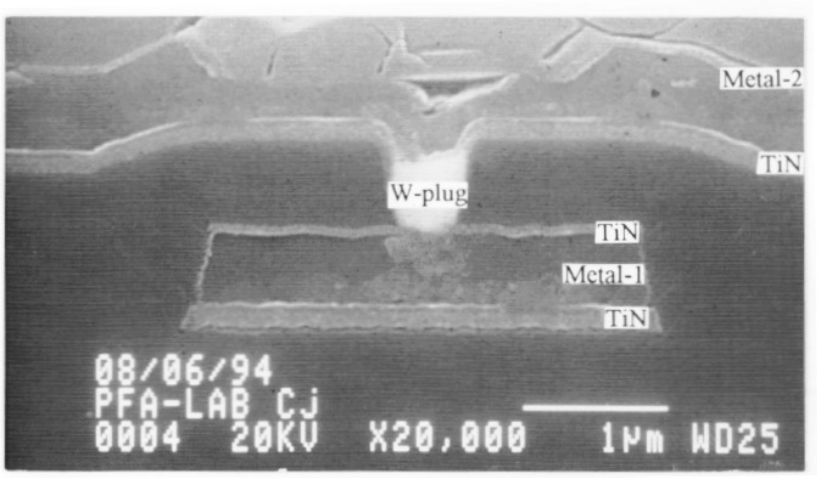

Figure 2. Via etch stopped on the metal 1 TiN cap.

via structures were individually packaged in ceramic units, mounted with four aluminium wedge wire bonds, and put under constant current and elevated temperature. The room-temperature time-zero resistance of the 0.5 μm and 0.6 μm vias was measured by Kelvin contact to be 0.9 Ω and 0.6 Ω respectively. Via-plus-lead resistance was measured to be approximately 13.0 Ω at room temperature.

2.2. EM testing

In the Ti/TiN/AlCu/TiN (barrier/Al alloy/cap) stack metallization both electron flow (e-flow) directions, e-flow from metal 1 to metal 2 and e-flow from metal 2 to metal 1, were tested at a constant current and elevated temperature. The via structures were also tested at different stressing currents to verify the reproducibility of the EM performance. In the Ti/TiN/AlCu/Ti/TiN (Ti as a part of capping layer) stack metallization, only e-flow from metal 2 to metal 1 was tested since the effect of $TiAl_3$ formation on EM performance was the main focus of study. The existence of the $TiAl_3$ layer has been discussed elsewhere [2].

During the EM tests, the Van der Pauw (VDP) structures were stressed at a constant current supplied by two terminals, leaving the other two unstressed. The time-to-failure was recorded after a 20% rise in the via-plus-lead resistance. In order to gather the lognormal statistics, at least 25 samples per stress condition were used. The testing conditions for all experiments are summarized in table 1.

3. Results and observations

Assuming a lognormal distribution, which is normally done for EM failures, it is well known that the time-to-failure

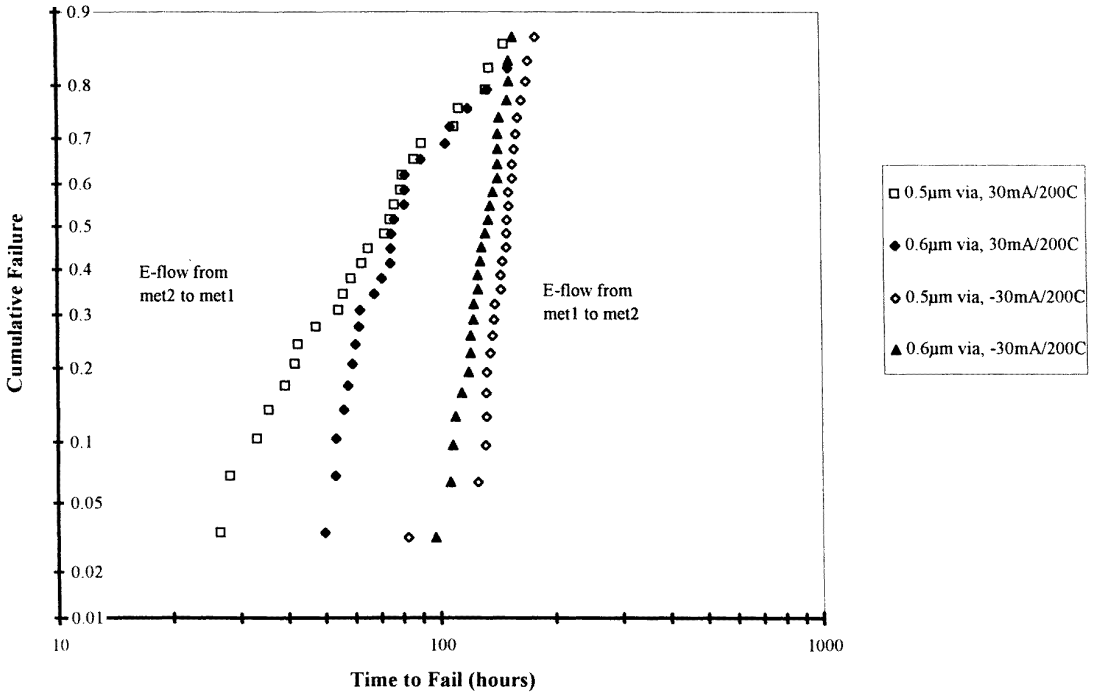

Figure 3. TF distributions of 0.5 μm and 0.6 μm vias with a TiN cap. The e-flow direction is indicated.

Table 1. EM stressing conditions.

Barrier/Al-alloy/Cap	e-flow direction	Current (mA)	Ambient (°C)
Ti/TiN/AlCu/TiN	metal 2 to metal 1	30	200
Ti/TiN/AlCu/TiN	metal 2 to metal 1	25	200
Ti/TiN/AlCu/TiN	metal 2 to metal 1	20	200
Ti/TiN/AlCu/TiN	metal 1 to metal 2	30	200
Ti/TiN/AlCu/Ti/TiN	metal 2 to metal 1	30	200

(TF) during use conditions (relatively lower temperature and current density) can be determined from the lifetime at stress conditions (relatively higher temperature and current density) by the equation [9]

$$\mathrm{TF}(f_{\%})_{\mathrm{use}} = \frac{\mathrm{AF} \times \mathrm{T50}}{\exp(Z(f_{\%})\sigma)} \tag{1}$$

where $(f_{\%})_{\mathrm{use}}$ represents the percentage of cumulative failure under use conditions, T50 is the median time-to-failure under stress conditions, σ is the time-to-failure dispersion = ln(T50/T16); and the Z factors are determined from the standard normal distribution tables where $Z(16\%) = 1.00$, $Z(1\%) = 2.33$, $Z(0.13\%) = 3.00$.

The acceleration factor AF during EM testing is determined from Black's equation

$$\mathrm{AF} = \left(\frac{J_1}{J_2}\right)^{-N} \exp\left[\frac{Q}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right] \tag{2}$$

where N determines the dependence on the current density J (N is normally assumed to be equal to 2), Q is the activation energy and K_B is the Boltzmann's constant.

Equation (1) indicates that although the median time-to-failure (T50) for two distributions may be approximately equal, EM lifetimes for a lower cumulative percentage can be quite different if the sigmas are different.

Figure 3 shows a lognormal plot of the time-to-failure (TF) distribution for the 0.5 μm and 0.6 μm vias with a TiN cap. For the metal 2 to metal 1 e-flow direction, the TF distributions of the 0.5 μm and 0.6 μm vias tended to be quite different in the early fail region. The difference was consistently observed at different stressing currents (figure 4). Although the median time-to-failure (T50) appeared to be approximately equal for the 0.5 μm and 0.6 μm vias, the 0.5 μm via sigma ($\sigma = 0.63$) was higher than that for 0.6 μm vias ($\sigma = 0.43$).

For the metal 1 to metal 2 e-flow direction (figure 3), TF distributions were nearly identical for the two via sizes. Similarly, for the vias with Ti as a part of the capping layer, the 0.5 μm and 0.6 μm via TF distributions coincided (figure 5). Sigmas obtained from lognormal plots in these two cases were low ($\sigma = 0.1$).

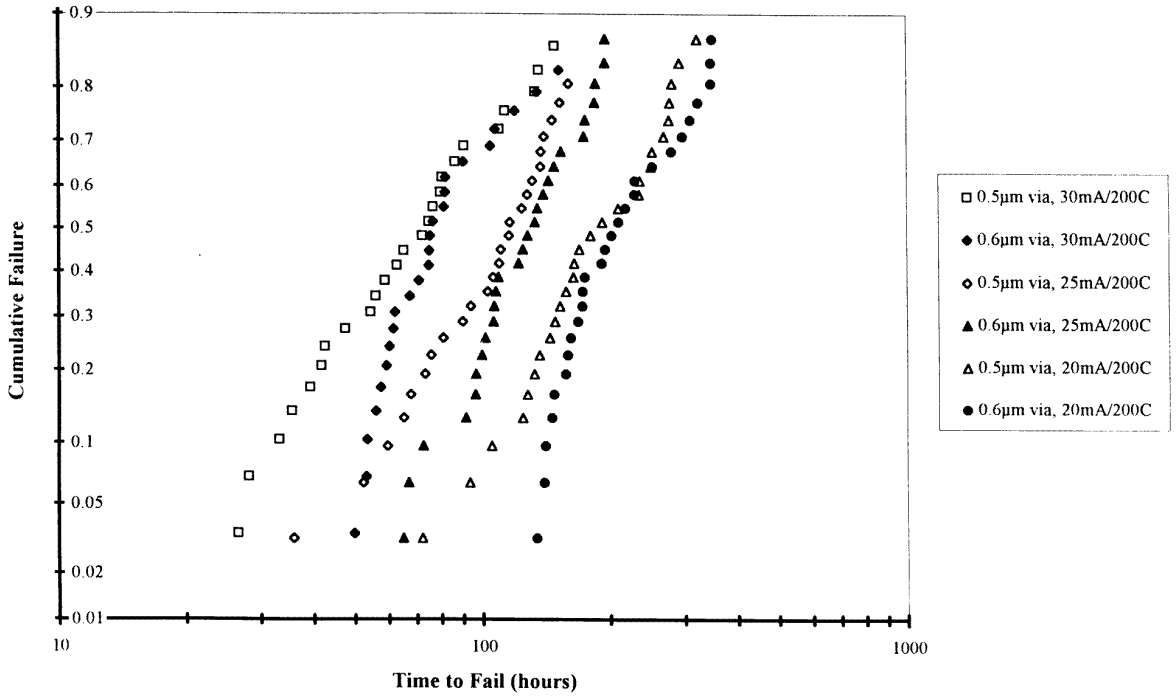

Figure 4. TF distribution of 0.5 μm and 0.6 μm vias in a TiN cap system stressed at different currents. The e-flow direction was from metal 2 to metal 1.

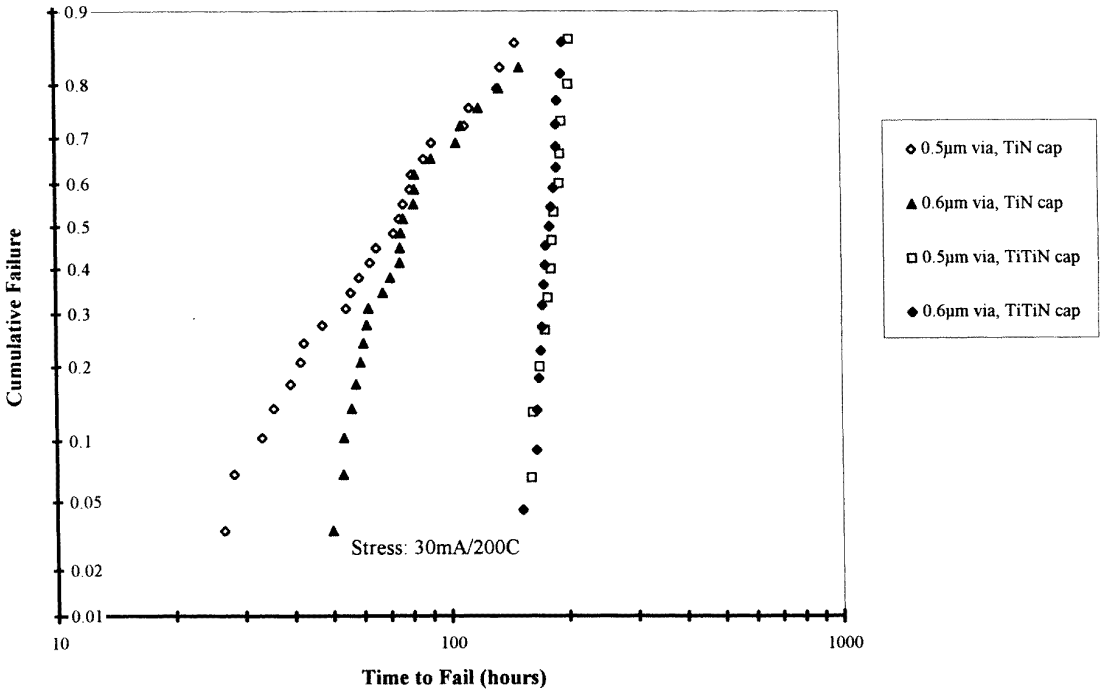

Figure 5. TF distribution of 0.5 μm and 0.6 μm vias in a Ti/TiN cap system. The e-flow direction was from metal 2 to metal 1.

4. Failure analysis and discussion of results

As representatives of the failing structures, five failing structures (with TiN caps) were removed from the test oven soon after a 20% rise in resistance was recorded. These units had been stressed at 30 mA/200 °C with e-flow being from metal 2 to metal 1. Via-plus-lead resistance was measured at room temperature across both the two stressed terminals (R_s) and the two unstressed terminals (R_u) in the Kelvin arrangement of leads as shown schematically in figure 6. R_s was found to be approximately equal to R_u. This result indicates that most of the damage occurred in the

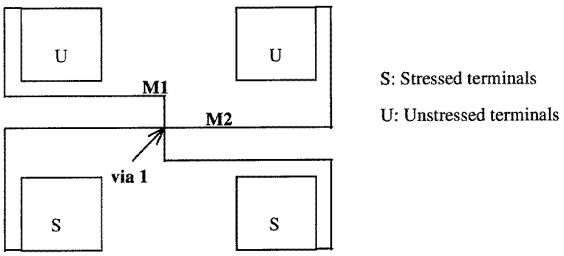

Figure 6. Via 1 (interconnection between metal 1 and metal 2) Kelvin structure used in this study.

neighbourhood of the W-plug. Similar room-temperature measurements done on five failing via structures taken out after a 50% rise in resistance indicated that R_s was greater than R_u, implying that the void propagated downstream from the via. The averaged values of R_s and R_u of five failing units measured after 20% and 50% rises in resistance are summarized in table 2.

Three units, consisting of the third failing unit (early fail), the thirteenth failing unit (median fail) and the twenty-fourth failing unit (late fail), were cross sectioned during failure analysis. SEM results indicated that there were at least three different failure modes associated with the via EM time-to-failure distribution. A SEM cross section of the early failing unit indicated that the W-plug was forced down into metal 1 during EM testing in the direction of the electron wind. The via failure in this case consisted of two simultaneous processes: first, the drifting away of AlCu at the bottom of the via due to flux divergence and secondly, a pressure increase from the top of the W-plug due to the accummulation of AlCu in metal 2. Eventually, when the pressure from the top of the via was high enough and the void at the bottom of the via was large enough, the Ti/TiN liner in the via failed, resulting in the W-plug being forced into metal 1 as shown in figure 7. The evidence supporting the W-plug movement hypothesis is strong. First, prior to

Table 2. Averaged values of resistances measured at room temperature across the stressed and unstressed terminals after a 20% and 50% rise in resistance.

ΔR (%)	R_s (Ω)	R_u (Ω)
20	15.9 ± 0.36	15.8 ± 0.24
50	19.8 ± 0.42	16.0 ± 0.31

stressing, the via resistance was completely normal. This implied that the W-plug was not in the position as shown in figure 7 prior to stressing. Secondly, the electrical failure analysis done on the VDP via structures after being stressed indicated that the damage occurred at the via. Thirdly, the W-plug is seen to be deformed into an hour-glass shape that could not have been created by a via etch cutting severely into metal 1 and then the tungsten being CVD-deposited. Finally, the existence of severe mechanical stress at the top of the via can be seen from figure 7, where delamination/cracking of the interlevel oxide is apparent. Via size, in this case, played an important role since it determined the current density at the W/Al interface and consequently affected the TF of the device.

SEM cross section of the medial time-to-failure unit in the time-to-failure distribution showed that the via etch had stopped on the TiN cap. The TiN capping layer serves as a current spreader, increasing the effective conductive area at the W/Al interface. This effective area increase tended to reduce the flux divergence, and as a result, slowed down the onset of EM failure. In this case, the W-plug was not forced into metal 1, as is shown in figure 8.

Like that of the early failing unit, SEM cross section of the late-failing unit (see figure 9) from the time-of-failure distribution showed that the via etch stopped inside the aluminium, yet there was no evidence of W-plug movement during EM testing. Void formation was observed along the boundaries between AlCu and the TiN barrier, and between AlCu and the surrounding dielectric, but not at

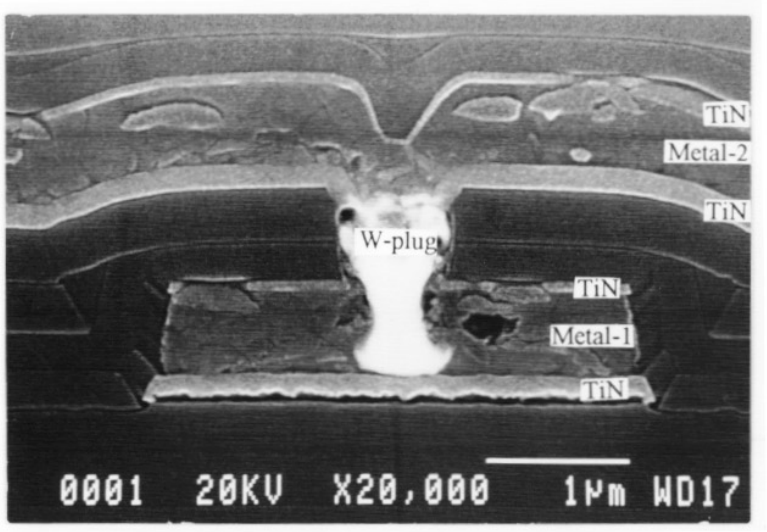

Figure 7. SEM micrograph showing the displaced W-plug (the early time-to-failure unit). The e-flow direction was from metal 2 to metal 1. Al voiding is evident in metal 1.

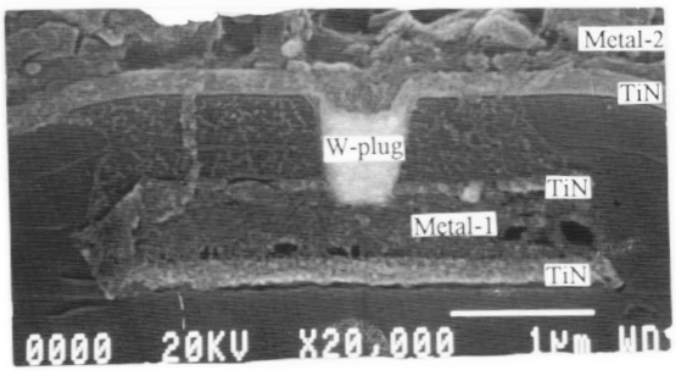

Figure 8. SEM micrograph showing the median time-to-failure unit. The e-flow direction was from metal 2 to metal 1. Al voiding is evident in metal 1.

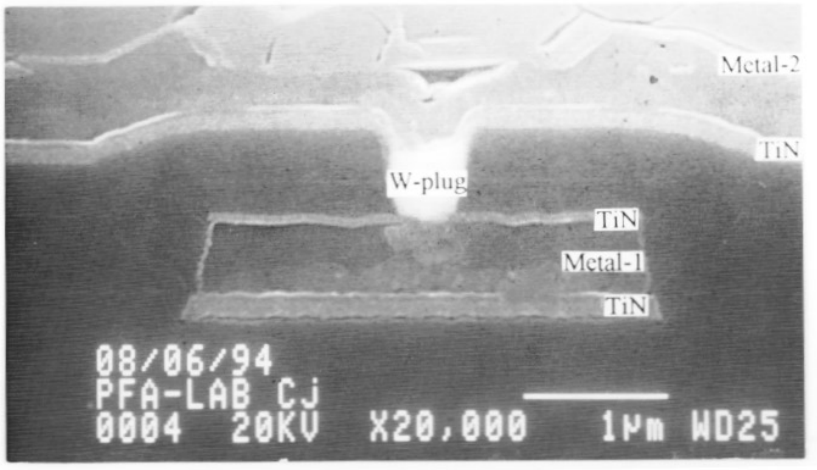

Figure 9. SEM micrograph showing the late time-to-failure unit. The e-flow direction was from metal 2 to metal 1. An accumulation of aluminium in metal 2 (over the via) is evident causing interlevel oxide cracking.

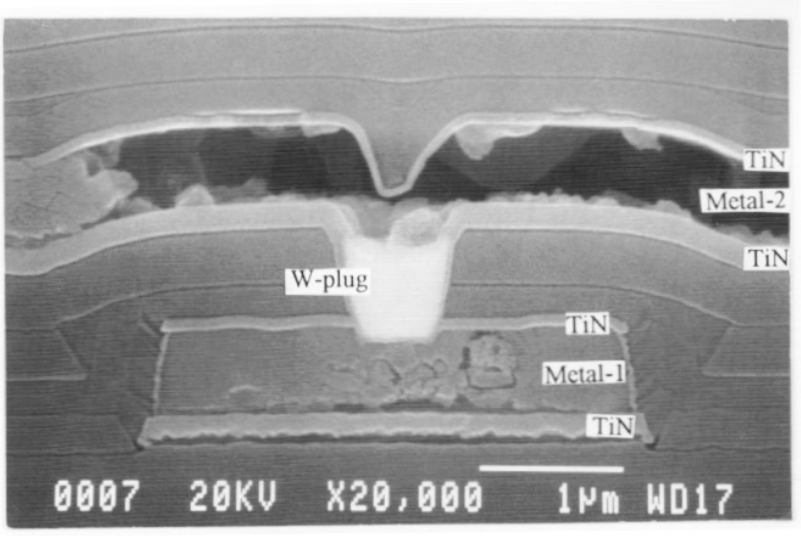

Figure 10. SEM micrograph for via failure when the e-flow was from metal 1 to metal 2. Aluminium voiding in metal 2 is evident over the via.

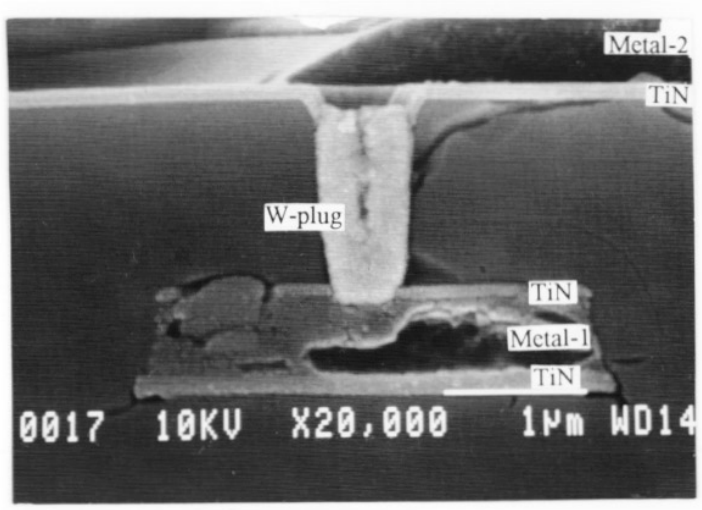

Figure 11. SEM micrograph showing void formation at the bottom of via with Ti/TiN cap. The e-flow direction was from metal 2 to metal 1. A worst-case aspect ratio of 3:1 was used for this particular evaluation. Aluminium voiding is evident in metal 1.

the W/Al interface. This type of failure indicated that interfacial diffusion was the failure mechanism responsible in this case. The fact that the aluminium did not migrate away from under the W-plug, causing W-plug movement, might have been due to the positioning of the W-plug within a single grain of aluminium (no grain boundaries in the vicinity of the W-plug). This might have reduced or eliminated the grain boundary diffusion of Al atoms away from underneath the W-plug.

For the via with TiN cap, when e-flow direction was from metal 1 to metal 2, the TiN barrier in metal 2 served as a current spreader which tended to minimize the current crowding effect due to small via size. As a result, there was no statistical difference between the 0.5 μm and 0.6 μm via time-to-failure distributions (figure 3). This type of structure also prevented the W-plug from moving (figure 10) because the continuous TiN barrier in metal 2 protected the W-plug.

Similarly, for the via with a Ti/TiN cap, when the e-flow was from metal 2 to metal 1, the onset of EM failure was slowed down by a continuous and hard $TiAl_3$ intermetallic layer formed by the interaction of Ti and Al as shown in figure 11. The e-flow entered the metal lead through the 'effective' current spreader in this case ($TiAl_3$ intermetallic layer). This served to create a gradual transition of current density from inside of the via to the W/Al interface and finally to the Al stripe. In addition, the continuous intermetallic compound $TiAl_3$ mechanically strengthened the W/Al interface. For this special evaluation, a worst-case via aspect ratio of 3:1 was used. All other evaluations used a via aspect ratio of 1:1.

5. Conclusions

In a VLSI metallization system with TiN cap and W-plug via, 0.5 μm and 0.6 μm vias have different TF distributions when the electron flow is from metal 2 to metal 1. The early failures can be described as 'W-plug failure', because damage was restricted primarily to the via for a 20% resistance rise, i.e. little to no damage occurred in the servicing metal stripes. In some cases, the W-plug was forced down into a voiding metal 1 by aluminium accumulation in metal 2. Vias with etch stop on the TiN cap tended to outperform vias with etch stop in metal 1.

When the electron flow was from metal 1 to metal 2, there was no statistical difference between the 0.5 μm and 0.6 μm via TF distributions. This indicated that the time-to-failure is independent of via size, i.e. independent of via current density, and is thought to be due to the current spreading effect of the TiN barrier in metal 2. Ti-capped metal shows superior via EM performance due to the formation of a continuous $TiAl_3$ intermetallic layer which serves as a current spreader and a stronger barrier.

Acknowledgments

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