Analysis of Gate-Bias-Induced Heating Effects in Deep-Submicron ESD Protection Designs

Kwang-Hoon Oh, *Student Member, IEEE*, Charvaka Duvvury, *Senior Member, IEEE*, Kaustav Banerjee, *Member, IEEE*, and Robert W. Dutton, *Fellow, IEEE*

***Abstract*—This paper presents a detailed investigation of the degradation of electrostatic discharge (ESD) strength with high gate bias for deep-submicron salicided ESD protection nMOS transistors, which has significant implications for protection designs where high gate coupling occurs under ESD stress. It has been shown that gate-bias-induced heating is the primary cause of early ESD failure and that this impact of gate bias depends on the finger width of the protection devices. In addition, it has been established that substrate biasing can effectively alleviate the adverse impact of the gate bias and can improve ESD strength despite the gate-coupling level. Improved understanding of ESD behavior for advanced devices under high gate-coupling conditions can extend design capabilities of protection structures.**

***Index Terms*—Electrostatic discharges, ESD protection, gate-bias-induced heating, salicided nMOS transistor, second breakdown triggering current.**

I. Introduction

FOR multifinger nMOS protection, it has been recognized that the gate coupling technique is efficient since it ensures uniform triggering of the lateral n-p-n bipolar transistors [1], [2]. However, its effectiveness is dubious in silicided processes [3]. Additionally, it is also well known that excess gate coupling degrades the second breakdown triggering current I_{t2} of nMOS devices [4], [5] and, thus, design techniques have been used to limit the gate coupling. Even with controlled gate coupling on the protection device, under electrostatic discharge (ESD) stress, high gate coupling on the output nMOS transistor causes human-body model (HBM) or charged-device model (CDM) failures in output buffer protections, thereby placing some restrictions on the design of ESD protection. This phenomenon of degradation of I_{t2} is technology dependent and its impact on the advanced protection design has not been fully explored. Moreover, for advanced salicided technologies, the severity of this effect has been shown to be dependent on the finger width and the extent of lateral uniformity of ESD current conduction [6]. In this work, we identify the root cause of this degradation of I_{t2} with high gate bias for a 0.13-μm technology and also investigate the impact of substrate bias on the gate-coupling effect. Accounting for this ESD behavior involved in advanced salicided devices, design guidelines useful for designing protection structures are also presented.

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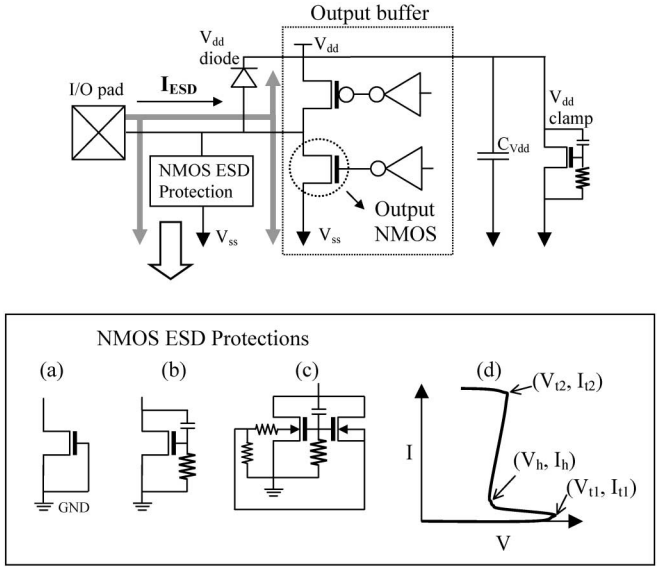


Fig. 1. Simplified output buffer protection scheme with various protection nMOS transistor options. Irrespective of protection transistor options, under ESD conditions, high ESD voltage can be fed into the gate of the output nMOS transistor, which could lead to early ESD failures. (The gray arrows indicate the ESD current paths.) (a) Gate-grounded nMOS. (b) Gate-coupled nMOS. (c) Substrate-pump nMOS. (d) Generalized high-current I–V characteristics of the gate-grounded nMOS.

II. Output NMOS Failure

A typical output buffer protection scheme with different protection device options is shown in Fig. 1. In ESD protection circuits, there are several nMOS protection structures available, such as the gate-grounded nMOS (GGNMOS), the gate-coupled nMOS (GCNMOS), and the substrate-pump nMOS structures. Especially, both the GCNMOS and substrate-pump nMOS have been proposed to ensure uniform lateral bipolar current conduction [5], [7]. Under ESD stress from the I/O pad to the ground, the ESD current is shared by the several different competing current paths, mostly through the nMOS protection structures and partially through the lateral V_{dd} diode and the output nMOS transistor itself. During such conditions, the potential of the I/O pad reaches the voltage level enough to trigger the nMOS protection structure and, finally, the voltage of the I/O pad remains near the holding voltage V_h depending on the nMOS protection options. The ESD current through the

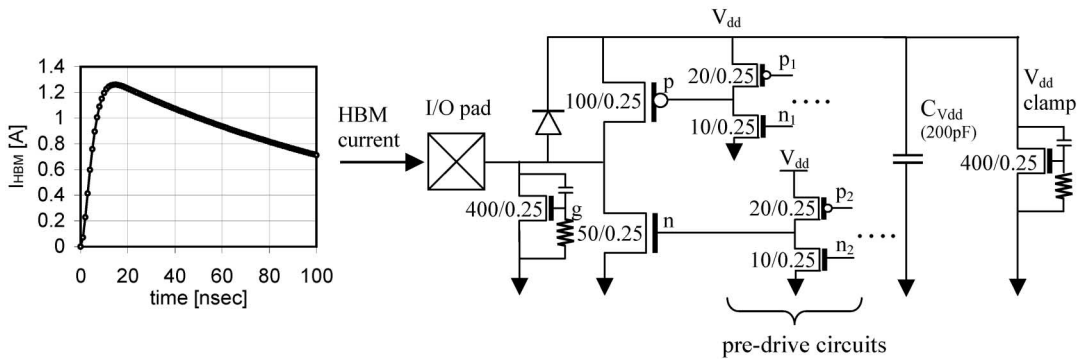


Fig. 2. Schematic of the standard 2-kV HBM tests for the simple output buffer protection circuit.

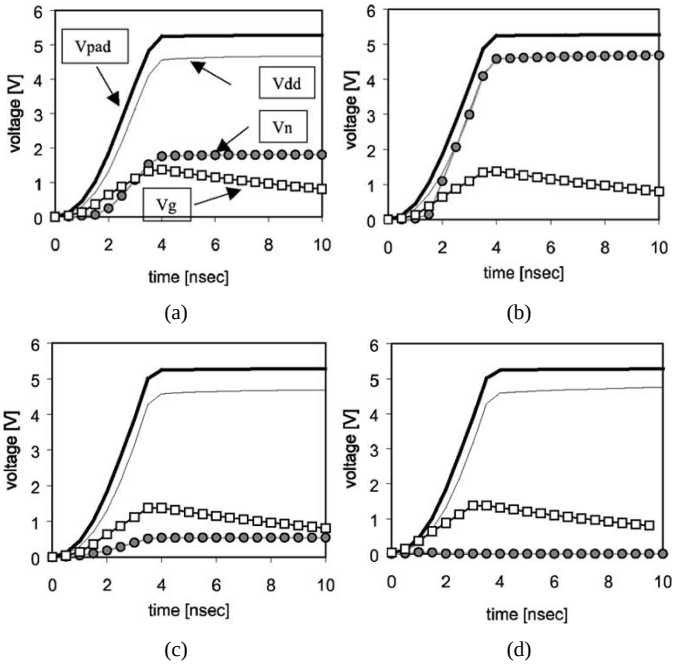


Fig. 3. Simulated voltage waveforms of each node of the output buffer protection under 2-kV HBM stress with the four different predrive circuit conditions. (a) $p_1 = p_2 =$ low and $n_1 = n_2 =$ high. (b) $p_1 = p_2 = n_1 = n_2 =$ low. (c) $p_1 = p_2 =$ high and $n_1 = n_2 =$ low. (d) $p_1 = p_2 = n_1 = n_2 =$ high.

lateral diode to the V_{dd} node charges the V_{dd} capacitance up to about $V_h - 0.7$ V. It should be noted that the maximum voltage of the V_{dd} node is also limited by the presence of the V_{dd} clamp. As a result, depending on the predrive circuit conditions, this voltage (at the V_{dd} node) can be fed into the gate of the output nMOS transistor through internal circuit blocks, which can influence the effectiveness of the ESD protection design. By using HSPICE, a 2-kV HBM test mode was reproduced for a simplified output buffer protection scheme shown in Fig. 2 [8]. A 3.3-V nMOS transistor model was used, which has a holding voltage of $\sim$ 5.3 V. Initially, all the nodes are floating and then voltages at the I/O pad and V_{dd} line start to increase with the injection of the standard 2-kV HBM current. The gate voltage of the output nMOS transistor is determined depending on the condition of the predrive circuits of the output devices. Typically, the predrive circuits can have the logic value of either high (1) or low (0). Since the predrive circuit condition is unpredictable at the ESD event, by assuming different conditions

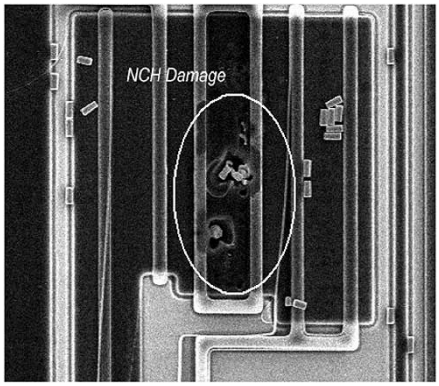


Fig. 4. Failure image of the output nMOS transistor in HBM test mode. Since increased gate voltage of the device due to high gate coupling lowers its ESD strength, the device fails earlier than the protection devices.

of the predrive circuits, the gate potential of the output nMOS and protection nMOS transistors was investigated. As shown in Fig. 3, with conditions (a) and (b), the gate voltage V_n of the output nMOS transistor increases with a slight delay and finally goes higher than that of the protection nMOS device V_g, which can lead to a reduction in the ESD strength relative to the protection device. On the other hand, for conditions (c) and (d), the gate potential of the output nMOS stays below 0.5 V and, thus, no severe I_{t2} degradation is expected. For the simulation, the gate voltage of the output nMOS transistor ranges from ground to the voltage at V_{dd} ($\sim$ 4.8 V) depending on the conditions of the predrive circuits and similar effects can take place for any other potential values induced at the V_{dd} node. Therefore, the gate-bias effect for the output nMOS transistor has significant implications for the overall design of ESD protection. In Fig. 4, the early ESD failure of the output nMOS transistor has been shown for HBM test due to the high gate-coupling-induced I_{t2} degradation, regardless of the ESD strength of the protection device itself. The same failure mode has also been observed for the CDM tests.

III. Experiments and Analysis

In this study, 1.5-V ($L_{\text{poly}} = 0.175$ μm and $t_{\text{ox}} = 27$ Å) and 3.3-V ($L_{\text{poly}} = 0.5$ μm and $t_{\text{ox}} = 70$ Å) single-finger ESD nMOS transistors, manufactured using a salicided 0.13-μm technology, have been investigated. In order to observe early ESD failure with excess gate coupling, involving various gate-bias conditions, I_{t2} was measured with the transmission line pulsing

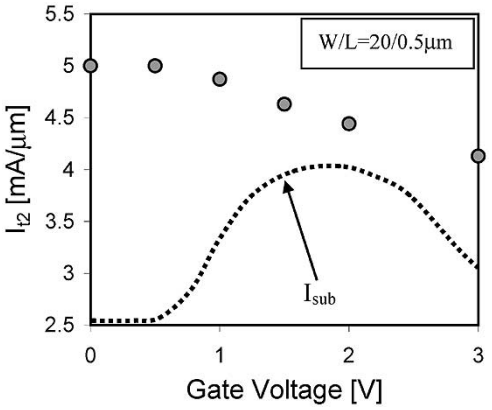


Fig. 5. Second breakdown triggering current I_{t2} versus gate voltage for a salicided ($TiSi_2$) 0.35-μm technology node. The dotted line is the well-known substrate current (in arbitrary unit) for conventional nMOS transistors, which shows that the degradation of I_{t2} is not due to the substrate current behavior as a function of gate bias and further suggests that the turn-on efficiency of the parasitic n-p-n transistor is not the primary cause of this phenomenon.

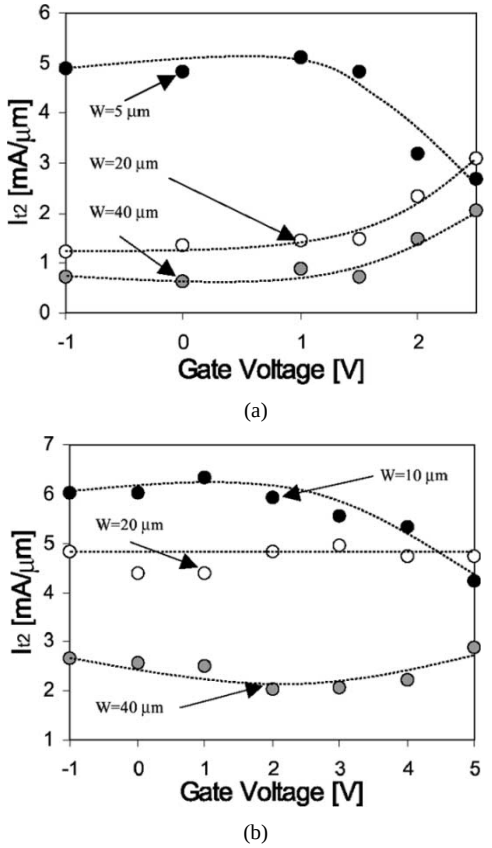


Fig. 6. Second breakdown triggering current I_{t2} with gate bias for the two different nMOS transistors for a 0.13-μm technology. The dependence of I_{t2} on gate bias is influenced by the finger widths. Gate bias improves I_{t2} for wide-finger-width nMOS transistors, but degrades I_{t2} of narrow-finger-width devices. (a) 1.5 V nMOS. (b) 3.3 V nMOS.

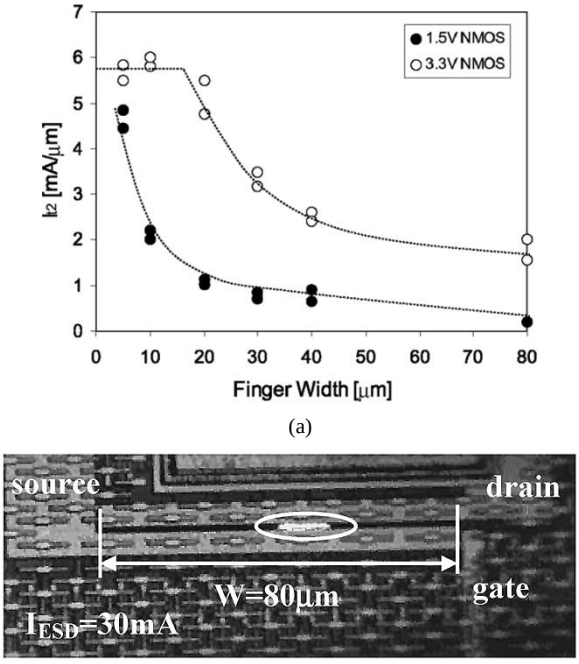


Fig. 7. (a) I_{t2} for the output nMOS transistors (both of 1.5-V and 3.3-V transistors) with $V_{gs} = 0$ V for different finger widths. (b) EMMI image of the spatial distribution of the ESD current $I_{\rm ESD}$ of 30 mA for the 3.3-V nMOS transistor. Both images show that strong nonuniform conduction occurs in salicided nMOS transistors for the 0.13-μm technology. For the EMMI analysis, a pulsed bias with duration T_p of 300 ns was applied at a frequency of 400 Hz for the exposure time $T_{\rm exp}$ of 6 min.

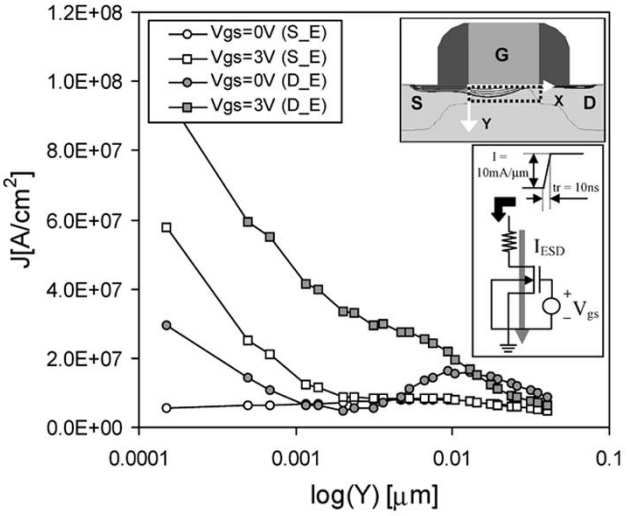
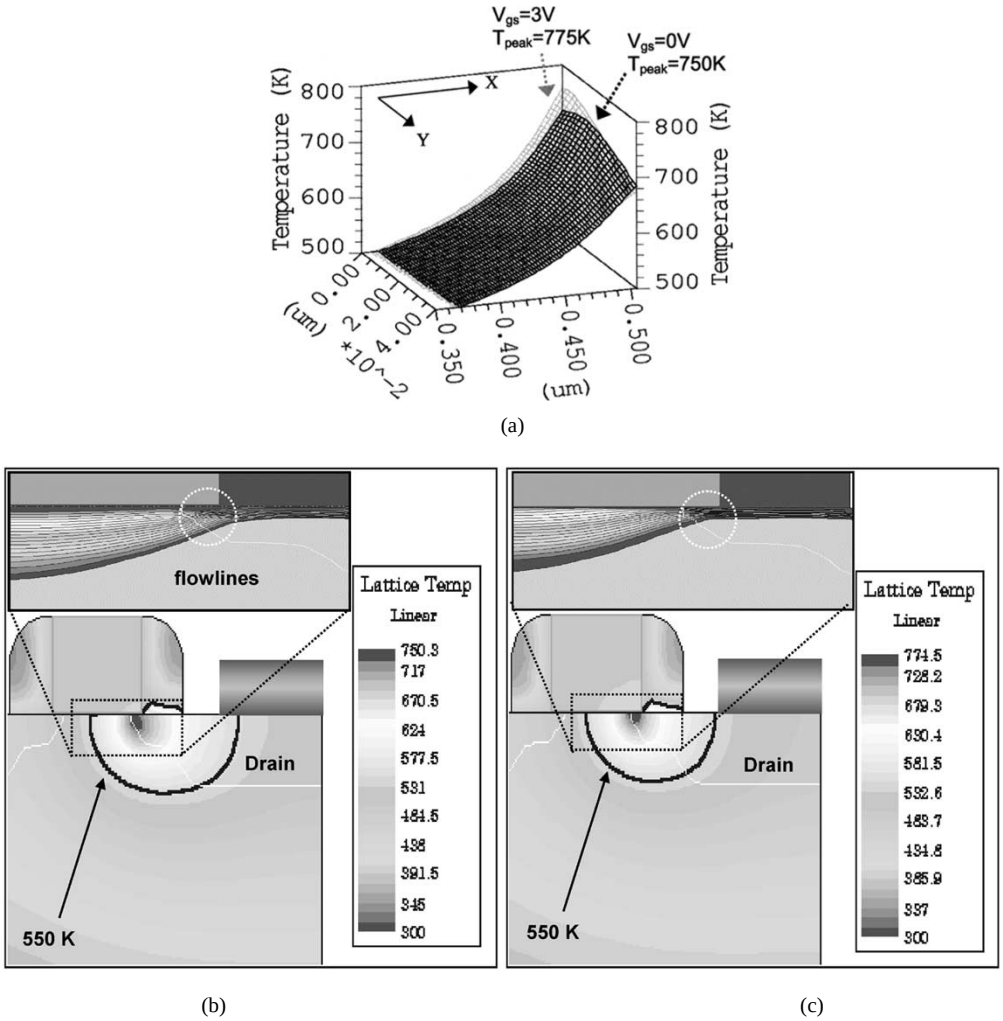


Fig. 8. Current density at the edge of source S_E and drain D_E extension along the y axis with gate bias (see the x and y axes in the rectangle underneath the gate). The schematic of the transient simulation circuit is shown in the inset.

(TLP) method with a 200-ns voltage pulse. In Fig. 5, the I_{t2} values with gate bias are shown for a 0.35-μm technology. As can be seen, contrary to the conventional belief, the phenomenon of degradation of I_{t2} does not follow the substrate current behavior with gate bias. This implies that the parasitic bipolar turn-on efficiency cannot be the primary cause of the I_{t2} degradation and, furthermore, that there is a new physical mechanism governing this phenomenon. In addition, it has been recently reported that ESD current distributes nonuniformly depending on the finger width and under ESD conditions the effective width of devices is limited by the extent of the nonuniformity of the bipolar current distribution [9], which throws new light on the gate-bias-induced phenomenon.

For advanced salicided devices in a 0.13-μm technology, the impact of gate bias on I_{t2}, which can be clearly observed in



(a)

(b) (c)

Fig. 9. Local temperature rises with (a) $V_{gs} = 0$ V and $V_{gs} = 3$ V and temperature contours with (b) $V_{gs} = 0$ V and (c) $V_{gs} = 3$ V. The simulations indicate that the channel and drain extension area undergo more heating and that the temperature distribution is more localized with gate bias.

Fig. 6, is also finger-width dependent for both low-voltage and high-voltage nMOS transistors. The I_{t2} dependence on the gate bias is no longer consistent with Fig. 5 for the $W = 20$ μm and $W = 40$ μm devices of the 0.13-μm technology node. Contrary to the dependence observed in the 0.35-μm technology node, opposite trends appear depending on the gate finger width of the nMOS transistor. This implies that the gate bias can result in two different competing physical mechanisms depending on the finger width for a given structure. As shown in Fig. 7(a), the I_{t2} values of the advanced salicided transistors are severely degraded with increasing finger widths. The ESD current distribution is uniform within a very narrow finger width such as $W<5$ μm for the low-voltage (1.5-V) transistors and $W\leq 10$ μm for the high-voltage (3.3-V) transistors. In addition, the emission microscopy (EMMI) images with a pulsed bias condition shows that only a small part of the finger width is effective for the ESD current conduction in the 80-μm-wide salicided nMOS devices [Fig. 7(b)]. Further increase in the drain-current level caused thermal damage without full triggering of the nMOS transistor. This strong width dependence of I_{t2} for advanced technologies is attributed to the localized (nonuniform) bipolar conduction. As discussed in [9], this nonuniform bipolar conduction becomes more serious for devices with low resistance substrates and silicided diffusions. Considering the results in Figs. 6 and 7, it can be inferred that gate bias can improve I_{t2} of the wide finger devices ($W = 20$ μm and $W = 40$ μm) where the ESD currents are nonuniform. On the other hand, the I_{t2} of the narrow finger device ($W = 5$ μm for 1.5-V nMOS and $W = 10$ μm for 3.3-V nMOS), where ESD current is known to conduct almost uniformly, is degraded with gate bias.

IV. Simulations and Discussion

As is well known, boosting of the substrate current with gate bias can minimize the current localization under ESD conditions. This mechanism seems to work for the wide-finger 1.5-V nMOS devices [see Fig. 6(a)] with considerable improvement of I_{t2}, while the improvement of I_{t2} for the 3.3-V devices is less apparent [Fig. 6(b)]. However, the severe reduction in I_{t2} with gate bias for the narrow transistors cannot be described by this mechanism involved in the efficiency of the lateral n-p-n structure. Hence, to comprehend the underlying physical mechanism that leads to early ESD failure, electrothermal transient simulations have been performed for a structure that was devised using TSUPREM-4 [10]. Due to the relatively lower thermal conductivity of the passivation layers and shallow trench

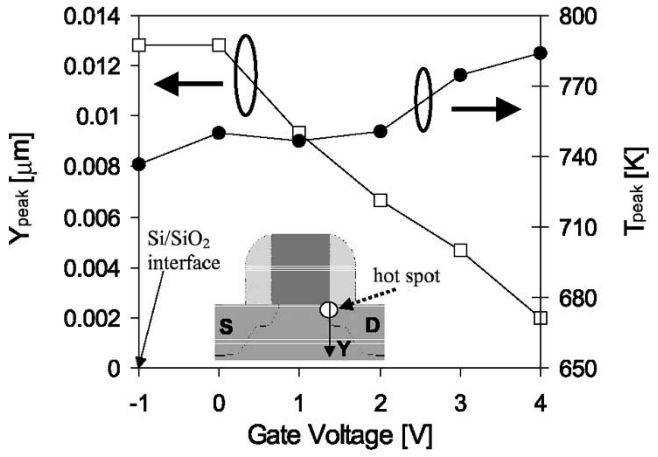


Fig. 10. Location of peak temperature and the peak temperature value with gate bias. With increase in gate bias, $Y_{\rm peak}$ moves closer to the surface and the peak temperature $T_{\rm peak}$ also increases moderately.

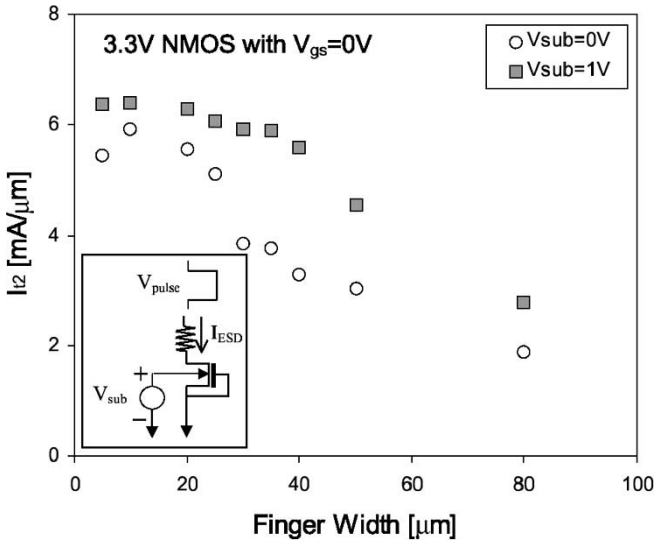
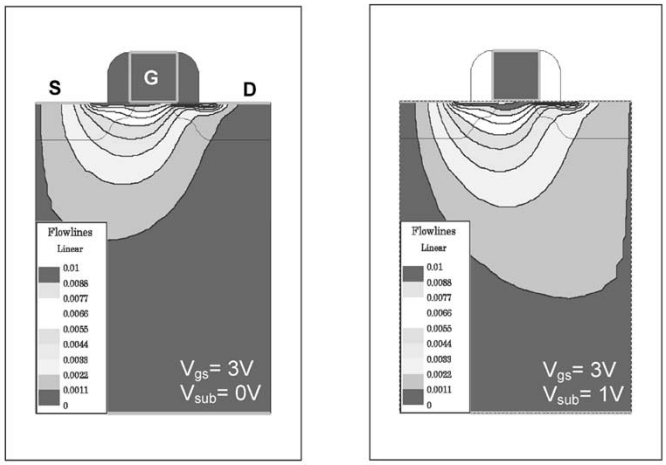


Fig. 11. Impact of substrate bias on the I_{t2} with finger widths.

isolation (STI) structures, all the generated heat in the device is assumed to flow toward the substrate of nMOS structure, and the temperature of the substrate is set to the ambient temperature. This thermal boundary condition reasonably represents the actual wafer-level test environment and is verified by using the thermal simulator ANSYS [11]. As shown in Fig. 8, the current density within the source/drain extension junction depth is strongly modulated by gate bias. This implies that the distribution of the local temperature rise in the drain extension and the channel area (indicated by the rectangle in nMOS) can also be influenced by the applied gate bias. At a given drain current of 10 mA/μm (at $t = 10$ ns), the local temperature rise in the box, depending on the gate bias, is shown in Fig. 9. The simulation results show that the distribution of the local temperature near the channel area as well as the peak temperature increases as gate bias increases. Also, the isothermal line of 550 K shows that the temperature distribution becomes more localized with the gate bias. In addition, as shown in Fig. 10, the location of the maximum temperature has been simulated with gate bias. For the negative gate bias, the location of the peak temperature does not change at all. This simulation result suggests that I_{t2} remains the same with the negative gate bias. This observation agrees well with the measured data in Fig. 6. However, the surface heating becomes stronger with the gate bias since the location of the peak temperature approaches the Si/SiO_2 interface. The overall simulation results indicate that more heat can be accumulated within a smaller volume near the surface with gate bias and the device tends to be more vulnerable to thermal failures at the surface. Hence, this gate-bias-induced heating effect can lead to I_{t2} degradation in devices where the lateral ESD currents flow uniformly. At this point, it is instructive to note that a recent work [12] has reported that for sub-180-nm devices, the heat-diffusion equation underestimates the maximum device temperature compared to the one based on phonon Boltzmann transport equation. Therefore, the temperature value from the simulation (MEDICI) may not be accurate enough to predict the exact failure threshold of the device, but it provides a relative dependence of thermal effects on the bias conditions for a structure of interest.



(a) (b)

Fig. 12. Simulated current flowlines in the presence of gate bias with (a) $V_{\rm sub} = 0$ V and (b) $V_{\rm sub} = 1$ V. With substrate bias, the current flows more deeply into substrate and this leads to increase in effective volume for power dissipation.

To verify this heating effect, I_{t2} was also measured with both the gate and the substrate bias. As shown in Fig. 11, with substrate bias, I_{t2} increases since the maximum turned-on width of the nMOS device is increased. Also, with substrate bias, the ESD currents spread out deeper into the silicon substrate despite the presence of gate bias, as shown in Fig. 12. As a result, the effective volume for power dissipation can be augmented. This suggests that the reduction in I_{t2} with gate bias could be alleviated by applying appropriate substrate bias, since the lateral ESD currents conduct more deeply into the silicon substrate with reduced current density near the surface and, in turn, the heating is reduced, as shown in Fig. 13. The experimental I_{t2} values confirm our argument, as shown in Fig. 14. Despite high gate bias, the degradation of I_{t2} for both low-voltage and high-voltage transistors is mitigated with substrate bias. Hence, using the insightful results from device simulation and experimental data, it can be concluded

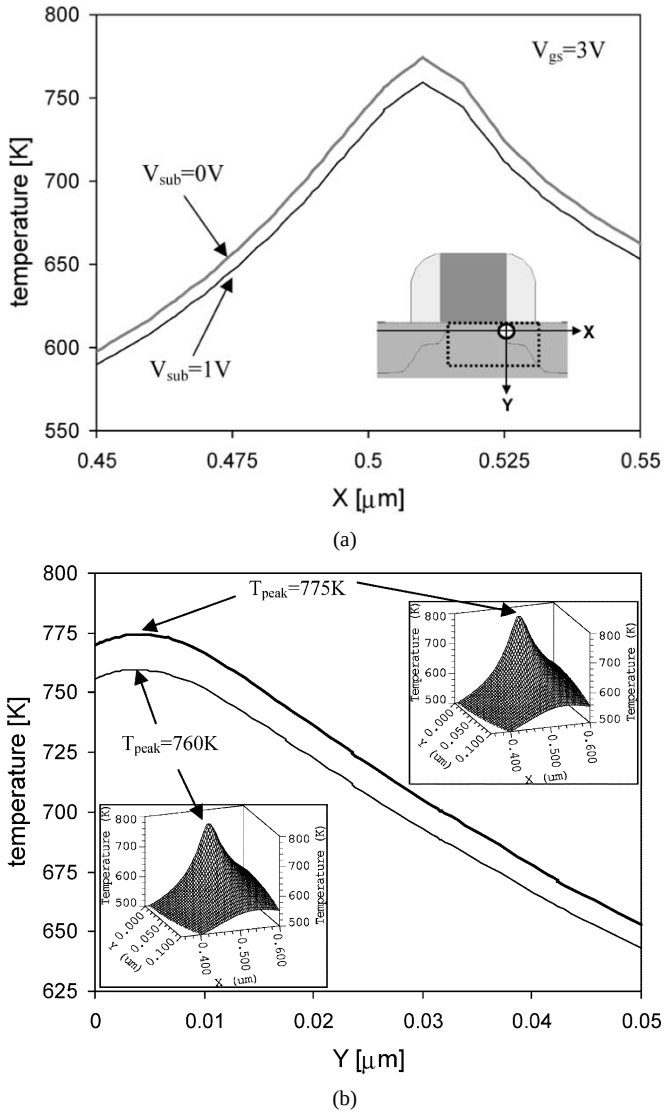


Fig. 13. Temperature distribution with substrate bias in the presence of gate bias. (a) Temperature distribution along the x axis. (b) Temperature distribution along the y axis where $T_{\rm peak} = 775$ K for $V_{\rm sub} = 0$ V and $T_{\rm peak} = 760$ K for $V_{\rm sub} = 1$ V.

that gate-bias-induced heating effect primarily accounts for the reduction in I_{t2} for devices with uniform lateral ESD current conduction. Based on these results, useful design considerations can be drawn for advanced salicided ESD protection. Hence, for the substrate trigger protection [7], [9], I_{t2} rolloff with gate bias is not important. In fact, protection can be designed with the GGNMOS structures as long as substrate bias is supplied for an efficient multifinger n-p-n. On the other hand, for the design of the gate-coupled ESD protection devices without substrate bias, the gate of the protection device should be designed with appropriate values of R and C [Fig. 1(b)] to maintain the gate bias below the level above which I_{t2} begins to roll off with the gate bias. Finally, for the output transistor, since the substrate bias is not available and the gate coupling is unpredictable, the buffer size should be designed based on the failure current component that it can handle, which depends on its gate-coupling level. For the above-described ESD protection design, the gate-coupling level and the optimum size of devices can be determined with high-current ESD circuit simulations,

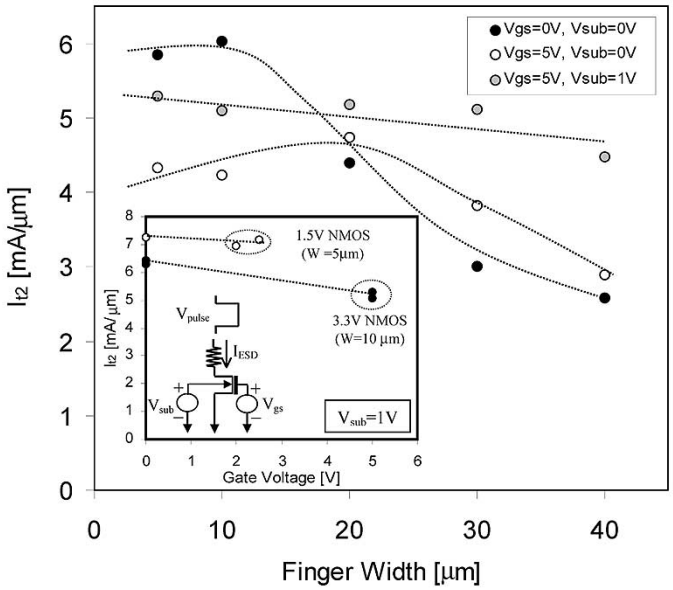


Fig. 14. Effect of substrate bias on the I_{t2} degradation for high-voltage (3.3-V) nMOS transistors with different finger width and gate bias, which shows that I_{t2} degradation is alleviated with substrate bias. The inset also shows the impact of substrate bias on I_{t2} degradation for narrow-finger, high-voltage, and low-voltage transistors.

which show the primary ESD current paths as well as the weak points for ESD [13].

V. Conclusion

An extensive investigation into the degradation of ESD strength with gate bias has been carried out to provide improved understanding of ESD behavior and new insight into the gate-bias effect involved in advanced salicided nMOS devices. It has been shown that gate-bias-induced heating near the drain extension region close to the Si/SiO_2 surface is the primary cause of this degradation. It has also been established that substrate biasing can help eliminate the negative impact of the gate bias effect. Results from this work can be used to generate design guidelines for efficient and robust ESD protection design, including compatible output buffer design, to overcome ESD failures in advanced deep-submicron technologies.

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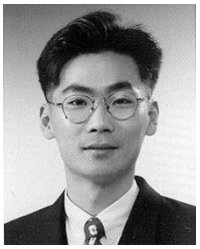

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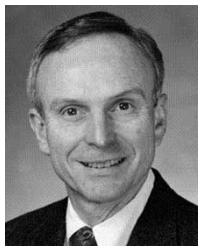
After working as a Postdoctoral Fellow in Physics with the University of Alberta, Edmonton, AB, Canada, he joined Texas Instruments Incorporated (TI), Houston, TX, in 1977. He initially worked in the Houston DRAM group as a Design/Product Engineer for the 4K/16K DRAMS. He then was part of the first 256K CMOS DRAM design and the Advanced Development group that worked on the 1 M DRAM with specific contributions in DRAM circuit design, transistor modeling, and reliability studies. He joined the Semicondutor Process and Device Center, TI, Dallas, TX, in 1988, where his work was on the transistor modeling of CMOS/BiCMOS technologies, and development of ESD protection for high-voltage designs and submicron CMOS technologies. He was elected Senior Member of the Technical Staff in 1990, Distinguished Member of the Technical Staff in 1997, and TI Fellow in 1997. His current research is on ESD developemnt for the deep-submicron CMOS technologies. He has published over 65 papers in technical journals and conferences, and holds 25 patents with several pending. He has coauthored books on hot carriers, modeling of electrical overstress, and ESD reliability phenomena and protection design.

Dr. Duvvury received the Outstanding Contributions Award from the EOS/ESD Symposium in 1990, the Outstanding Mentor Award from the SRC in 1994, several Best Paper Awards from the EOS/ESD Symposium, and an Outstanding Paper Award from the International Reliability Physics Symposium. He is a member of the ESD Association Board of Directors. He was Technical Program Chairman of the 1992 Symposium and General Chairman of the 1994 ESD Symposium. He is a member of Eta Kappa Nu and Sigma Xi.

Kaustav Banerjee (S'94–M'99) received the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley in 1999.

He was with Stanford University, Stanford, CA, from 1999 to 2002 as a Research Associate with the Center for Integrated Systems. In July 2002, he joined the faculty of the University of California at Santa Barbara as an Assistant Professor with the Department of Electrical and Computer Engineering. His research interests include nanometer-scale circuit effects and their implications for high-performance/low-power VLSI and mixed-signal designs and their design automation methods. He is also interested in some exploratory interconnect and circuit architectures such as three-dimensional ICs, integrated optoelectronics, and nanotechnologies such as single-electron transistors. He co-mentors several doctoral students at Stanford University. He also co-advises doctoral students in the electrical engineering departments of the University of Southern California, Los Angeles, and the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland. From February 2002 to August 2002, he was a Visiting Professor at the Microprocessor Research Laboratories, Intel, Hillsboro, OR. In the past, he has also held summer/visiting positions with Texas Instruments Incorporated, Dallas, TX, and the EPFL, Lausanne, and has served as a Consultant for Magma Design Automation, Cupertino, CA, and Fujitsu Laboratories of America, Sunnyvale, CA. He has authored or coauthored over 70 technical papers in archival journals and referred international conferences, and has presented numerous invited lectures and tutorials.

Dr. Banerjee served as Technical Program Chair of the 2002 IEEE International Symposium on Quality Electronic Design (ISQED'02) and is the Conference Chair for the ISQED'03. He also serves on the technical program committees of the ACM International Symposium on Physical Design, the EOS/ESD Symposium, and the IEEE International Reliability Physics Symposium. He was the recipient of a Best Paper Award at the 2001 ACM Design Automation Conference.



Robert W. Dutton (S'67–M'70–SM'80–F'84) received the B.S., M.S., and Ph.D. degrees from the University of California at Berkeley in 1966, 1967, and 1970, respectively.

He is Professor of electrical engineering with Stanford University, Stanford, CA, and Director of Research in the Center for Integrated Systems. He has held summer staff positions at Fairchild, Bell Laboratories, Hewlett-Packard, IBM Research, and Matsushita in 1967, 1973, 1975, 1977, and 1988, respectively. He has published more than 200 journal articles and graduated more than 48 doctoral students. His research interests focus on IC process, device, and circuit technologies, especially the use of computer-aided design (CAD) in device scaling and for RF designs.

Dr. Dutton was Editor of the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS from 1984 to 1986. He was the winner of the 1987 IEEE J. J. Ebers Award, the 1996 Jack A. Morton Award, the 1988 Guggenheim Fellowship to study in Japan, and the 2000 C&C Prize (Japan). He was elected to the National Academy of Engineering in 1991.