

Analytical Modeling of Single Electron Transistor for Hybrid CMOS-SET Analog IC Design

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Abstract—A physically based compact analytical single electron transistor (SET) model is proposed for hybrid CMOS-SET analog circuit simulation. The modeling approach is based on the “orthodox theory” of single electron tunneling, and valid for single or multi gate, symmetric or asymmetric devices and can also explain the background charge effect. The model parameters are physical device parameters and an associated parameter extraction procedure is reported. The device characteristics produced by the proposed model are verified with Monte Carlo simulation for large range of drain to source voltages ($|V_{DS}| \leq 3e/C_{\Sigma}$) and temperatures [$T \leq e^2/(10k_B C_{\Sigma})$] and good agreements are observed. The proposed model is implemented in a commercial circuit simulator in order to develop a computer-aided design framework for CMOS-SET hybrid IC designs. A series of SPICE simulations are successfully carried out for different CMOS-SET hybrid circuits in order to reproduce their experimental/Monte Carlo simulated characteristics.

Index Terms—Analog hardware description language (AHDL), CMOS-nano codesign, computer-aided design (CAD), Coulomb blockade, hybrid circuits, master equation circuit simulation, Monte Carlo simulation, semiconductor device modeling, single electron transistor (SET).

I. INTRODUCTION

TREMENDOUS PROGRESS in microelectronics has pushed the MOSFET dimension toward the 10-nm limits and motivated the interest for new devices that could perform at nanoscale according to International Technology Roadmap for Semiconductors figures of merit [1]. In the near future it is then probable that CMOS will need to share its domination with fundamentally new devices, such as single electron transistors (SETs). SETs have recently attracted much attention because of their nano feature size [2], [3], ultralow power dissipation (four–five decades lower than advanced digital CMOS) [3]–[5], new functionalities [6]–[8], and CMOS compatible fabrication process [3], [9]. It also appears that CMOS and SETs are rather complementary. For example, SET shows unique advantages

in terms of low-power consumption and of new characteristics related to its unique Coulomb Blockade oscillations, while CMOS is still unrivaled in high-speed driving and voltage gain. Therefore, although a complete replacement of CMOS by SET is quite unlikely in the near future, it is also true that combining SET and CMOS, one can bring out novel functionalities [6]–[8], which are difficult to achieve in pure CMOS technology. However, designing circuits with SETs is a difficult task, because of the electrical characteristics of SETs that are governed by phenomena such as Coulomb oscillations and Coulomb blockade characteristics are quite different compared to that of MOS transistors. The aim of this paper is to contribute to the design and analysis of hybrid CMOS-SET circuits by formulating an accurate analytical model that incorporates various *physical* effects including the background charge and temperature effects, along with necessary parameter extraction procedure. The analytical model allows faster circuit analysis as compared to the Monte Carlo simulations (e.g., SIMON [10], MOSES [11] and KOSEC [12]) and master equation methods [13], [14] that are quite accurate but also very time consuming, making them ineffective even for the most basic circuits involving a few devices. On the other hand, the macro-modeling [15] approach provides little physical insight into the operation of the devices and may not be easily scalable. The proposed analytical model is incorporated in a commercial circuit simulator using an analog hardware description language (AHDL) that essentially embeds the SET model as a separate module in the circuit simulator without actually having to rigorously solve the SET characteristic equations along with other nonlinear elements in the hybrid circuit. This hybrid simulator is then used to cosimulate some CMOS-SET circuit styles and benchmarked against Monte Carlo simulations to simply provide a proof-of-concept. The results reported in this paper are promising enough to justify further investigations in large-scale hybrid CMOS-SET circuit design and analysis.

The basic schematic of a SET device, where a conductive island is sandwiched between two tunnel junctions, is depicted in Fig. 1(a). A proper operation of a SET device requires: 1) the tunnel junction resistances (R_D, R_S) to be greater than the quantum resistance ($\sim 26 \text{ k}\Omega$) to confine the electrons in the island, and 2) the charging energy of the island capacitance to be larger than the available thermal energy to avoid electron tunneling due to the thermionic emission. Fig. 1(b) demonstrates the typical Coulomb blockade oscillation behavior in SET I_{DS} – V_{GS} characteristics. It also reveals the fact that when $|V_{DS}| > e/C_{\Sigma}$ (where e is the elementary charge, C_{Σ} is the

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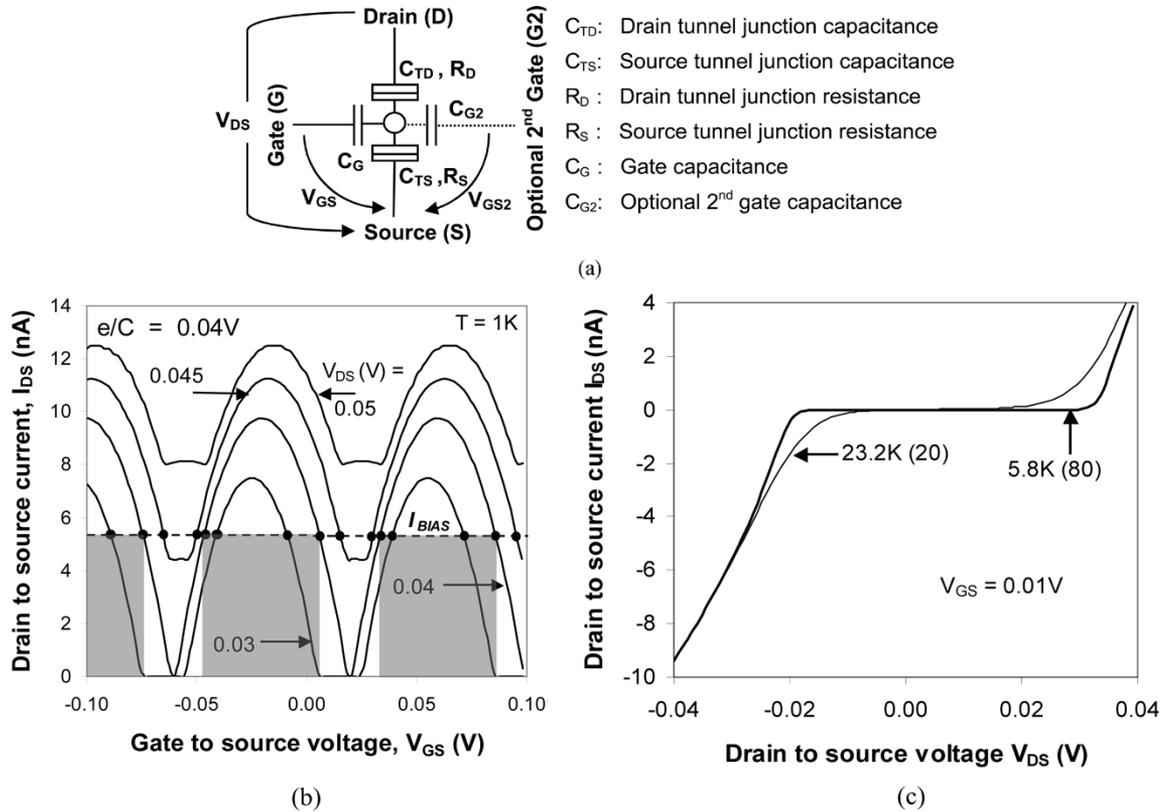


Fig. 1. (a) Schematic of a basic single electron transistor and its different device parameters. Typical $I_{DS}-V_{GS}$ characteristics (simulated by using SIMON [10]) for (b) different values of V_{DS} and, (c) different values of the temperatures (where the numbers within bracket denotes the ratio between the charging energy of the island capacitance and the available thermal energy). The solid circles represent the operating points of a constant current biased (I_{BIAS}) SET. The SET device parameters are $C_G = 2$ aF, $C_{TD} = C_{TS} = 1$ aF and $R_D = R_S = 1$ M Ω .

total island capacitance with respect to the ground), it is no more possible to obtain the Coulomb blockade (when the drain current is almost zero for certain values of V_{GS}) in the device characteristics. Therefore, for any switching application of SET, $|V_{DS}|$ should be less than e/C_Σ . However, if a SET is biased by a constant current source (I_{BIAS}), which is a basic building block for almost all analog SET/hybrid CMOS-SET architectures [6]–[8], [16], then as demonstrated in Fig. 1(b), for certain values of V_{GS} (unshaded region), the V_{DS} could be higher than e/C_Σ . Moreover, in a mixed CMOS-SET architecture, it is very difficult to maintain the V_{DS} of the SET lower than e/C_Σ , as the MOS devices are biased at higher voltages and carry much higher currents than SET [7]. Therefore, unlike digital SET circuits, the region $|V_{DS}| > e/C_\Sigma$ is equally important for analog SET IC design. The effect of temperature (T) on the device characteristics is demonstrated in Fig. 1(c), and it shows that the Coulomb Blockade region becomes thinner at higher temperatures. Therefore, an accurate compact analytical model for analog SET/hybrid CMOS-SET circuit simulation must be able to capture both the effect of temperature and the effect of high V_{DS} on the device characteristics.

Until now, to the best of our knowledge, only two compact analytical models (Uchida *et al.* [17] and Mahapatra *et al.* [5], [18]) for SET devices have been reported, which appear to be attractive for practical IC design. The model reported by Uchida *et al.* is more accurate at higher temperature but it is only applicable to the *single gate resistively symmetric*

device and does not account for the *background charge effect*, which is significant for SET operations. A very recent article [19] has proposed a scheme to extend this model to the asymmetric devices. On the other hand MIB (named after Mahapatra–Ionescu–Banerjee) [5], [18], is more flexible and can be adapted for single or multiple-gate and symmetric or asymmetric device geometries and it can also explain the background charge effect. However, as MIB considers only unidirectional electron flow, it contains fewer exponential terms (which enhances the simulation speed for large circuits), and thus is less accurate at higher temperatures at low V_{DS} . It is important to note that both these models were developed under the basic assumption of $|V_{DS}| \leq e/C_\Sigma$, which is quite practical for digital circuits. However, as explained earlier, for analog applications of SET, one needs models valid for higher values of V_{DS} as well.

In this paper, we propose an improved version of the MIB model in order to extend its validity for $|V_{DS}| > e/C_\Sigma$ and make it suitable for analog SET/hybrid CMOS-SET circuit simulations. The proposed model differs from another very recent model [20] at least in some key aspects. In our model, only one directional electron flow has been considered in order to minimize the number of exponential terms, yet keeping the accuracy at acceptable level and all analytical calculations corresponds to this assumption. Speed of the simulation and the accuracy of the proposed approach have also been compared by considering the bi-directional electron flow. In addition, a simple yet effi-

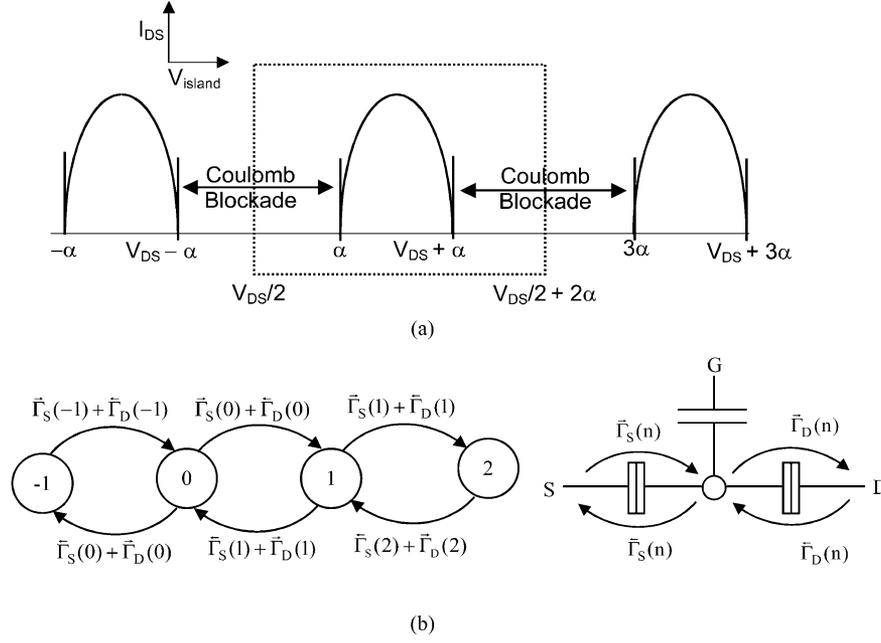


Fig. 2. (a) Schematic of SET drain current (I_{DS}) characteristics as a function of the island potential V_{island} [(2)] for any positive $V_{DS} (\leq e/C_{\Sigma})$ at $T = 0$ K. (b) Transition between different states in SET, where each state is represented by the number of electrons (n) in the island (i.e., the number inside each circle). Here, $\bar{\Gamma}_S$ (or $\bar{\Gamma}_S$) represents the electron tunneling rate from source to island (or island to source) and $\bar{\Gamma}_D$ (or $\bar{\Gamma}_D$) represents the electron tunneling rate from island to drain (or drain to island).

cient method for extracting the model parameters is presented for a generalized asymmetric device, which is essential for SET based circuit design as there is no fixed, unified technology for SET fabrication.

II. DEVELOPMENT AND VERIFICATION OF NEW MIB MODEL

A. Assumption

Proposed model MIB is based on the ‘‘orthodox theory of single electron tunneling’’ [10], where we assume the following:

- The charge is discrete but the energy is continuous.
- Tunnel junction resistance is larger than the quantum resistance (~ 26 K Ω) to ensure the confinement of the electrons on the island during SET operation.
- There is no co-tunneling.

Our model also employs another practical assumption that the interconnect capacitance associated with the gate, source, and drain terminals are much larger than the device capacitances, which ensures the total capacitance of the island with respect to ground (C_{Σ}) to be equal to the summation of all device capacitances, i.e.

$$C_{\Sigma} = C_G + C_{G2} + C_{TD} + C_{TS}. \quad (1)$$

This assures that the SET characteristics are independent of the capacitances of neighboring devices but only depend upon the nodal voltages of source, gate, and drain terminals.

B. Modeling of the Drain Current

The MIB model has been developed in three major steps: 1) calculation of the island potential, 2) shifting the drain cur-

rent window and 3) calculation of the drain current, as discussed below.

1) *Calculation of Island Potential (V_{island})*: With a certain external bias (i.e., V_{GS} , V_{GS2} and V_{DS}), before any electron tunneling takes place, the tunnel junctions act as capacitance, and therefore

$$V_{\text{island}} = \frac{C_{TD}}{C_{\Sigma}} V_{DS} + \frac{C_G}{C_{\Sigma}} V_{GS} + \frac{C_{G2}}{C_{\Sigma}} V_{GS2} - \frac{\zeta e}{C_{\Sigma}} \quad (2)$$

where ζ is a real number representing the background charge. Now, from the orthodox theory of single electron tunneling, we know that, at $T = 0$ K, the electron tunneling through any tunnel junction is only possible when the potential drop across it becomes higher than $\alpha [= e/(2C_{\Sigma})]$. Therefore, considering positive V_{DS} and grounded source, we can say that when $V_{\text{island}} > \alpha$, one electron tunnels in from the source to the island, and as a result V_{island} decreases by of 2α . Now, if the potential difference between drain-to-island is higher than α , one electron tunnels out from island to the drain (otherwise, the device enters into Coulomb Blockade region) and V_{island} increases by 2α (back to its original value). One can continue with this basic idea of electron tunneling in order to achieve the periodic drain current oscillation of a SET device as a function of the V_{island} [(2)] as demonstrated in Fig. 2(a).

2) *Shifting of the Drain Current Window*: As seen in Fig. 2(a), the drain current is a periodic function of V_{island} with a periodicity of 2α . In this paper, the drain current model has been developed only for the period: $V_{DS}/2 \leq V_{\text{island}} \leq 2\alpha + V_{DS}/2$, [which is shown by the dotted window in Fig. 2(a)] and for any other value of V_{island} one can shift by an integral multiple of 2α into this window and can apply the same model to calculate

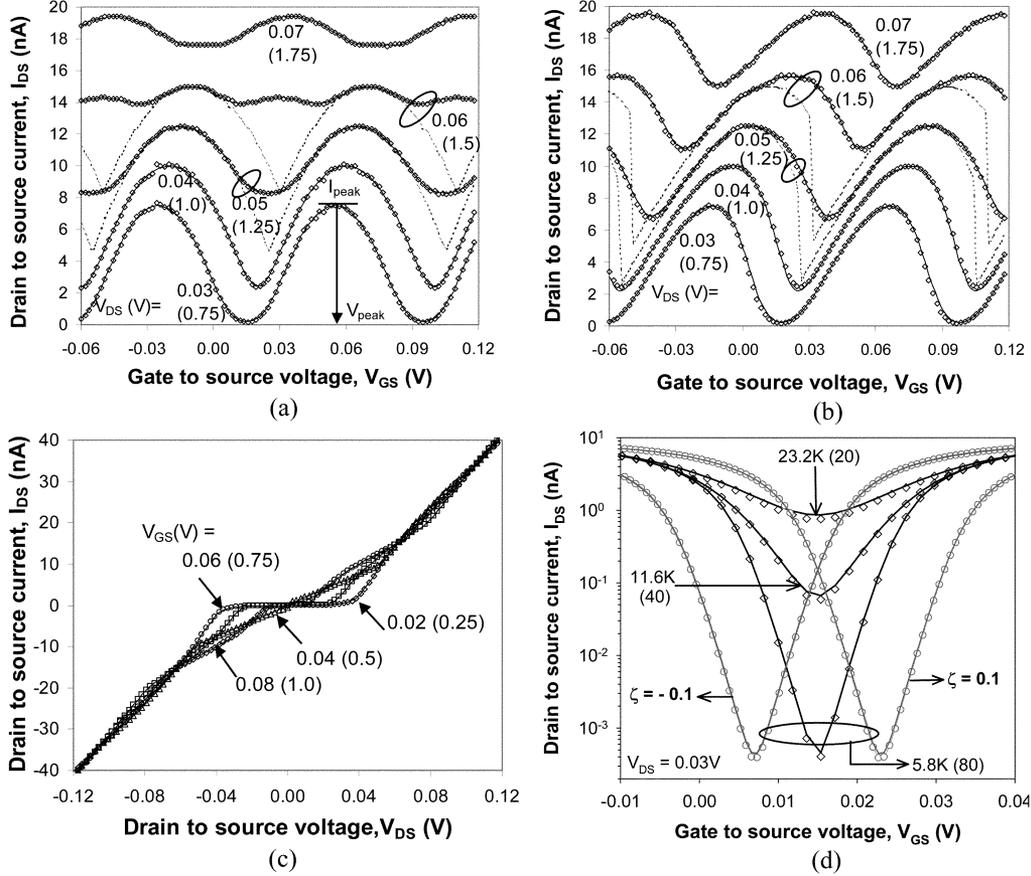


Fig. 3. Verification of MIB model for the $I_{DS}-V_{GS}$ characteristics for (a) symmetric SET ($R_D = R_S = 1 \text{ M}\Omega$) and (b) asymmetric SET ($R_D = 0.382 \text{ M}\Omega$, $R_S = 1.91 \text{ M}\Omega$) with the same device capacitances as Fig. 1 at different values of V_{DS} at $T = 15 \text{ K}$. Here the numbers within brackets represent the $V_{DS}/(e/C_\Sigma)$ factor. (c) Verification of MIB model for the $I_{DS}-V_{DS}$ characteristics of the symmetric device at different V_{GS} at $T = 15 \text{ K}$, where the numbers within brackets represent the $V_{GS}/(e/C_G)$ factor. (d) Validation of MIB model at different temperature levels for symmetric device, where the numbers within brackets represent the $(e^2/C_\Sigma)/k_B T$ factor. (d) also shows the effect of background charge on device characteristics. In these figures symbols denote the Monte Carlo simulation (SIMON) and solid line represents the proposed MIB model and dotted line represents the older version of the MIB model [i.e., without $|V_{DS}| > e/C_\Sigma$ extension as expressed by (9)].

the drain current. This shifting of this drain current window can be done in the following way:

$$\text{if } \lambda V_{\text{island}} > (2\alpha + \lambda V_{DS}/2)$$

$$V_{\text{island}} \leftarrow V_{\text{island}} - 2\lambda\alpha \left(1 + \left[\frac{|V_{\text{island}} - 2\alpha - \frac{\lambda V_{DS}}{2}|}{2\alpha} \right] \right) \quad (3a)$$

$$\text{if } \lambda V_{\text{island}} < \lambda V_{DS}/2$$

$$V_{\text{island}} \leftarrow V_{\text{island}} + 2\lambda\alpha \left(1 + \left[\frac{|V_{\text{island}} - \frac{V_{DS}}{2}|}{2\alpha} \right] \right). \quad (3b)$$

Here λ holds the sign of V_{DS} and the *box function*, $[x]$, returns the greatest integer less than or equals to x .

3) *Calculation of the Drain Current*: We have developed our MIB model by solving the steady-state master equation for single electron tunneling [10]. The state transition diagram for the electron tunneling in a SET device is demonstrated in Fig. 2(b) and (c). In this paper, for a given bias condition, only the two most probable number of electrons are taken into account, i.e., the number of electrons in the island could be 0

or 1 (or 1 or 2, or -1 or 0). Now solving master equation for “ $0 \leftrightarrow 1$,” “ $1 \leftrightarrow 2$,” “ $-1 \leftrightarrow 0$ ” state transition, one gets

$$p_1 = \frac{\vec{\Gamma}_S(0) + \overleftarrow{\Gamma}_D(0)}{\vec{\Gamma}_S(1) + \overleftarrow{\Gamma}_D(1)} p_0 \quad (4a)$$

$$p_2 = \frac{\vec{\Gamma}_S(1) + \overleftarrow{\Gamma}_D(1)}{\vec{\Gamma}_D(2)} \times \frac{\vec{\Gamma}_S(0) + \overleftarrow{\Gamma}_D(0)}{\vec{\Gamma}_S(1) + \overleftarrow{\Gamma}_D(1)} p_0 \quad (4b)$$

$$p_{-1} = \frac{\overleftarrow{\Gamma}_S(0) + \vec{\Gamma}_D(0)}{\overleftarrow{\Gamma}_S(-1)} p_0 \quad (4c)$$

where p_n is the probability of finding n electrons in the island and $\vec{\Gamma}$ is the electron tunneling rate as described in Fig. 2(b). Now using the fact that $\sum_n p_n = 1$, we can derive the model for SET drain current as [10]: see (5), shown at the bottom of the next page.

Now, considering one directional electron flow (i.e., assuming $\vec{\Gamma}_S, \vec{\Gamma}_D \gg \overleftarrow{\Gamma}_S, \overleftarrow{\Gamma}_D$) and replacing the tunneling rates with tunneling current (i.e., $I_S(n) = e \vec{\Gamma}_S(n)$,

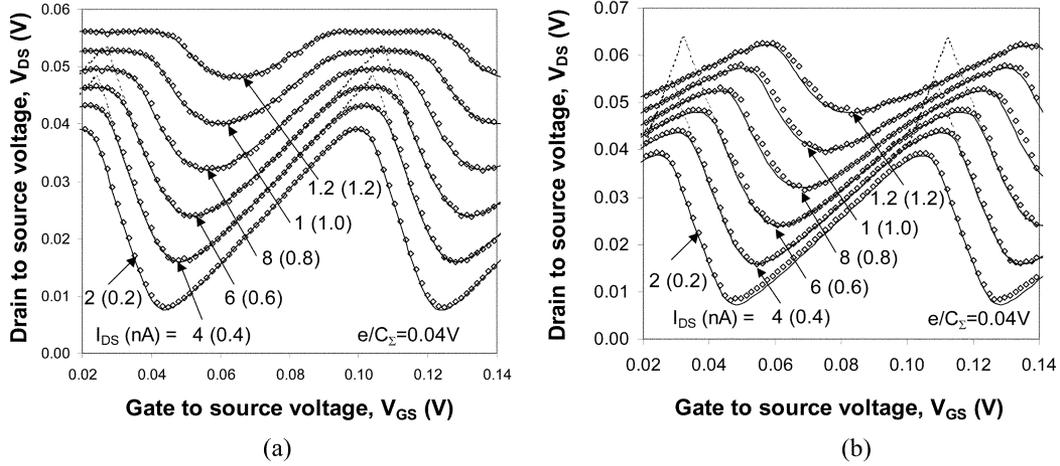


Fig. 4. $V_{DS}-V_{GS}$ characteristics of a constant current biased SET for (a) symmetric (b) asymmetric devices as simulated by the proposed MIB (solid line), older version of MIB (dotted line) and MC simulations (symbols) at $T = 15$ K. Here, we have used the same device parameters as in Fig. 3. The values within the third brackets represent the $I_{DS}/\{e/C_{\Sigma}(\sqrt{R_S} + \sqrt{R_D})^2\}$ factor.

$I_D(n) = e \vec{\Gamma}_D(n)$ the *final expression* for the drain current in our MIB model becomes

$$I_{DS} = \lambda \frac{I_S(0)I_D(1) + I_S(0)I_S(1) + I_D(1)I_D(0)}{I_S(0) + I_D(1) + \frac{I_S(0)I_S(1)}{I_D(2)} + \frac{I_D(1)I_D(0)}{I_S(-1)}} \quad (6)$$

$$\text{where } I_S(n) = \frac{\lambda V_{\text{island}} - (2n+1)\alpha}{\left(1 - \exp\left(-\frac{\lambda V_{\text{island}} - (2n+1)\alpha}{V_T}\right)\right) R_D} \quad (7)$$

$$\text{and } I_D(n) = \frac{\lambda V_{DS} - \lambda V_{\text{island}} + (2n-1)\alpha}{\left(1 - \exp\left(-\frac{\lambda V_{DS} - \lambda V_{\text{island}} + (2n-1)\alpha}{V_T}\right)\right) R_S} \quad (8)$$

and V_T is the thermal voltage ($k_B T/e$, k_B is the Boltzmann constant). The effect of this “one directional electron flow” assumption will be discussed in Section IV-A. It should be noted that as we have considered maximum 2 and minimum -1 number of electrons in the island, therefore the proposed model is valid for $|V_{DS}| \leq 3e/C_{\Sigma}$. By considering only “ $0 \leftrightarrow 1$ ” state transitions, we can further reduce (6) for $|V_{DS}| \leq e/C_{\Sigma}$ as follows:

$$I_{DS} = \lambda \frac{I_S(0)I_D(1)}{I_S(0) + I_D(1)} \quad (9)$$

which, shows that the device current is the half of the harmonic mean of the drain and source tunneling currents [5], [8], [21].

C. Model Verification

The proposed model has been verified against simulations from the widely accepted Monte Carlo (MC) simulator SIMON [10]. Different SET device characteristics ($I_{DS}-V_{GS}$, $I_{DS}-V_{DS}$, effect of the temperature and background charge) have been simulated and compared with Monte Carlo simulation as demonstrated in Fig. 3. Fig. 4 reveals the accuracy of our model to predict the $V_{DS}-V_{GS}$ characteristics of a constant current biased symmetric and asymmetric SET device, which is extremely important for analog SET/hybrid CMOS-SET IC design. It should be noted that the MC simulators are usually extremely time consuming when the simulation involves 1) high-temperature operation, 2) current-biased SET 3) any resistance is present in a SET-based circuit, in comparison, the proposed MIB model takes only a fraction of a second to simulate the same with similar accuracy.

III. PARAMETER EXTRACTION

In contrast with CMOS, there is no fixed, unified technology for SET fabrication. SET can be fabricated by metal (Al, Au),

$$\begin{aligned} I_{DS} &= e \sum_{n=-1,0,1} p_n \left(\vec{\Gamma}_S(n) - \vec{\Gamma}_S(n) \right) = e \left\{ p_{-1} \vec{\Gamma}_S(-1) + p_0 (\vec{\Gamma}_S(0) - \vec{\Gamma}_S(0)) + p_1 (\vec{\Gamma}_S(1) - \vec{\Gamma}_S(1)) \right\} \\ &= e \frac{\left(\vec{\Gamma}_S(0) - \vec{\Gamma}_S(0) \right) \left(\vec{\Gamma}_S(1) + \vec{\Gamma}_D(1) \right) + \left(\vec{\Gamma}_S(1) - \vec{\Gamma}_S(1) \right) \left(\vec{\Gamma}_S(0) + \vec{\Gamma}_D(0) \right) + \left(\vec{\Gamma}_S(1) + \vec{\Gamma}_D(1) \right) \left(\vec{\Gamma}_S(0) + \vec{\Gamma}_D(0) \right)}{\left(\vec{\Gamma}_S(1) + \vec{\Gamma}_D(1) \right) + \left(\vec{\Gamma}_S(0) + \vec{\Gamma}_D(0) \right) + \frac{\left(\vec{\Gamma}_S(1) + \vec{\Gamma}_D(1) \right) \left(\vec{\Gamma}_S(0) + \vec{\Gamma}_D(0) \right)}{\vec{\Gamma}_D(2)} + \frac{\left(\vec{\Gamma}_S(0) + \vec{\Gamma}_D(0) \right) \left(\vec{\Gamma}_S(1) + \vec{\Gamma}_D(1) \right)}{\vec{\Gamma}_S(-1)}} \end{aligned} \quad (5)$$

TABLE I
DIFFERENT MIB MODEL PARAMETER EXTRACTED BY THE PROPOSED PARAMETER EXTRACTION PROCEDURE AT $T = 10$ K AND AT $T = 20$ K

	Original	Results of extraction at 10K	Results of extraction at 20K
R_S	5M Ω	4.895M Ω	4.540M Ω
R_D	2M Ω	2.047M Ω	2.275M Ω
C_G	1.1aF	1.105aF	1.111aF
C_{G2}	0.9aF	0.9171aF	0.8933aF
C_{TD}	0.8aF	0.8155aF	0.8656aF
C_{TS}	1.2aF	1.271aF	1.406aF
ζ_{eff}	0.5	0.5005	0.5032

Silicon (or silicon on insulator), III–V material, and even by carbon nanotubes [10]. However, if the values of the device capacitances and resistances are known, MIB model can predict the device behavior of a SET irrespective of its technology (geometry of islands and tunneling junctions), as it is physically founded in terms of effective electrical parameters (device capacitances and resistances). Therefore, the proposed model is technology independent and hence it requires an accurate parameter extraction procedure. The extraction procedure of MIB model parameters (C_G , C_{G2} , C_{TS} , C_{TD} , R_D , R_S , and ζ), which is based on the assumption that the second gate is grounded, is described below:

Step 1: Record a set of I_{DS} versus V_{GS} characteristics for different values of positive V_{DS} . The period of oscillations (e/C_G) in the measured I_{DS} – V_{GS} characteristics gives us the value of the gate capacitance (C_G). Now, the maximum value of $I_{DS}(= I_{\text{peak}})$ at any particular V_{DS} and the corresponding value of $V_{GS}(= V_{\text{peak}})$ [Fig. 3(a)] can be expressed as [5]

$$I_{\text{peak}} = \frac{V_{DS}}{(\sqrt{R_S} + \sqrt{R_D})^2} \quad (10)$$

$$V_{\text{peak}} = \left(\zeta_{\text{eff}} + k + \frac{1}{2} \right) \frac{e}{C_G} + \frac{C_{\Sigma}}{C_G} \left\{ \frac{\sqrt{R_S}}{\sqrt{R_S} + \sqrt{R_D}} - \frac{C_{TD}}{C_{\Sigma}} \right\} V_{DS} \quad (11)$$

where ζ_{eff} is the effective (signed fractional part of ζ) fixed background charge of the device and k is an integer number.

Equation (11) suggests that the plot of V_{peak} versus V_{DS} is a set of parallel straight lines (for different k) and the intercept with the vertical axis can be used to extract ζ_{eff} . Please note that, if the slope of (11) is found to be too small to measure then one can switch the drain and source terminal and perform the same procedure again.

Step 2: Bias the SET with a constant current source [$I_{\text{BIAS}} < e / \{10C_{\Sigma}(\sqrt{R_D} + \sqrt{R_S})^2\}$], and record a set of quasi-triangular V_{GS} – V_{DS} characteristics. The slopes of these characteristics could be formulated as

$$1) \text{ Slope (rise) : } K_1 = \frac{C_G}{C_{TS} + C_G + C_{G2}} \quad (12)$$

$$2) \text{ Slope (fall) : } K_2 = -\frac{C_G}{C_{TD}}. \quad (13)$$

If similar characteristics are then recorded by exchanging the drain and source terminals of the SET, one can have another set of equations for the slopes of V_{GD} – V_{SD} characteristics

$$1) \text{ Slope (rise) : } K_3 = \frac{C_G}{C_{TD} + C_G + C_{G2}} \quad (14)$$

$$2) \text{ Slope (fall) : } K_4 = -\frac{C_G}{C_{TS}}. \quad (15)$$

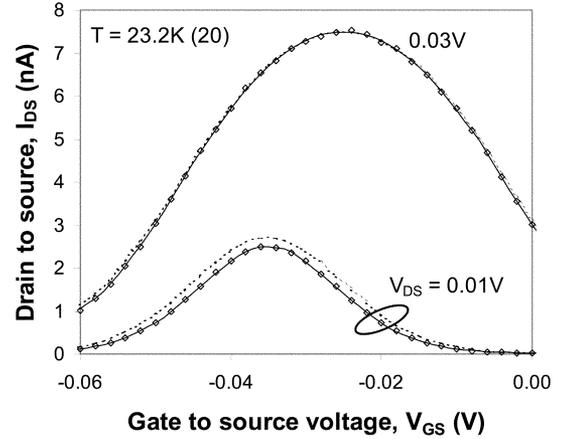


Fig. 5. Effect of the “unidirectional electron flow” approximation on the MIB model. Here the symbols represents Monte Carlo simulation, dotted and solid line represents MIB model with “unidirectional electron flow” approximation (6) and without approximation (16), respectively.

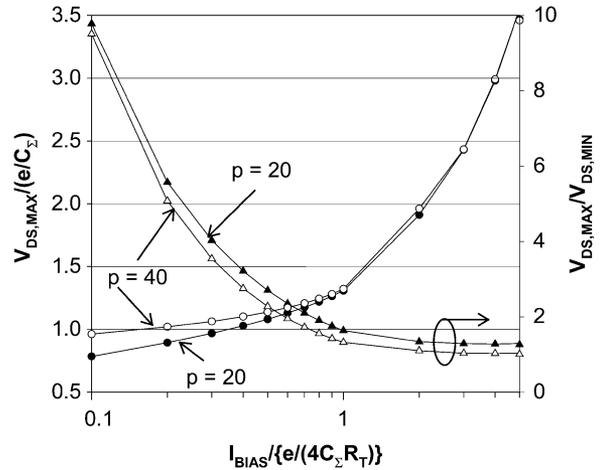


Fig. 6. Effect of the bias current on the constant current based SET analog architectures (here $R_T = R_D = R_S$ and $p = (e^2/C_{\Sigma})/k_B T$), where the symbols denotes the MC simulation and solid line represents the proposed MIB model.

Using (12)–(15) one can extract all the device capacitances by using the already extracted value of C_G and the value of the tunnel junction resistances (R_D and R_S) can be easily extracted by using those device capacitances values in (10) and (11).

Proposed model and extraction procedure have been validated using a self-consistent approach: a set of realistic model parameters are used as inputs to the MC simulator (SIMON) and the SET is simulated, following which, the parameters can be estimated by applying the proposed extraction procedure to the

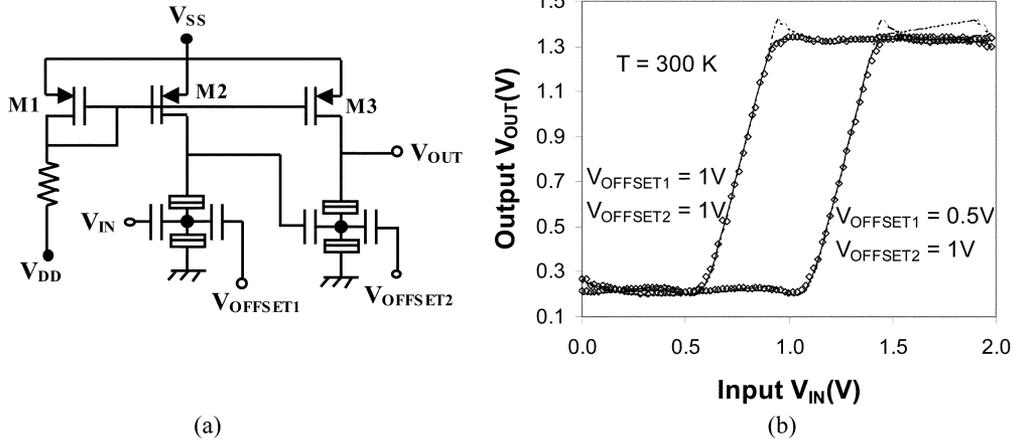


Fig. 7. (a) Schematic and (b) characteristics of a basic CMOS-SET hybrid neuron cell (with $C_G = C_{G2} = 0.04$ aF, $C_{TD} = C_{TS} = 0.02$ aF, $R_D = R_S = 1$ M Ω) as predicted by SIMON (symbol) and SMARTSPICE (solid and dotted line). It should be noted that I_{BIAS} is taken to be 50 nA for SIMON simulation and for SMARTSPICE simulation the MOS current source is designed in such a way that it can drive the same bias current through the SET. Here the pMOSFET parameters are $L = 0.5$ μ m, $W = 0.8$ μ m, $T_{OX} = 9.74$ nm, $V_{TH} = -0.55$ and EKV [24] MOSFET model is used. The dotted line represents MIB model without the $|V_{DS}| > e/C_{\Sigma}$ extension.

simulated characteristics. It should also be noted that the proposed parameter extraction procedure is temperature dependent as given in Table I and hence it is recommended to perform all the measurement at low temperatures [$T < e^2/(40k_B C_{\Sigma})$].

Please note that, the reported extraction procedure is based on elementary SET characteristics and independent of MIB model complexities [5], [18] and also valid for any other SET models [17], [19], [20], which use only device capacitances, resistances and background charge as model parameters.

IV. DISCUSSION

A. Effect of the “Unidirectional Electron Tunneling” Approximation

The MIB model proposed in this work [expressed by (6)], is based on the approximation that the electron tunneling rate toward the positive potential (i.e., from source-to-island-to-drain for positive V_{DS} and drain-to-island-to-source for negative V_{DS}) is much higher than the electron tunneling rate in the opposite direction. By considering the bi-directional electron flows, from (5), the MIB model for SET drain current can be formulated as (16)–(18), shown at the bottom of the next page. It should be noted that (6) and (16) contains six and ten different exponential terms respectively. The differences between the two approaches [(6) and (16)] are demonstrated in Fig. 5. The “bi-directional electron tunneling” approach only improves the model accuracy at low drain voltage at high temperatures, and at

the same time introduces many exponential terms, which makes the simulations time consuming (the “unidirectional tunneling approach” overestimates the drain current by 9.24% at $V_{DS} = 0.01$ V for the SET parameters $C_G = 2$ aF, $C_{TD} = C_{TS} = 1$ aF, $R_D = R_S = 1$ M Ω). We have found that in a Pentium III 1200MHz CPU, (16) consumes 22% more processing time than (6) to simulate the characteristics of a current biased SET.

B. Effect of the Bias Current on CMOS-SET Hybrid Circuit Design

Fig. 6 demonstrates the relation between the bias current and the output voltage (V_{DS}) of a constant current biased SET. As the bias current increases: 1) $V_{DS,MAX}$ increases, 2) the dynamic range of the V_{DS} variation decreases, and 3) influence of the temperature on the output voltage decreases. Therefore, for SET/ hybrid CMOS-SET analog IC design, in order to optimize the tradeoff between the $V_{DS,MAX}$ and the dynamic range of the V_{DS} variation, the bias current should be less than $0.5I_{BIAS}/\{e/(4C_{\Sigma}R_T)\}$.

V. CMOS-SET HYBRID CIRCUIT SIMULATION

In this work, circuit level CMOS-SET cosimulations have been successfully performed by implementing the proposed MIB model in commercial circuit simulator SMARTSPICE by its Verilog-A interface [22], [23]. Verilog-A [23] is an Analog

$$I_{DS} = \lambda \frac{(I_S(0) - i_S(0))(i_S(1) + I_D(1)) + (I_S(1) - i_S(1))(I_S(0) + i_D(0)) + (i_S(1) + I_D(1))(i_S(0) + I_D(0))}{(i_S(1) + I_D(1)) + (I_S(0) + i_D(0)) + \frac{(I_S(1) + i_D(1))(I_S(0) + i_D(0))}{I_D(2)} + \frac{(i_S(1) + I_D(1))(i_S(0) + I_D(0))}{I_S(-1)}} \quad (16)$$

$$\text{where, } i_S(n) = e \overleftarrow{\Gamma}_S(n) = \frac{-\lambda V_{\text{island}} + (2n-1)\alpha}{\left(1 - \exp\left(-\frac{-\lambda V_{\text{island}} + (2n-1)\alpha}{V_T}\right)\right)} R_S \quad (17)$$

$$\text{and, } i_D(n) = e \overleftarrow{\Gamma}_D(n) = \frac{-\lambda V_{DS} + \lambda V_{\text{island}} - (2n+1)\alpha}{\left(1 - \exp\left(-\frac{-\lambda V_{DS} + \lambda V_{\text{island}} - (2n+1)\alpha}{V_T}\right)\right)} R_D \quad (18)$$

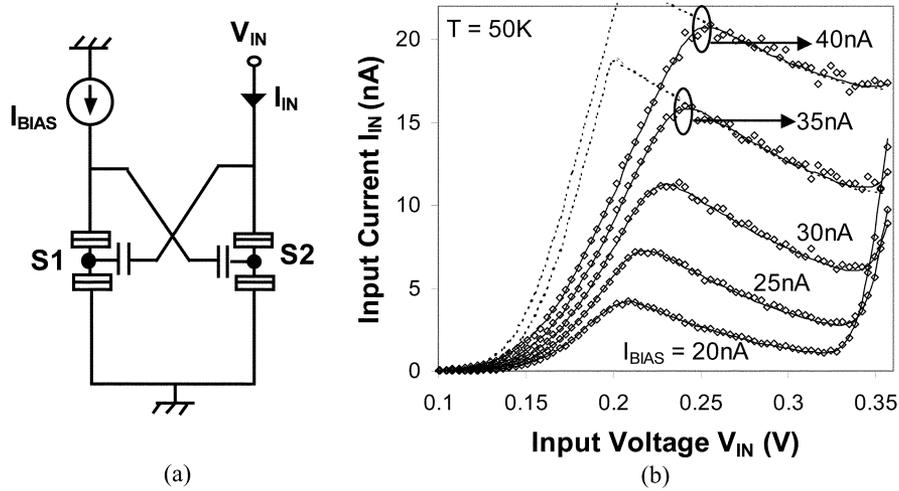


Fig. 8. (a) Schematic and (b) characteristics of NDR device for different bias current (I_{BIAS}) as simulated by SIMON (symbol) and MIB (solid and dotted line) with the device parameters are: $C_G = 0.2$ aF, $C_T = 0.15$ aF, $R_D = R_S = 1$ M Ω for S1 and $C_G = C_T = 0.15$ aF, $R_D = R_S = 1$ M Ω for S2. The dotted line represents MIB simulation without $|V_{DS}| > e/C_{\Sigma}$ extension.

High Level Hardware Description Language (AHDL) for analog systems in which one can mix SMARTSPICE device models (such as EKV [24], BSIM [25], etc.) and Verilog-A modules in the same netlist. Analog SET and CMOS-SET co-simulations have been successfully carried out for different benchmarked circuit as discussed in Sections V-A–D.

A. Neural Network Circuit

Since a powerful signal processor demands a large neural network, therefore, due to the power dissipation and size of the neural chip, it is difficult to design efficient neural network by CMOS technology. However, one can exploit the ultra low power dissipation of SET devices and its nano feature size in order to realize compact neural device. A SET-based neural network scheme (composed of two-cascaded current biased SET), as proposed by Goossen's [8] is depicted in Fig. 7(a). For the proper operation of the circuit, the drain and source tunnel capacitances of the SET have to be equal ($C_{TD} = C_{TS}$) and gate capacitances have to be twice of that ($C_G = C_{G2} = 2C_{TD}$) [8]. One point should be noted that in order to drive currents of the order of nA through the SET one has to bias the MOS transistors in subthreshold (weak inversion) region. Using SMARTSPICE, the static characteristics of the neuron cell, has been simulated accurately and good agreement with MC simulation Fig. 7(b) demonstrates the accuracy of the proposed model.

B. NDR Circuit

A negative differential resistance (NDR) is a useful element with a wide variety of circuit applications such as in oscillators, amplifiers, logic cell, and memory. Fig. 8 depicts an alternative architecture of SET-based NDR cell [16], which is composed of two cross-connected SET (S1 and S2) and a current source. The current–voltage I – V characteristics of this NDR cell and the effect of the bias current on the circuit behavior are shown in Fig. 8. The input voltage (V_{IN}) and the constant current biased first SET (S1) creates a feedback loop that helps to decrease the gate-to-source voltage of second SET (S2) for a certain range of increasing V_{IN} , and which follows a decrease in the drain current (or the input current, I_{IN}) of S2 (NDR effect). It is found that

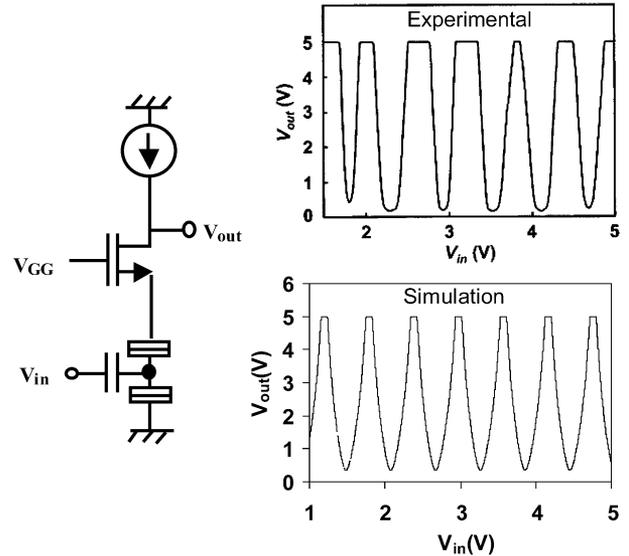


Fig. 9. Schematic of the universal literal gate comprising a SET and a MOSFET and comparison between measured and simulated V_{in} – V_{out} characteristics of the universal literal gate at $T = 27$ K. The SET device parameters are $C_G = 0.27$ aF, $C_{TD} = C_{TS} = 2.7$ aF, $R_D = R_S = 200$ k Ω and MOS device parameters are $W = 12$ μ m, $L = 14$ μ m, $T_{ox} = 90$ nm, $V_{TH} = 0.64$ V. V_{GG} is set to 1.08 V, and V_{out} is hard-limited at 5 V [6]. EKV [24] model is used to simulate the MOS device. Experimental data are reproduced after [6] at the end.

this NDR architecture appears more versatile than previously reported structure [26] in terms of dynamic range of NDR region, current controllability and drivability, and offers a very effective solution for real implementation of the NDR functionality.

C. Multiple-Valued Logic (MVL) Circuit

Multiple-valued logics (MVL) have potential advantages over binary logics with respect to the number of elements per function and operating speed. Most MVL circuits, been fabricated with MOS and bipolar devices, have limited success partially because the devices are inherently single-threshold or single-peak, and are not fully suited for MVL. Inokawa *et al.* [6] have recently proposed a hybrid CMOS-SET MVL circuit

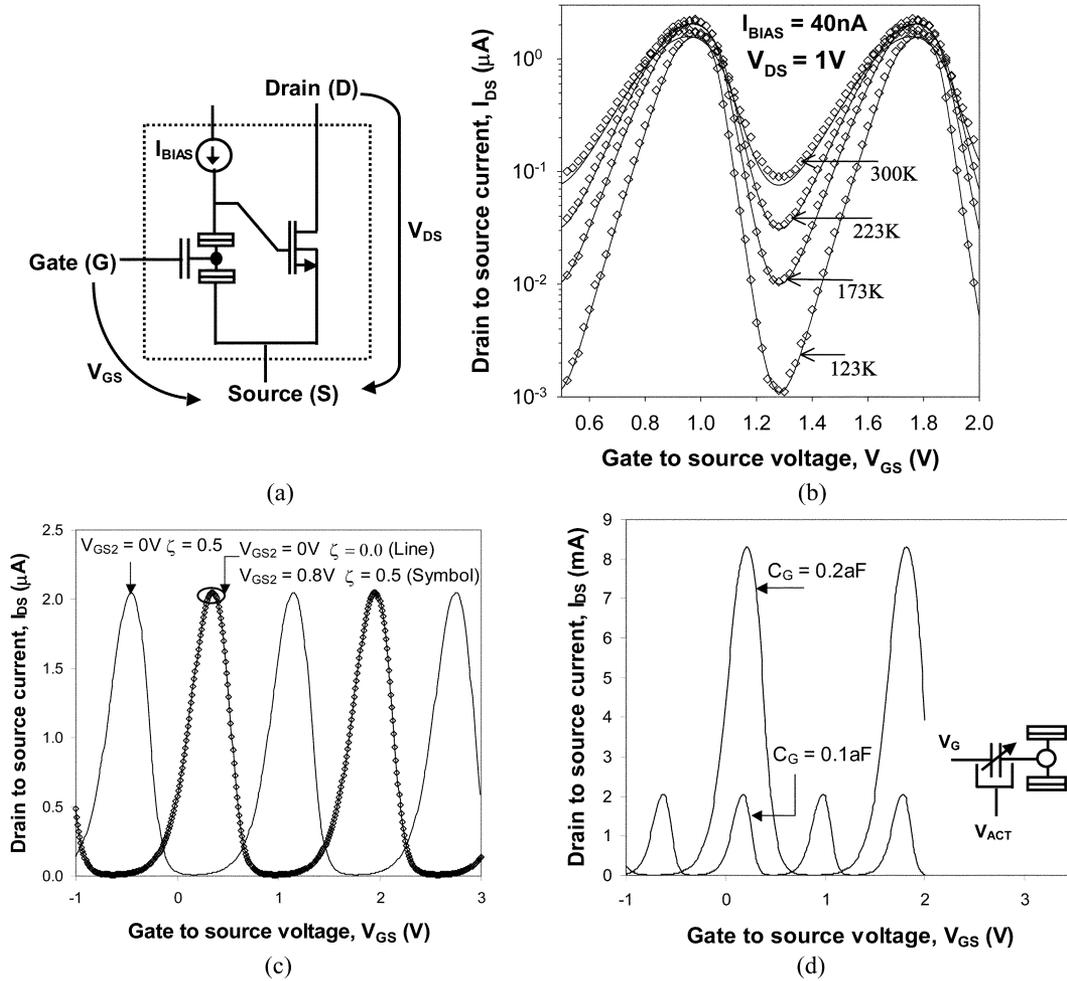


Fig. 10. (a) Schematic of the SETMOS device and (b) its characteristics as predicted by SMARTSPICE (solid line) at different temperatures for the SET device parameters: $C_G = 0.2$ aF, $C_{TD} = C_{TS} = 0.15$ aF, $R_{TD} = R_{TS} = 1$ M Ω . The MOSFET parameters are $L = 65$ nm, $W = 100$ nm, $V_{TH} = 0.32$ V, $T_{ox} = 1.7$ nm respectively. The result obtained from simulating the SET device by SIMON and MOSFET device by SMARTSPICE separately is denoted by the symbols. We have used 65-nm node calibrated BSIM [25] model to simulate the MOS devices. (c) Effect of background charge on a double gate SETMOS device with $C_G = C_{G2} = 0.1$ aF and (d) characteristics of a tunable gate NEMS-SETMOS device at $V_{DS} = 1$ V and $T = 173$ K.

for practical application (e.g., quantizer for digital communication system). Fig. 9 shows the schematic of a hybrid CMOS-SET universal literal gate that acts as a MVL cell. The simulated V_{in} - V_{out} characteristics of this circuit is demonstrated in Fig. 9, which shows good resemblance with the measured data, as presented in [6].

D. SETMOS Device

SETMOS [7] is a true novel hybrid CMOS-SET architecture, that is able to extend the Coulomb blockade oscillations of a SET transistor into the μ A current range in the subambient temperature (-150 $^{\circ}$ C up to -100 $^{\circ}$ C) regime, corresponding to near subthreshold operation region of a nanometer-scale MOSFET. The SETMOS Coulomb blockade oscillation period (e/C_G) is dictated by SET gate capacitance and its input voltage and is of the same order of magnitude. The schematic of the SETMOS device is presented in Fig. 10(a). The characteristics of the SETMOS device, as simulated by SMARTSPICE, for a wide range of temperature variation are demonstrated in Fig. 10(b), and a close agreement with MC simulation has been observed. This unique device can be converted into a NDR behavior, whose NDR characteristic is a quasi-periodic

function of the input voltage [7]. Fig. 10(c) demonstrates the shift of SETMOS characteristics due to background charge effect. It also shows how using an appropriate bias at the second gate of the SET could restore the original characteristics. Fig. 10(d) reveals a concept of using tunable NEMS gate SET in order to extend the functionalities of the SETMOS device. The gate capacitance can be switched between two values by tuning the V_{ACT} [7], which enables us to change the output current level and also the periodicity. Such architectures can be used to build background charge independent SET based communication system where signal would be coded in the periodicity instead of its amplitude. Fig. 10(d) also shows that the proposed model enables us to cosimulate SET with other types of devices, e.g., variable MEMS/NEMS capacitors that could add new attributes to conventional SET as tunable gate capacitances.

VI. CONCLUSION

A new version of the MIB model for SET devices has been reported, which is specially intended for analog CMOS-SET operation. In this work, the earlier version of MIB model is

extended to $|V_{DS}| > e/C_{\Sigma}$ (up to $3e/C_{\Sigma}$), which is essential for analog SET operation. The proposed model has been verified at the device level for both symmetric and asymmetric devices and a good agreement with Monte Carlo simulation is found. MIB is then implemented in the professional circuit simulator SMARTSPICE using its AHDL interface in order to co-simulate the SET devices along with CMOS devices. A series of simulations is then successfully performed for different benchmarked CMOS-SET hybrid architecture. MIB has some clear advantages: 1) it is physically based, and able to accurately describe the drain current for symmetric and asymmetric, single/double gate device up to $T = e^2/(10k_B C_{\Sigma})$ 2) it is simple (carries less exponential terms than other models) yet able to predict device behavior accurately up to $|V_{DS}| = 3e/C_{\Sigma}$. Finally, the model is shown to be very accurate for the simulation, design, and verification of both digital and analog hybrid CMOS-SET circuit architectures.

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