Accurate Analysis of On-Chip Inductance Effects and Implications for Optimal Repeater Insertion and Technology Scaling

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Abstract

This paper introduces an accurate analysis of on-chip inductance effects for distributed *RLC* interconnects that takes the effect of both the series resistance and the output parasitic capacitance of the driver into account. Using rigorous first principle calculations, accurate expressions for the transfer function of these lines and their time-domain response have been presented for the first time. Furthermore, an optimal repeater insertion scheme for distributed *RLC* interconnects is also presented using a novel performance optimization methodology. Additionally, the impact of line inductance on interconnect performance has been analyzed in detail with especial regards to technology scaling based on the International Technology Roadmap for Semiconductors (ITRS). Contrary to conventional wisdom, it is shown that the effect of line inductance on optimized interconnect performance will actually diminish for *scaled* global interconnects.

Introduction

For deep submicron technologies on-chip inductive effects arising due to increasing clock speeds, decreasing signal rise times and increasing length of on-chip interconnects are a concern for signal integrity and overall chip performance [1]. Inductance can increase the interconnect delay per unit length and can cause ringing in the signal waveforms, which can adversely affect signal integrity. Furthermore, inductance effects in global interconnects are more severe due to the lower resistance per unit length of these lines, which results in the reactive component of the interconnect impedance to become comparable to the resistive component, and also due to the presence of significant mutual inductive coupling between interconnects resulting from longer current return paths. With the introduction of Copper based interconnect technologies, line resistances have decreased further and as a result, inductive effects are expected to become more significant. Accurate analysis of inductance is therefore critical for predicting the performance of global interconnects, which in turn are known to determine the chip performance. Also, accuracy of the inductance analysis is important for the precise quantification of their impact on performance optimization. Furthermore, it is of utmost importance to understand the degree by which future deep submicron technologies would be impacted by interconnect inductance effects.

In this paper, the transfer function and the time-domain response of a realistic driver-interconnect-load configuration have been presented for the first time based on a rigorous analysis of the distributed structure. It is shown that the series resistance and output parasitic capacitance of the driver have a significant impact on the waveform and delay and must be included for accurate analysis of realistic distributed *RLC* lines. Based on the new delay model a novel interconnect performance optimization is presented and their implications for optimal repeater insertion and technology scaling have been quantified.

Time-Domain Response of an *RLC* Interconnect Segment

Consider a uniform line with resistance, capacitance and inductance per unit length of r, c and l respectively, driven by a repeater of series resistance R_S and output parasitic capacitance C_P, and driving an identical repeater with load capacitance C_L (Figure 1). For a given technology, let the output resistance, output parasitic capacitance and input capacitance of a minimum sized repeater be r_s, c_p and c_0 respectively. Therefore if the repeater size is k times the size of a minimum sized repeater, $R_S = r_s/k$, $C_P = c_p k$ and $C_L = c_0 k$. For this analysis it is assumed that the repeater resistance and output parasitic capacitance is linear throughout the output voltage transition range. Using the ABCD parameters of a uniform distributed *RLC* line, it can be shown that the input-output transfer function is given by[1]

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{1}{[1+sR_S(C_P+C_L)]\cosh(\theta)+\left[\frac{R_S}{Z_0}+sC_LZ_0+s^2R_SC_PC_LZ_0\right]\sinh(\theta)} \quad (1)$$

where $Z_0 = \sqrt{\frac{r+sl}{sc}}$, $\theta = \sqrt{(r+sl)sc}h$, h is the length of the interconnect segment as shown in Figure 1 and s is the complex frequency ($j\omega$).

The step-response of this system is given by $V_o(s) = \frac{1}{s}H(s)$ in the Laplace domain. However, computing the response in the time-domain is analytically intractable. Kahng and Muddu [2] suggested using a second-order expansion of the transfer function[2] in order to compute the two-pole, time-domain response of the following form

$$v_o(t) = V_0[1 + a_1\exp(s_1t) + a_2\exp(s_2t)]$$

for appropriate s_is and a_is. Some fitting parameters were introduced in [3] to modify a_is and s_is in the above expression in order to get better matching with SPICE output.

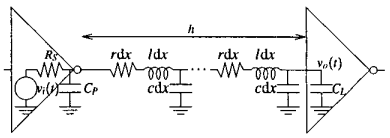

Fig. 1. Equivalent circuit of a driver-interconnect-load segment.

A rigorous time-domain expression for the output of a distributed *RLC* interconnect with a driver of arbitrary *series* impedance is derived in [4, 5, 6, 7] *without* explicitly requiring the computation of the Laplace-domain transfer function. However, for a practical driver, the capacitance from output to ground cannot be modelled as a series impedance, and therefore the expression that they derived cannot be easily adapted for a realistic scenario. Moreover, their delay expression involves Bessel functions and cannot be easily used for driver and interconnect optimization for delay minimization which we present later on.

Recall that a lumped *RLC* circuit with one inductance and one capacitance has a two-pole transfer function. Therefore the two pole approximation effectively ignores the distributed nature of the *RLC* interconnect. Therefore for better accuracy, higher order terms also need to be considered. In this work, we consider a fourth-order Padé approximation of (1), i.e.,

$$H(s) \approx \frac{1}{1+sb_1+s^2b_2+s^3b_3+s^4b_4}$$

where

$$b_1 = R_S(C_P+C_L)+\frac{rch^2}{2!}+R_Sch+C_Lrh$$

$$b_2 = \frac{lch^2}{2!}+\frac{r^2c^2h^4}{4!}+R_S(C_P+C_L)\frac{rch^2}{2!}+(R_Sch+C_Lrh)\frac{rch^2}{3!}+(C_Llh+R_SC_PC_Lrh)$$

$$b_3 = \frac{c^3r^3h^6}{6!}+\frac{2c^2rlh^4}{4!}+R_S(C_P+C_L)\left[\frac{lch^2}{2!}+\frac{r^2c^2h^4}{4!}\right]+(R_Sch+C_Lrh)\left[\frac{lch^2}{3!}+\frac{r^2c^2h^4}{5!}\right]$$
$$+(C_Llh+R_SC_PC_Lrh)\frac{rch^2}{3!}+R_SC_PC_Llh$$

$$b_4 = \frac{c^2l^2h^4}{4!}+\frac{3c^3r^2lh^6}{6!}+\frac{c^4r^4h^8}{8!}+R_S(C_P+C_L)\left[\frac{c^3r^3h^6}{6!}+\frac{2c^2rlh^4}{4!}\right]+(R_Sch+C_Lrh)\left[\frac{c^3r^3h^6}{7!}+\frac{2c^2rlh^4}{5!}\right]$$
$$+(C_Llh+R_SC_PC_Lrh)\left[\frac{lch^2}{3!}+\frac{r^2c^2h^4}{5!}\right]+\frac{R_SC_PC_Lrch^3}{3!}$$

The step-response can be calculated as

$$v_o(t) = V_0\left[1 + d_1\exp(s_1t) + d_2\exp(s_2t) + d_3\exp(s_3t) + d_4\exp(s_4t)\right]$$

for appropriate residues (d_is) and poles (s_is).

Figure 2 compares the output voltage of the interconnect system in Figure 1 for a 3.3 mm long, minimum width metal 6 line for 180 nm technology node with $r = 36281\ \Omega$/m, $c = 269$ pF/m, $l = 4\ \mu$H/m, which is driven by an inverter which is 174 times larger than the minimum sized inverter in that technology using a second, third and fourth order approximation of (1). Note that output waveforms of these three approximations are significantly different and will lead to different time delays. In Figure 2, it can be noticed that the 60% delay is identical for the three cases. However this is true only for the specific combination of parameters chosen in this example and is not true for any other combination. It should also be noted that the delay is not a smooth function

[1] derivation omitted for brevity

[2] their driver-interconnect configuration did not include C_P and included a driver inductance L_S in series with R_S

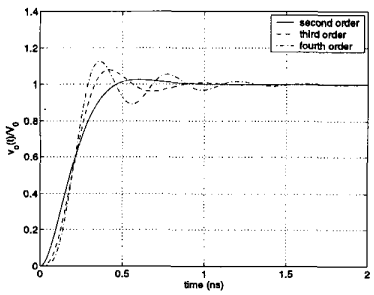

Fig. 2. Second, third and fourth order response of the driver and interconnect structure of Figure 1.

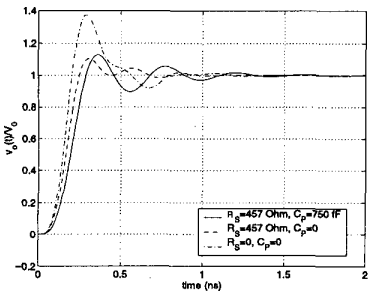

Fig. 3. Step-response of the driver and interconnect structure for three cases (1) R_S and C_P the same as in Figure 2, (2) $C_P = 0$ (3) $C_P = 0$ and $R_S = 0$. Other parameters are same as for Figure 2.

of l for a fourth order response. Therefore if a fourth order response is used for delay computation and optimization, the resulting optimum interconnect lengths and driver sizes may also not be smooth functions of l. However, the magnitude of the resulting *kink* is very small as will be illustrated later.

Effect of Driver Characteristics on Interconnect Response

Driver resistance R_S and output capacitance C_P have a significant effect on the waveform and delay. Previous analyses have either considered ideal drivers, i.e., ignored both R_S and C_P [3] or ignored C_P [2, 4, 5, 6, 7]. Ignoring R_S leads to large errors in delay expressions and interconnect length optimization for delay minimization cannot be performed if $R_S = 0$. Ignoring C_P also introduces nonneglible errors in delay computation if C_P is comparable to C_L and line capacitance. For deep sub-micron technologies, C_P is actually larger than C_L and therefore should also be accounted for. Figure 3 shows that the step-response as well as the delay for distributed *RLC* lines are significantly affected if R_S or C_P are ignored.

Performance Optimization Methodology

There is a recent work that suggests an optimum repeater insertion scheme for *RLC* lines [8]. However, their delay model is identical to [2] (that ignores C_P) and requires curve fitting with circuit simulation results. Also, their empirical equations have a limited range of validity. A new optimal repeater insertion methodology is outlined below for distributed *RLC* lines.

For a step input, the $f \times 100\%$, (where $0 \leq f < 1$) delay, τ, (i.e., $v(\tau) = fV_0$) is the solution of the following equation

$$1 - f + \sum_i d_i \exp(s_i \tau) = 0 \tag{2}$$

For given values of d_is and s_is, the above equation can be solved numerically, (for instance, using Newton-Raphsons) to compute the value of τ.

Consider a long interconnect of length L. In order to minimize its delay, the line is broken up into buffered segments of length h, each of which is driven

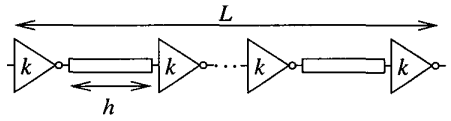

Fig. 4. Long interconnect broken up into buffered segments.

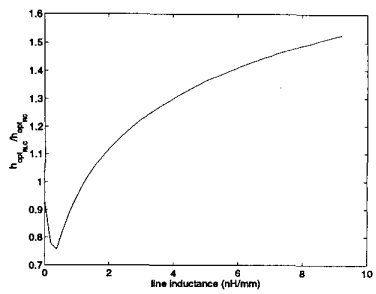

Fig. 5. $h_{opt_{RLC}}/h_{opt_{RC}}$ as a function of line inductance for 180 nm technology.

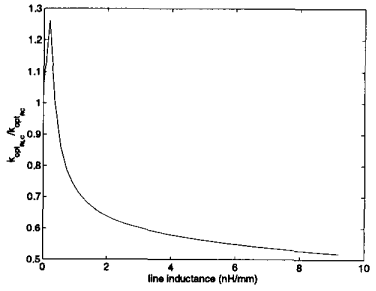

Fig. 6. $k_{opt_{RLC}}/k_{opt_{RC}}$ as a function of line inductance for 180 nm technology.

by a buffer of size k and has a delay τ (Figure 4). The overall delay of the line is given by total delay= $\frac{L}{h}\tau$. We therefore seek to minimize the *delay per unit length* τ/h. Setting the derivative of delay per unit length with respect to h and k to zero we have:

$$\frac{\partial \tau/h}{\partial h} = 0 \Rightarrow \frac{\partial \tau}{\partial h} = \frac{\tau}{h} \tag{3}$$

$$\frac{\partial \tau/h}{\partial k} = 0 \Rightarrow \frac{\partial \tau}{\partial k} = 0 \tag{4}$$

Differentiating (2) with respect to h and k and using (3) and (4) we get

$$0 = g_1 = \sum_i \left[\frac{\partial d_i}{\partial h} + d_i\left(\tau\frac{\partial s_i}{\partial h} + \frac{\tau}{h}s_i\right)\right]\exp(s_i\tau) \tag{5}$$

$$0 = g_2 = \sum_i \left[\frac{\partial d_i}{\partial k} + d_i\tau\frac{\partial s_i}{\partial k}\right]\exp(s_i\tau) \tag{6}$$

These equations can be solved numerically to obtain values of interconnect length $h_{opt_{RLC}}$ and buffer size $k_{opt_{RLC}}$ which result in minimum interconnect delay.

Results and Discussion

We now apply our optimization technique to the top level metal interconnects for 180 nm, 130 nm, 100 nm, 70 nm and 50 nm technology nodes as per ITRS specifications [9]. Full 3-D capacitance extraction was performed using FASTCAP [10]. Here we summarize our results for the 180 nm technology node and point out the salient characteristics of our performance optimization solution. The effect of technology scaling will be addressed in the following section.

First consider the case of optimum repeater insertion by considering only the line resistance and capacitance and optimizing the Elmore delay. The total Elmore delay of interconnect of length L (Figure 4) is given by

$$t_{Elmore} = \frac{L}{h}\left[\frac{r_s}{k}(c_p k + c_0 k) + \frac{r_s}{k}ch + rhc_0 k + \frac{1}{2}rch^2\right]$$

Therefore the optimum repeater size $k_{opt_{RC}}$ and interconnect length $h_{opt_{RC}}$ for minimum delay is given by

$$h_{opt_{RC}} = \sqrt{\frac{2r_s(c_0 + c_p)}{rc}} \qquad k_{opt_{RC}} = \sqrt{\frac{r_s c}{rc_0}}$$

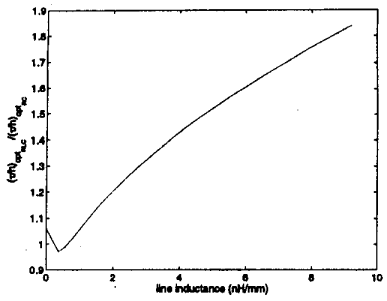

Fig. 7. Ratio of optimum delay per unit length, $(\frac{\tau}{h})_{opt_{RLC}}$, and $(\frac{\tau}{h})_{opt_{RC}}$ as a function of line inductance l for 180 nm technology.

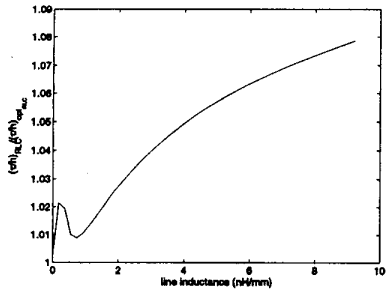

Fig. 8. Ratio of *RLC* delays per unit length of an interconnect with $h = h_{opt_{RC}}$ and $k = k_{opt_{RC}}$, and with $h = h_{opt_{RLC}}$ and $k = k_{opt_{RLC}}$ as a function of l for 180 nm technology.

Furthermore, the delay of one segment of length $h_{opt_{RC}}$ driven by a buffer of size $k_{opt_{RC}}$ is given by

$$\tau_{opt_{RC}} = 2r_s(c_0 + c_p)\left(1 + \sqrt{\frac{2c_0}{c_0 + c_p}}\right)$$

In general, for a given technology, r_s, c_p and c_0 cannot be easily determined. Moreover, r_s and c_p are voltage dependent. Therefore for this study, we find $h_{opt_{RC}}$ and $k_{opt_{RC}}$ by SPICE simulations. These simulations also provide $\tau_{opt_{RC}}$. Using the above equations, r_s, c_p and c_0 can be determined for a particular technology.

We now show the effect of including line inductance in the optimization as shown in the previous section. It should be noted that l is not a fixed parameter for a given technology and metal layer but depends on the current return path and varies substantially with input vectors. However, a worst-case number for line inductance can be determined as follows: the line inductance would be greatest when the current return path is the farthest from the line, i.e., the substrate. Let this inductance be $l_{\max}$. We have carried out delay minimization for $0 \le l < l_{\max}$.

Figure 5 shows the optimum interconnect length $h_{opt_{RLC}}$ as a ratio of $h_{opt_{RC}}$. Figure 6 shows the optimum buffer size $k_{opt_{RLC}}$ as a ratio of $k_{opt_{RC}}$. These plots also corroborate the observations made in [1] that with increasing line inductance l, the *RLC* interconnect increasingly resembles an ideal LC transmission line and the delay becomes progressively linear with interconnect length. Therefore $h_{opt_{RLC}}$ increases as the line inductance is increased and $k_{opt_{RLC}}$ reduces and asymptotes to a value for which the driver output impedance is equal to the characteristic impedance of the line. Figure 7 plots the ratio of optimized interconnect delay per unit length with and without considering line inductance as a function of l. As expected, the optimized interconnect delay per unit length increases as line inductance increases.

As discussed earlier, in a realistic scenario, it is very difficult to predict the effective interconnect inductance because the current return path varies a lot for different input vector patterns. As a result, it is difficult to target a specific value of the line inductance l and optimize the buffer size and interconnect length for that value of l. Therefore it is useful to determine the *RLC* interconnect delay for a given buffer size and interconnect length as the line inductance l is varied and compare it with the *RLC* based optimum delay for the corresponding values of l. As an example, suppose the driver size and interconnect length are chosen to be $k_{opt_{RC}}$ and $h_{opt_{RC}}$ respectively, i.e., without considering line inductance. For non-zero l, the *RLC* delay per unit length of this line would be greater than the *RC* delay. If l were known beforehand, one could optimize the driver size and interconnect length to potentially get a lower *RLC* interconnect delay per unit length $(\frac{\tau}{h})_{opt_{RLC}}$, as compared to the unoptimized case. Figure 8 plots the ratio of these two delays as a function of l. For the 180 nm technology the worst-case increase in delay over the optimized *RLC* case is 8%. Therefore even if the line inductance were known precisely, in the best case, there would be a meager 8% improvement in the delay per unit length.

Tech. node (nm)	180	130	100	70	50
width (nm)	525	382.5	280	195	137.5
height (nm)	1155	1033	756	546	399
t_{ins} (nm)	7699	6664	6022	5571	4116
ε_r	3.75	3.1	1.9	1.5	1.25
r (kΩ/m)	36.3	60.1	103.9	206.6	401.3
c (pF/m)	269	240	154	125	106
$l_{\max}$ (nH/mm)	9.2	10.9	13.5	17.9	18.8
$h_{opt_{RC}}$ (mm)	3.33	2.5	2.22	1.32	1.06
$k_{opt_{RC}}$	174	151	110	82	53
$\tau_{opt_{RC}}$ (ns)	0.165	0.147	0.125	0.089	0.071
r_s (kΩ)	8	9.5	10	15.8	12.5
c_0 (fF)	1.9	1.7	1.5	1.3	1.2
c_p (fF)	4.8	3.5	2.5	1.5	0.75

TABLE I
TECHNOLOGY AND EQUIVALENT CIRCUIT MODEL PARAMETERS FOR TOP LAYER METAL FOR DIFFERENT TECHNOLOGY NODES BASED ON THE ITRS.

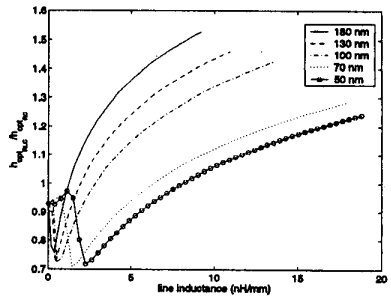

Fig. 9. $h_{opt_{RLC}}/h_{opt_{RC}}$ as a function of line inductance for various technology nodes.

Effect of Technology Scaling

We now consider the effect of inductance with technology scaling. Various technology parameters are shown in Table I and are based on ITRS data. Note that r increases dramatically with scaling as the line dimensions of the top level metal layers also scale. Figures 9, 10, 11 and 12 plot the ratio of $h_{opt_{RLC}}$ and $h_{opt_{RC}}$, $k_{opt_{RLC}}$ and $k_{opt_{RC}}$, $(\frac{\tau}{h})_{opt_{RLC}}$ and $(\frac{\tau}{h})_{opt_{RC}}$, and the ratio of *RLC* delay per unit length of an interconnect with $h = h_{opt_{RC}}$ and $k = k_{opt_{RC}}$, and *RLC* delay with $h = h_{opt_{RLC}}$ and $k = k_{opt_{RLC}}$ as a function of l respectively. For all these figures, note that effect of inductance on performance is reducing as the technology scales. This is best illustrated by Figures 11 and 12. For example, in Figure 11 the ratio of optimal *RLC* and *RC* delays per unit length approaches 1 as the technology scales even though $l_{\max}$ is increasing as the technology scales.

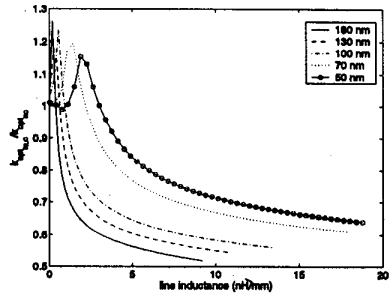

Fig. 10. $k_{opt_{RLC}}/k_{opt_{RC}}$ as a function of line inductance for various technology nodes.

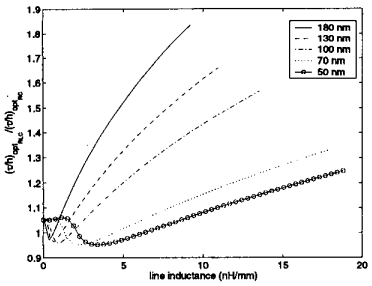

Fig. 11. Ratio of optimum delay per unit length, $(\frac{\tau}{h})_{opt_{RLC}}$, and $(\frac{\tau}{h})_{opt_{RC}}$ as a function of line inductance l for various technology nodes.

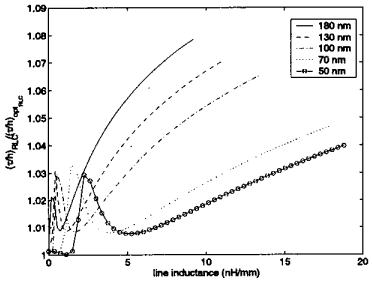

Fig. 12. Ratio of *RLC* delays per unit length of an interconnect with $h = h_{opt_{RC}}$ and $k = k_{opt_{RC}}$, and with $h = h_{opt_{RLC}}$ and $k = k_{opt_{RLC}}$ as a function of l for various technology nodes.

Another way of visualizing the same phenomenon is by using the concept of critical inductance. As an illustration, consider the second order approximation of the transfer function in (1), i.e.,

$$H(s) \approx \frac{1}{1+b_1 s+b_2 s^2}$$

This second order system is *critically damped*, *overdamped* and *underdamped* when $b_1^2 - 4b_2$ is equal to, greater than or less than 0 respectively. The response of an overdamped system is very similar to an RC line. Since b_1 and b_2 are functions of h and k and b_2 is a function of l (as shown earlier), at $h = h_{opt_{RLC}}$ and $k_{opt_{RLC}}$, a value l_{crit} can be obtained for which the system will be critically damped. l_{crit} is given by

$$l_{crit} = \frac{\frac{b_1^2}{4} - \frac{r^2c^2h^4}{4!} - R_S(C_P+C_L)\frac{rch^2}{2!} - (R_Sch+C_Lrh)\frac{rch^2}{3!} - R_SC_PC_Lrh}{\frac{ch^2}{2!}+C_Lh}$$

Figure 13 plots this critical inductance as a function of l. Recall that the system is overdamped if $l < l_{crit}$. We find that l_{crit} increases as the technology scales which also implies the diminishing effect of line inductance since the range of l over which the system is overdamped increases with scaling. The above analysis has been carried out assuming that the width of the topmost metal layer

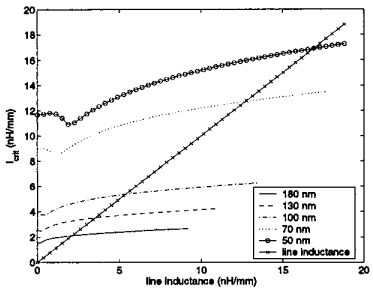

Fig. 13. Critical inductance as a function of line inductance for various technology nodes.

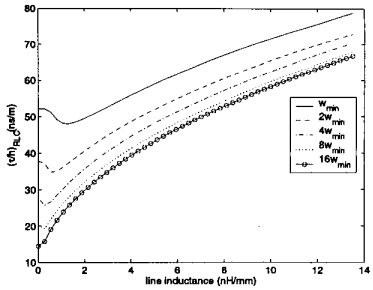

Fig. 14. *RLC* delay per unit length for five different line widths for 100 nm technology node as a function of line inductance.

is the minimum width prescribed by the ITRS data. However, to reduce signal delay interconnects which are wider than the minimum width are often used in high performance design. For these lines, the resistance per unit length is smaller and therefore inductive effects can become significant. As an illustration, consider the top layer metal in 100 nm technology node. Five different metal widths are considered: $w_{\min}$, $2w_{\min}$, $4w_{\min}$, $8w_{\min}$ and $16w_{\min}$. $h_{opt_{RC}}$ and $k_{opt_{RC}}$ are recomputed for each of these widths. Figure 14 plots the *RLC* delay per unit length as a function of l when an interconnect of length $h_{opt_{RC}}$ is driven by a buffer of size $k_{opt_{RC}}$ for each of these line widths. As expected, for very small values of l, the delay of the wider lines is much smaller but as l increases, the advantage of using wider lines diminishes as the difference between the delays per unit length for different line widths reduces.

Conclusion

In conclusion, this paper has presented an accurate analysis of on-chip inductance effects for distributed *RLC* interconnects. Unlike previous work, the effects of both the series resistance and the output parasitic capacitance of the driver have been taken into account. Using rigorous analysis, accurate expressions for the transfer function of these lines and their time-domain response have been presented for the first time. It is shown that complete driver characteristics must be included in the analysis of distributed *RLC* interconnect structures for computing their precise time delay. Furthermore, an optimal repeater insertion scheme for distributed *RLC* interconnects has also been presented using a novel performance optimization technique. Most importantly, the impact of line inductance on optimum interconnect performance has been analyzed in detail for future deep submicron technologies based on the ITRS. Contrary to conventional wisdom, it is shown that the effect of inductance on optimized interconnect performance will actually *diminish* for scaled global interconnects.

Acknowledgments

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