Non-Uniform Chip-Temperature Dependent Signal Integrity

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Abstract

In traditional design flows the temperature of the chip is assumed to be uniform across the substrate. However, for most high-performance designs, the substrate temperature is non-uniform, which can be a major source of inaccuracy in delay and skew computations. This paper introduces the analysis and modeling of non-uniform substrate temperature and its effect on signal integrity. Using a novel non-uniform temperature-dependent analytical distributed RC interconnect delay model, the thermally dependent signal integrity metrics, i.e. signal delay and clock skew, are analyzed and some design techniques are provided to eliminate the non-uniform temperature-dependent clock skew.

I. Introduction

Management of thermally related issues is rapidly becoming one of the most challenging efforts in high-performance chip designs [1]. At the circuit level, thermal problems have important implications for circuit performance and reliability [2]. Dynamic power management and functional block clock gating tend to cause large thermal gradients over the substrate. Furthermore, as the technology feature size shrinks down, the upper metal layers that carry the global signals (including the clock) get closer to the substrate [1]. Consequently, the effect of non-uniform substrate temperature on the interconnect temperature profile becomes more critical. This thermal non-uniformity causes a non-uniform temperature profile along global signal lines, resulting in a non-uniform interconnect resistance per unit length. In high performance designs, it is of utmost importance to provide design techniques to overcome physical non-uniformities and process variations. This is necessary to provide uniform unit length interconnect capacitance and resistance in order to ensure a near-zero clock skew [3]. Hence, analysis and modeling of the effect of non-uniform substrate temperature on the integrity of global signal lines is critical.

II. Non-Uniform Chip and Interconnect Thermal Profile

Due to the different switching activities of the cells in the substrate, a non-uniform temperature gradient, which is created by the so-called *hot spots* in the substrate, is inevitable. Since long global wires span a large area of the substrate surface, they will pass over these hot spots. As a result, determining the interconnect thermal profile is crucial to the signal integrity analysis of the global interconnects.

Consider an interconnect with length L, width w and thickness t_m that passes over the substrate with an insulator of thickness t_{ins} and thermal conductivity k_{ins} separating the two (Figure 1). The interconnect is connected to the substrate by vias/contacts at its two ends. Using appropriate boundary conditions, the temperature profile along the interconnect can be obtained by solving the heat diffusion equation. In the steady state, by assuming that the four sidewalls and the top surface of the chip are thermally isolated (which are in general valid assumptions), the heat diffusion equation can be written as follows:

$$\frac{d^2 T_{line}(x)}{dx^2} = \lambda^2 T_{line}(x) - \lambda^2 T_{ref}(x) - \theta \qquad (1)$$

where λ and θ are constants given as follows:

$$\lambda^2 = \frac{1}{k_m}\left(\frac{k_{ins}}{t_m \cdot t_{ins}} - \frac{I_{rms}^2 \cdot \rho \cdot \beta}{w^2 \cdot t_m^2}\right) \quad , \quad \theta = \frac{I_{rms}^2 \cdot \rho}{w^2 \cdot t_m^2 \cdot k_m} \qquad (2)$$

T_{line} is the interconnect temperature as a function of position along the length of the interconnect, T_{ref} is the substrate temperature, ρ is the metal electrical resistivity at the reference temperature (0 °C), and β is the temperature coefficient of interconnect metal resistance in 1/°C. In order to have a unique solution for (1), we need to provide two boundary conditions. Figure 2 and 3 show the thermal profiles of the point-to-point interconnect depicted in Figure 1 for two different technology nodes under various substrate thermal profiles.

III. Non-Uniform Temperature-Dependent Signal Delay Model

The resistance of the interconnect is a function of the line temperature as $r(x)=r_0(1+\beta.T(x))$ where r_0 is the unit length resistance at 0 °C and β is the temperature coefficient of resistance (1/°C). Consider an interconnect with length L and uniform capacitance per unit length c_0 that is driven by a driver of output resistance R_d and terminated by a load with capacitance C_L. Using a distributed RC Elmore delay model, the delay D of a signal passing through the line can be written as follows:

$$D = R_d \cdot \left(C_L + \int_0^L c_0(x)dx\right) + \int_0^L r(x) \cdot \left(\int_x^L c_0(\tau)d\tau + C_L\right)dx \qquad (3)$$

By applying the temperature-dependent resistance, the signal delay is:

$$D = D_0 + (c_0 L + C_L)\, r_0 \beta \int_0^L T(x)dx - c_0 r_0 \beta \int_0^L x T(x)dx \qquad (4)$$

where:

$$D_0 = R_d(C_L + c_0 L) + \left(c_0 r_0 \frac{L^2}{2} + r_0 L C_L\right) \qquad (5)$$

D_0 is the Elmore delay (at 0 °C) when the effect of temperature on the line resistance is neglected. Figure 5 shows the delay degradation due to temperature increase in an interconnect for various lengths using the parameters listed in Table 1 (assuming a constant thermal profile). In reality, and especially for long global lines, the thermal profile along the length of an interconnect is non-uniform. Figure 6 shows the importance of the line temperature non-uniformities on the delay by considering two different exponential thermal profiles depicted in Figure 4 for two different lengths. This shows that the assumption of a constant temperature along the wire (with peak-value) can introduce a large error in wire planning, wire routing, wire sizing and clock-skew analysis.

IV. Non-Uniform Temperature-Dependent Clock Skew

In addition to the performance degradation introduced by increasing temperature in the interconnect, the non-uniform thermal profile along upper layer interconnects has a major impact on the skew of the clock signal net. To ensure zero skew clock distribution, symmetric H-Tree structure or bottom-up merging are most commonly used [4]. In general, the top-level segments of the clock tree are long and assigned to the upper metal layers (Figure 7). As a result, they are exposed to the thermal non-uniformities in the substrate. Such non-uniformities result in different signal delays at the two ends of the clock tree segments, creating a non-zero skew in the tree. To ensure zero skew, we need to find the division point x along the length of the global segment (Figure 8) such that when the clock signal driver is connected to that point, the delay at the two ends of the segment becomes the same. By considering propagation delay from the driver to the two ends p and q and using (4), the optimum length l^* that guarantees zero clock skew can be obtained by solving the following equation:

$$\beta \int_0^{l^*} T(x)dx + l^* - A = 0 \qquad (6)$$

where A is a constant and can be written as follows:

$$A = \frac{1}{Lc_0 + C_L}\left(\frac{L^2 c_0}{2} + LC_L + \beta(Lc_0 + C_L)\int_0^L T(x)dx - c_0 \beta \int_0^L x T(x)dx\right) \qquad (7)$$

Given circuit parameters L, C_L, c_0, β and $T(x)$, one can easily compute the constant A and solve (6) to obtain the optimum position for the clock signal connection to the net segment. From (6), it is seen that with a constant thermal profile $T(x)$ along the length of the interconnect, we can guarantee a zero skew by connecting the clock signal at $l=L/2$. In fact, even a non-uniform but *symmetrical* thermal profile with the symmetry axis at $l=L/2$ results in a zero clock skew when the driver is connected to the middle of the line. We also see that a gradually decreasing (increasing) thermal profile along the length of the line from 0 to L (from p to q), results in an optimum length l^* less than (greater than) $L/2$. Table 2 shows the behavior of temperature-dependent clock skew for a 2000 µm line by applying three different interconnect thermal profiles. The third set of profiles approximates a hot spot along the length of an interconnect by using a constant-peak normal distribution with peak T_{max} (°C) at 100 °C, mean μ (µm) and standard deviation σ (µm). The reported normalized skew percentage in column 4 represents the ratio of the clock skew when $l=L/2$ over the delay from the driver to any endpoint of the interconnect when $l=l^*$. Hence,

the normalized skew percentage represents the skew if the location of the driver insertion into the clock line did not account for the non-uniform temperature profile along the interconnect length. These results show that neglecting the effects of thermal profiles on the clock tree delay fluctuations changes the normalized skew by as much as 10 percent and can dramatically affect the clock signal performance.

V. Conclusion

In conclusion, a detailed analysis of the impact of non-uniform chip-temperature distributions on the signal integrity of global lines was presented using a new analytical distributed RC delay model that incorporates the non-uniform interconnect temperature dependency. It was shown that non-uniform temperature distributions along long global wires in high-performance ICs can have a significant impact on the interconnect performance and the worst-case clock skew. Finally, an analytical model that helps the designers to cope with the non-uniformities in the chip-temperature during the clock net routing has been presented for the first time.

References:

[1] S. Im and K.Banerjee, *Tech. Digest IEDM*, 2000, pp. 727-730.

[2] K. Banerjee *et al.*, *36th Design Automation Conference*, 1999, pp. 885-891.

[3] P. Zarkesh-Ha *et al.*, *Proc. CICC* 1999, pp. 441-444.

[4] T.H. Chao *et al*, *IEEE Trans. Circuits and Systems-II*, vol. 39, no. 11, pp. 799-814, 1992.

[5] National technology Roadmap for Semiconductors (NTRS), 1997.

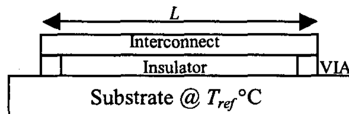

Figure 1: A point-to-point interconnect of length L over the substrate.

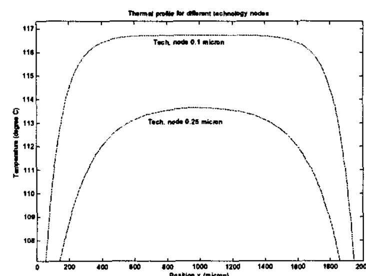

Figure 2: Thermal profile along the length of an interconnect with uniform substrate temperature using NTRS [5] interconnect parameters for 0.1 and 0.25 μm technology nodes.

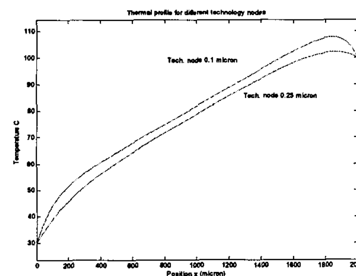

Figure 3: Thermal Profile along the length of an interconnect with a linear substrate thermal profile using parameters of 0.1 and 0.25 μm technologies provided by the NTRS.

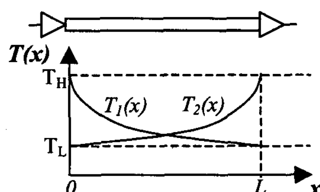

Figure 4: Schematic of two different exponential thermal profiles.

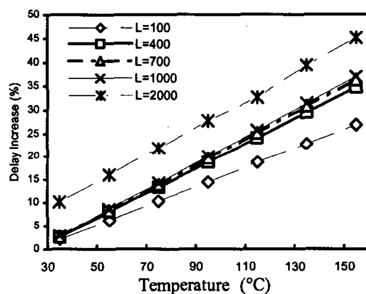

Figure 5: Delay degradation due to the increase of the interconnect temperature as a result of a uniform substrate thermal profile and Joule heating.

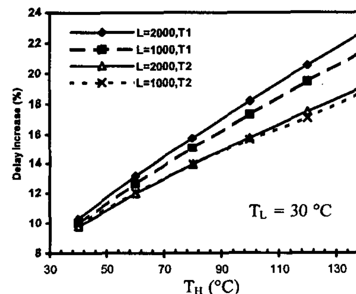

Figure 6: Delay degradation using the thermal profiles depicted in Figure 4 where T_H and T_L are the upper and lower temperature bounds, respectively.

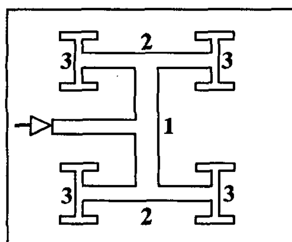

Figure 7: A balanced-load symmetrical H-Tree.

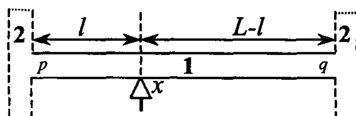

Figure 8: Optimal location for inserting the driver into the tree to guarantee zero skew.

Parameter	Nominal value	Unit
β	3E-03	1/°K
r_{sh}(25°C)	0.077	Ω/sq
c_{sh}	0.2	fF/sq
w	0.32	μm
R_d	10	Ω
C_L	1000	fF

Table 1: Parameters used in this work.

Thermal Profile	Parameters	l*	*Normalized Skew %*
$T(x) = ax+b$, $a = \frac{T_H - T_L}{L}$, $b = T_L$	T_H=170, T_L=90	1042	5.42
	T_H=170, T_L=110	1032	3.98
	T_H=170, T_L=130	1021	2.65
	T_H=170, T_L=150	1012	1.29
$T(x) = a \cdot e^{-bx}$, $a = T_H$, $b = \frac{1}{L}\ln(\frac{T_H}{T_L})$	T_H=170, T_L=90	957.5	5.24
	T_H=170, T_L=110	968.66	3.63
	T_H=170, T_L=130	979.5	2.40
	T_H=170, T_L=150	989.7	1.19
$T(x) = T_{max} \cdot e^{-\frac{(x-\mu)^2}{2\sigma^2}}$	μ=2000, σ=1000	1210	7.78
	μ=1000, σ=400	1000	0.0
	μ=500, σ=400	827	10.7
	μ=300, σ=700	911	9.57

Table 2: Comparison between the different non-uniform substrate thermal profiles and their effects on clock skew.