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Thermal Scaling Analysis of Multilevel Cu/Low-k Interconnect Structures in Deep Nanometer Scale Technologies

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Abstract

This paper presents a comprehensive thermal scaling analysis of multilevel interconnects in deep nanometer scale CMOS technologies based on technological, structural, and material data from ITRS '03 [1]. Numerical simulations have been performed using three-dimensional (3-D) electrothermal finite element methods (FEM), combined with accurate calculations of temperature- and size-dependent Cu resistivity and thermal conductivity of low-k interlayer dielectrics (ILD) based on fully physical models. The simulations also incorporate various scaling factors from fundamental material level to system level: the via-density dependent effective ILD thermal conductivity, the hierarchically varying RMS current stress based on SPICE simulations, and the thermal resistance of flip-chip package. It is shown that even after considering densely embedded vias, the interconnect temperature is expected to increase significantly with scaling, due to increasing surface and grain boundary contributions to metal resistivity and decreasing ILD thermal conductivity.

Introduction

Accurate estimates of multilevel interconnect temperatures are necessary for interconnect performance and reliability assessment in high performance VLSI circuits [2-3]. While some analytical thermal models are available for multilevel interconnects, the complicated multi-dimensional heat conduction within the 3-D interconnect structures are either neglected or treated approximately [4-7]. Previous thermal simulations for multilevel interconnects often assumed simplified geometries such as all parallel lines in six levels of metallization [8] and orthogonal wires in three to four metal levels [9-10]. Rigorous thermal analysis of multilevel interconnects must consider complex 3-D thermal coupling due to orthogonal interconnect arrays, densely embedded vias, increasing number of metal levels, and nonuniform current stress conditions.

This paper significantly improves upon our previous work [11] by including temperature- and size-dependent Cu resistivity, effective ILD thermal conductivity accounting for both varying via densities and via Joule heating, package thermal resistance scaling for high I/O chips, and realistic metal-level dependent RMS current stress inputs. In this paper, we first examine the scaling physics of Cu resistivity and low-k thermal conductivity. Secondly, we address detailed methodologies for the accurate FEM simulations including via density and flip-chip package effects. Finally, a scaling analysis of the multilevel interconnect temperature is presented along with discussion.

The predictions made for interconnect temperatures can be used for investigating highly coupled electrothermal phenomena resulting from material property and physical parameter scaling dictated by technology evolutions. These results can also be used for enhancing backend thermal management, performance, and reliability, and for incorporating thermal-awareness in interconnect design issues such as power/ground distribution network and clock design.

Material Property Scaling

A. Cu Resistivity Scaling

The metal resistivity increase is an emerging concern as the ITRS projected metal widths (21-237.5 nm) can be smaller than the mean free path of electrons (40 nm for Cu at room temperature). The compact analytical model in [12] is used to calculate the resistivity of rectangular wires, which is based on the Fuchs-Sondheimer model [13, 14] regarding surface scattering and the Mayadas and Shatzkes (MS) model [15] regarding grain boundary scattering of electrons,

$$\rho = \rho_o \left\{ \frac{1}{3} \Big/ \left[\frac{1}{3} - \frac{\alpha}{2} + \alpha^2 - \alpha^3 \ln\left(1 + \frac{1}{\alpha}\right) \right] + \frac{3}{8} C(1-p) \frac{1+AR}{AR} \frac{\lambda}{w} \right\}$$
$$\alpha = (\lambda / d_g)[R/(1-R)], \quad (1)$$

where ρ_o is the bulk resistivity, λ is the mean free path of electrons, w is the metal width excluding barrier layer thickness, AR is the aspect ratio (height over width), p is the specularity parameter, R is the reflectivity coefficient at grain boundaries, d_g is the average distance between grain boundaries ($d_g \sim w$, if $w <$ 320-400 nm [12]), and C is a constant (1.2 for rectangular cross sections). The barrier layer effect is also included in our calculations by using corrected w and AR for the ITRS specified barrier layer thickness.

The temperature- and size-dependent resistivity values are calculated for local, intermediate, and global wires at each technology node using (1) with the ITRS dictated metal dimensions at each technology node (Appendix). In advanced technology nodes, ρ is expected to increase significantly above ρ_o mainly due to the enhanced surface and grain boundary scattering effects (Fig. 1). The contribution of surface scattering and grain boundary scattering is roughly the same. The background scattering of the electrons by phonons,

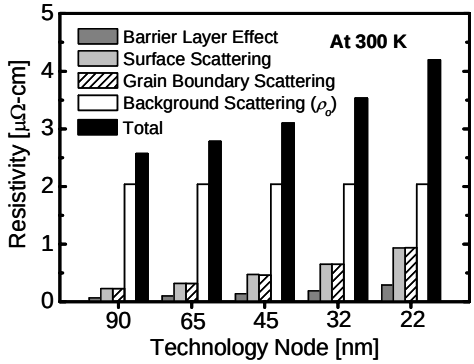

Fig. 1. Scaling of Cu resistivity for the ITRS intermediate wires (at 300K). The total resistivity is the sum of all resistivity components. Parameters are average values based on [12]: ρ_o=2.04 μΩ-cm (300K), λ=37.3 nm (300K), p=0.41, and R=0.22.

electrons and defects (impurities) contributes to ρ_o. The temperature-dependent resistivity values are calculated by plugging known temperature-dependent parameters (ρ_o and λ) [16] into (1). Note that other scattering parameters (p and R) are independent of temperature.

B. Low-k ILD Thermal Conductivity Scaling

The low-k dielectric materials for inter-layer dielectric (ILD) applications are expected to have much lower thermal conductivities than oxide. It is important to assess the correlation of the thermal conductivity and dielectric constant in order to evaluate the tradeoff between electrical and thermal performance. While the ITRS specifies the dielectric constant of ILD (k_{ILD}) at each technology node, the thermal conductivity of ILD (K_{ILD}), one of the essential material properties for electrothermal FEM simulations, is not available. It is difficult to find a universal relationship between K_{ILD} and k_{ILD} encompassing all low-k dielectric candidates owing to the intrinsic differences in their compositions and structures.

The relationship between K_{ILD} and k_{ILD} can be found if a dielectric material is porous. Using the Bruggemann effective medium theory [17], the k_{ILD} is expressed as

$$P\left(\frac{k_p - k_{ILD}}{k_p + 2k_{ILD}}\right) + (1-P)\left(\frac{k_m - k_{ILD}}{k_m + 2k_{ILD}}\right) = 0, \quad (2)$$

where P is the porosity ($0 < P < 1$), k_p is the dielectric constant of pores, and k_m is the dielectric constant of a matrix material.

The thermal conductivity of a porous dielectric material can be obtained from several models such as the parallel model, the serial model, the dilute particle model, the dilute fluid model, the porosity weighted simple medium (PWSM) model, the porosity weighted dilute medium (PWDM) model [18-19], and the differential-effective-medium (DEM) model [20]. The PWSM model for K_{ILD} is given by

$$K_{ILD} = [PK_p + (1-P)K_m](1-P^x) + \frac{K_p K_m P^x}{PK_m + (1-P)K_p}, \quad (3)$$

where K_p is the thermal conductivity of pores, K_m is the thermal conductivity of a matrix material, and x is the fitting parameter. Calculating K_{ILD} and k_{ILD} values by varying P ($0 < P < 1$) numerically yields the relationship between K_{ILD} and k_{ILD} for a given porous dielectric material.

In Fig. 2, predictions based on the DEM and PWSM models for porous silicate (xerogel) films are plotted with experimental data from literatures for various low-k candidates including xerogel: fluorinated silicate glass (FSG) [21], hydrogen-silsesquioxane (HSQ) [20, 22], carbon-doped oxide (CDO) [21-22], organic polymers [22], methyl-silsesquioxane (MSQ) [23], and xerogel [20, 24-25]. It can be observed that the PWSM model fits better with experimental data for xerogel. Although this model is plotted for xerogel, it can be used as a reasonable upper-bound of K_{ILD} for other low-k dielectrics. We extracted the required K_{ILD} values corresponding to the ITRS specified bulk k_{ILD} values using (2)-(3) with $0.357 < P < 0.668$ and parameters for xerogel.

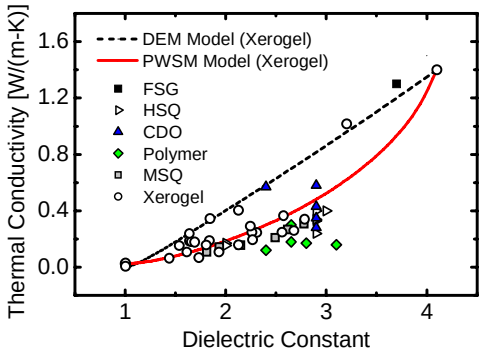

Fig. 2. Correlation of the thermal conductivity and dielectric constant. The DEM and PWSM models for xerogel films are calculated using parameters k_p=1, k_m=4.1, K_p=0.0255 W/(m-K), K_m=1.4 W/(m-K), and x=0.49 [18]. P is varied continuously from 0 to 1. P=0 yields properties of a fully dense material (silicate) and P=1 those of air.

Finite Element Electrothermal Simulations

A. Via Effects

The vias and contacts can be efficient heat dissipation paths from the upper level interconnects to the Si substrate and heat sink because they have much higher thermal conductivities than the ILD layers. On the other hand, since these electrical vias and contacts carry current, they also generate heat within their structures and increase the temperature of metal lines connected to them. Accurate estimates of interconnect temperature rise must consider these two opposite effects of vias [26]. The thermal impact of vias can be quantitatively represented by the effective thermal conductivity of ILD layers ($K_{ILD,eff}$). The $K_{ILD,eff}$ value strongly depends on the via density in each ILD layer, which is typically higher for local levels and lower for global levels. The analytical models for $K_{ILD,eff}$ have been derived by the one-dimensional (1-D) thermal circuit analysis [5, 27] or by solving heat conduction equations [7].

In order to evaluate existing analytical models for $K_{ILD,eff}$, FEM simulations are performed for the unit cell of periodic metal/via structure in Fig. 3(b). Considering heat dissipation

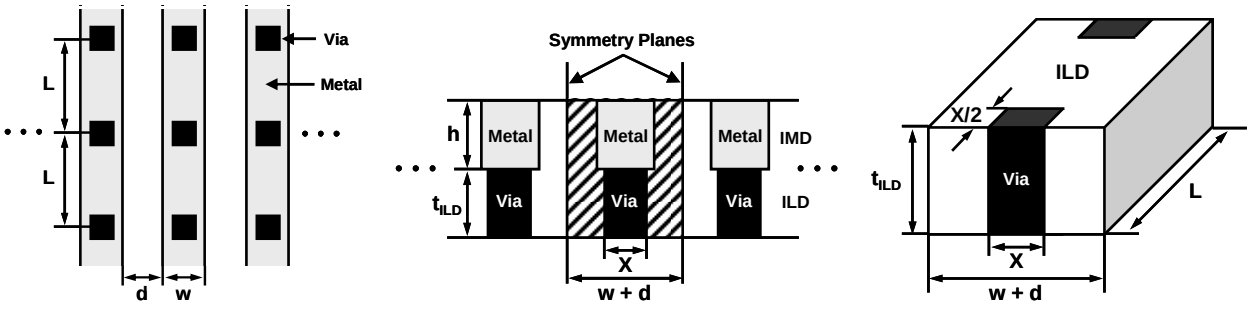

Fig. 3. Schematic of a periodic array of metal lines and vias: (a) layout, (b) cross section, and (c) the volume defining the via density. For a periodic array of uniformly spaced metal lines and vias in (a), a unit cell can be defined as the volume between the symmetry planes in (b). The unit cell contains one metal line segment within the inter-via distance L, two halves of vias and surrounding dielectrics.

from the sides of metal lines, the effective width where thermal conduction takes place is assumed as the entire width of the unit cell (=w+d). Constructing an equivalent 1-D thermal circuit for the unit cell results in

$$K_{ILD,eff} = f \cdot K_V + (1-f)K_{ILD}, \quad (4)$$

$$f = X^2/[(w+d)L], \quad (5)$$

where f ($0 < f < 1$) is the via density defined as the ratio of the via volume to the underlying ILD volume within the unit cell, as illustrated in Fig. 3 (c), K_V is the via thermal conductivity, K_{ILD} is the ILD thermal conductivity without vias, X is the via size, w is the metal width, d is the metal spacing, and L is the inter-via distance along the metal line. In this paper, the via size X is assumed to be the same as the minimum line width connected to the via.

The FEM simulations are performed for the unit cell of metal/via structure with varying L. Both metal and via Joule heating is induced by applying the same current through the metal line and via. The adiabatic thermal boundary condition is assumed at the top of the unit cell. The intermetal dielectric (IMD) layers are assumed to be the same material as the bulk ILD layers. The $K_{ILD,eff}$ values are extracted from FEM simulations by $K_{ILD,eff}=(J^2\rho \cdot h \cdot t_{ILD})/\Delta T_{avg}$, where J is the current density in the metal line, ρ is the metal resistivity, h is the metal height, t_{ILD} is the ILD thickness, and ΔT_{avg} is the average temperature rise of the metal line with respect to the bottom surface of the unit cell. Figure 4 compares the $K_{ILD,eff}$ values extracted from FEM simulations with the predictions

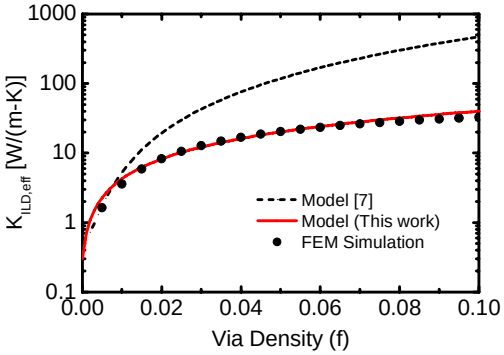

Fig. 4. Effective thermal conductivity of ILD layers ($K_{ILD,eff}$) as a function of via density (f). Simulation parameters are based on metal 1 (M1) of 65 nm technology node: $w = d = X = 76$ nm, $h = t_{ILD} = 129.2$ nm, $K_{ILD} = 0.3$ W/(m-K), $K_M = K_V = 396.36$ W/(m-K), $J = 3$ MA/cm^2, $\rho = 5.75$ μΩ-cm, and the reference temperature is 85 °C.

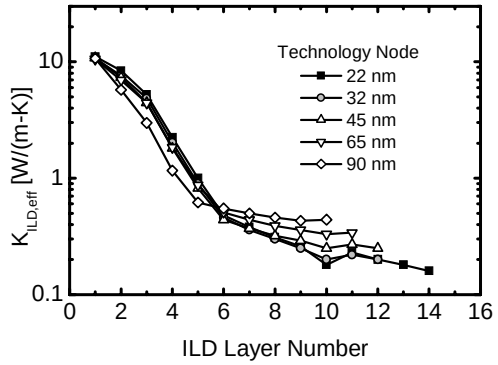

Fig. 5. Effective thermal conductivity of ILD layers ($K_{ILD,eff}$) as a function of ILD layer number for different technology nodes. The n^{th} ILD layer is defined as the ILD layer between the $(n\text{-}1)^{th}$ and n^{th} metal levels from the substrate.

from thermal models as a function of f. It is shown that the $K_{ILD,eff}$ using (4)-(5) fits better with the FEM simulation results. A previous model [7], which neglects heat dissipation from the sides of metal lines and heat generation in the vias themselves, significantly overestimates $K_{ILD,eff}$ especially for the higher via density ranges. In this work, (4)-(5) are used for calculating $K_{ILD,eff}$.

The via density (f) or inter-via distance (L), which is not provided by the ITRS, varies with metal level depending on various circuit design parameters. In this work, we propose reasonable L values at successive metal levels using the following criteria. For local (M1) wires, L is taken as the typical local interconnection length which is roughly 2-3 times the source/drain diffusion length of a minimum sized NMOS. For intermediate wires, the metal wire at the center of intermediate tier (M5 for 90 nm node and M6 for the other nodes) is assumed to have an inter-via distance equal to the typical length of intermediate level interconnections. For the topmost global wire, the typical inter-buffer distance (hence L) for optimal delay in the longest global wires at the current technology node (90 nm node) is taken as 1 mm, and for future technology generations this length is scaled in accordance with wire width scaling. For the remaining successive metal levels, the L values are assigned by linear interpolations on a log scale.

With these metal-level dependent L values and corresponding metal widths, the via density (f) values are calculated by using (5) for different technology nodes assuming d=w, and the $K_{ILD,eff}$ values are calculated by using (4). For the first ILD layer that is the premetal dielectric (PMD) layer, we assumed phospho silicate glass (PSG) as a PMD material and tungsten as a contact material with thermal conductivities of 0.94 W/(m-K) [28] and 165 W/(m-K) [29], respectively. Figure 5 plots the ILD layer dependent $K_{ILD,eff}$ values for different technology nodes. It is shown that the $K_{ILD,eff}$ values of lower ILD layers become much larger than the bulk ILD thermal conductivity, K_{ILD}=0.12-0.4 W/(m-K) (Appendix), due to densely embedded local vias. In the FEM simulations, these $K_{ILD,eff}$ values are parametrically assigned to each ILD layer as material properties, which effectively include vias with varying densities.

B. Package Effects

Heat dissipated from the multilevel interconnect stacks is often assumed to be removed through the Si die, integrated heat spreader (IHS) and heat sink by neglecting heat dissipation through the package layers to the printed-circuit board (PCB) [11]. Figure 6 shows schematic of a standard flip-chip controlled collapsed chip connection (C4) package. The topmost global interconnects covered by passivation layers are attached to the (solder bumps + underfill) layer, package substrate, solder balls, and PCB. In our simulations, we applied the ITRS specified constant temperatures (T_j) at

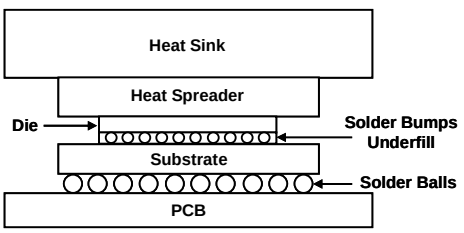

Fig. 6. Schematic of flip chip C4 package.

the Si junction, assuming that the thermal performance of thermal interface materials (TIM), IHS, and heat sink continues to improve in order to maintain the ITRS specified T_j with increased chip power densities. The required junction-to-ambient thermal resistance (toward the heat sink) needs to be continuously decreased from 88.24 mm^{2}K/W (90 nm node) to 43.01 mm^{2}K/W (22 nm node). Unlike our previous work [11], we effectively include heat dissipation through the package layers in our simulations by adding an equivalent package layer with thermal resistance of $R_{th,eq}$ to the topmost global wires,

$$R_{th,eq} = \sum_i R_{th,i} = \sum_i (t_i / K_i), \quad (6)$$

where i represents each package layer from passivation layers to PCB, $R_{th,i}$ is the thermal resistance (in mm^{2}K/W), t_i is the thickness, and K_i is the thermal conductivity of the i^{th} package layer, respectively.

For the **(**solder bumps + underfill**)** layer, we calculate the effective thermal conductivity ($K_{U,eff}$) at each technology node using the 1-D thermal circuit model similar to (4) and ITRS specified area array flip chip package requirements (Appendix) for high-performance microprocessor units (MPU). The calculated $K_{U,eff}$ values are 1.24-2.57 W/(m-K), which are within the range of published values [30-32]. For the other package layers, we use thickness and thermal conductivity values from [10, 21, 28, 30-31] to calculate the thermal resistance $R_{th,i}$ in each layer. The impact of **(**solder bumps + underfill**)** layer scaling is expected to be negligible, overwhelmed by the huge thermal resistances of other package layers such as the solder ball/air layer and PCB. The calculated $R_{th,eq}$ values are two orders of magnitude higher than the junction-to-ambient thermal resistances (toward the heat sink). Therefore, most heat dissipated from the multilevel interconnects is expected to be removed through the Si die, IHS and heat sink.

C. FEM Simulation Methodology

The 3-D electrothermal FEM simulations are performed by ANSYS® to account for temperature-dependent Joule heating of orthogonal multilevel interconnects. Parameters are based on the ITRS data for high performance MPUs (Appendix). The metal spacing for M1 is assumed to be the same as the width of M1. The spacings for intermediate and global wires are slightly adjusted with the spacing to width ratio of 1-1.22. With adjusted spacings, the ratio of the number of M1, intermediate and global lines per unit area is found to be 4:3:2 for all technology nodes. Assuming that all metal lines are uniformly spaced with this ratio and infinitely long, a unit cell can be defined by symmetry planes (Fig. 7). FEM simulations are performed for this unit cell, where four side walls satisfy symmetric (adiabatic) boundary conditions. The $\rho_{eff}(T)$ values are assigned to each metal line in a tabular form. The thermal conductivity of all intermetal dielectric (IMD) layers is the same as that of bulk ILD layers without vias (K_{ILD}). The $K_{ILD,eff}$ values accounting for metal-level dependent via densities are assigned to each ILD layer. The constant temperature boundary conditions (BC) are applied at the bottom of the unit cell (T_j) and at the top of the equivalent package layer (T_{amb}), where T_{amb} is the ITRS projected constant ambient temperature (45 ^{o}C). All model dimensions, material properties, and current loads are represented by parameters, which facilitate modifications.

The metal-level and technology dependent RMS currents (I_{rms}) are applied to all wires as the input loads in the electrothermal FEM simulations. The ITRS provides a single value of the maximum current density (J_{max}) for intermediate wires at each technology node. First, we assume that the ITRS specified J_{max} is the average current density (J_{avg}) and then calculate the average current (I_{avg}) at each technology node by $I_{avg}=J_{avg}\cdot A_i$, where A_i is the cross sectional area of intermediate wires. Assuming that I_{avg} is constant for all metal wires at a given technology node, the I_{rms} values are finally calculated by $I_{rms}=I_{avg}/r^{0.5}$, where r is the metal-level and technology dependent duty ratio. In this work, the r values at different metal levels and technology nodes are calculated for the first time (Table 1). The typical VLSI circuit scenario of a gate driving an appropriate interconnection and a capacitive load is used to estimate the duty ratio from SPICE simulations. It must be noted that the methodology used for the duty ratio calculations follow the same principle as that used for predicting the clock frequencies and minimum logic depths in the ITRS. For local and intermediate wires, one transition per clock cycle is assumed, which is a typical behavior for wires carrying logic signals. In the case of global wires, two values of duty ratio are calculated: one assuming a single transition (logic signals) and another assuming two transitions (clock signals) per clock cycle.

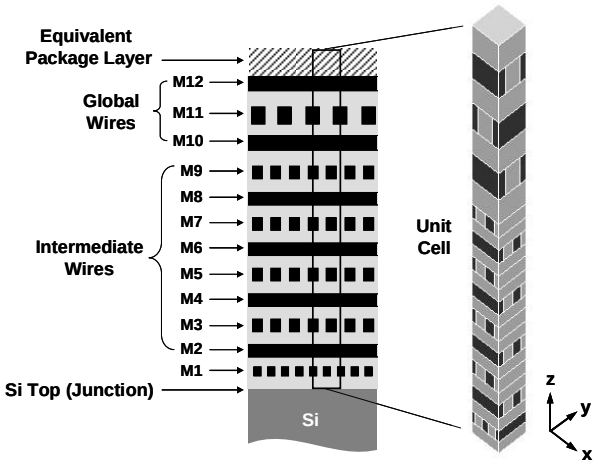

Fig. 7. FEM simulation geometry (unit cell) representing the periodic multilevel interconnect structure (45 nm technology node example).

Tech Node	90 nm	65 nm	45 nm	32 nm	22 nm
Local	0.016	0.034	0.040	0.041	0.044
Intermediate	0.132	0.158	0.175	0.182	0.180
Global (logic)	0.144	0.194	0.213	0.212	0.222
Global (clock)	0.287	0.387	0.427	0.424	0.445

Table 1. Metal level and technology dependent duty ratios.

Interconnect Temperature Scaling Trends

Temperature contours within the orthogonal multilevel interconnects are obtained using fully coupled 3-D electrothermal FEM simulations. Each simulation is composed of two different cases depending on the duty ratios for global wires: (i) all global wires carrying clock signals and (ii) all global wires carrying logic signals. Figure 8 plots the spatial chip temperature distributions along the vertical distance from the Si junction (z=0) to the topmost global wires for the case with clock global wires. For the current

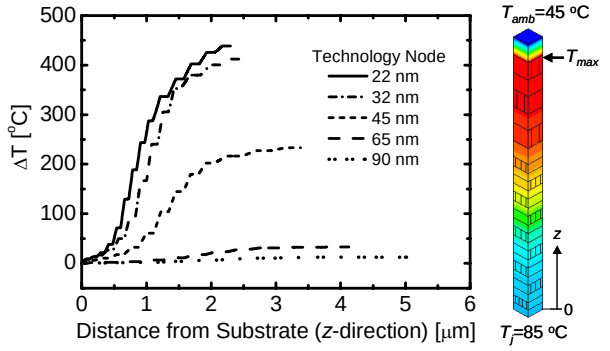

Fig. 8. Temperature rise with respect to the junction temperature ($\Delta T=T-T_j$) along the vertical distance from the Si junction (along the z-direction) for the case with clock global wires. The temperature contour plot of 45 nm technology node is shown as an example. The metal-level and technology dependent duty ratios are used.

technology node (90 nm node), the temperature rise within the interconnect stacks is less than 15 °C. However, metal temperatures increase significantly beyond 45 nm node due to the combined effects of increasing metal resistivity, increasing current density, and decreasing ILD thermal conductivity. Note that the total thickness of the (Cu+ILD) layers decreases as scaling continues, due to the smaller vertical dimensions of wires and insulators despite increasing number of metal levels. For the case with logic global wires that have smaller duty ratios and larger I_{rms} values, the temperature rises are found to be 18-107 % higher than those with clock global wires.

The maximum metal temperature (T_{max}) occurs at the topmost global wires as shown in Fig. 8. Figure 9 shows a plot of the maximum metal temperature rise with respect to the junction temperature ($\Delta T_{max}=T_{max}-T_j$) for different current stress conditions. The predictions for ΔT_{max} by using technology and metal-level and technology dependent duty ratios are compared with those by using a single constant duty ratio for all wires. For the case with the scaled duty ratio, the average values of ΔT_{max} are plotted with error bars based on two different simulations for global wires (clock and logic). It is shown that using an arbitrary duty ratio for all wires can result in significant underestimation or overestimation of ΔT_{max}. Even considering densely embedded vias, the ΔT_{max} increases rapidly with scaling beyond 45 nm node, reaching ΔT_{max}=672±165 °C at 22 nm node. We found that FEM simulations using temperature-independent resistivity values at T_j yield much lower temperature rises (ΔT_{max}=340±43 °C at 22 nm node), which indicates that the temperature-dependent

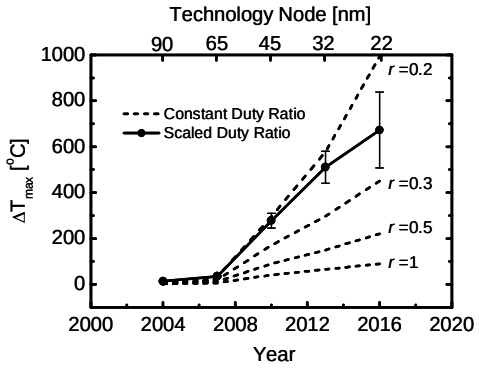

Fig. 9. Impact of duty ratio scaling on ΔT_{max}.

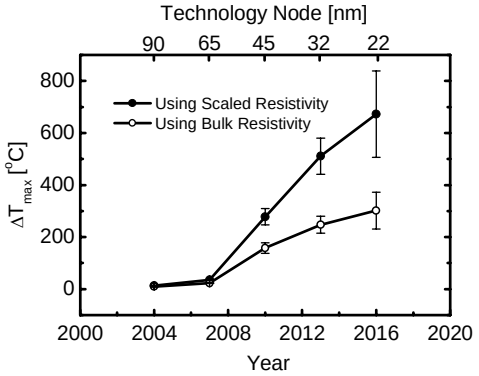

Fig. 10. Impact of resistivity scaling on ΔT_{max}. Note that the temperature dependency of resistivity is considered for both cases.

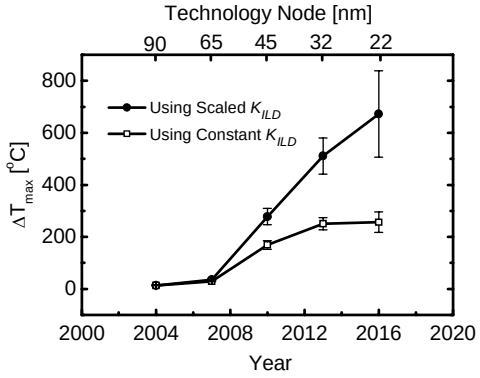

Fig. 11. Impact of ILD thermal conductivity scaling on ΔT_{max}. For constant K_{ILD}, the value at 90 nm node, 0.4 W/(m-K), is used for all technology nodes. Note the fully scaled temperature- and size-dependent resistivity values are used here.

electrothermal simulation is necessary for accurate estimates of multilevel interconnect temperatures.

If the metal resistivity increase associated with surface scattering, grain boundary scattering, and barrier layer effect is neglected, ΔT_{max} in sub-50 nm Cu interconnects can be significantly underestimated (Fig. 10). If the size-independent bulk resistivity (ρ_o) values are used for all technology nodes, ΔT_{max} remains less than 302±71 °C. Similarly, if the ILD thermal conductivity is not properly scaled with the dielectric constant, ΔT_{max} can also be underestimated (Fig. 11), yielding ΔT_{max}=257±39 °C at 22 nm node.

Conclusions

In conclusion, a rigorous scaling analysis of multilevel interconnect temperatures in high performance ICs has been performed using 3-D electrothermal FEM simulations. A methodology for extracting the correlation of thermal conductivity and dielectric constant of low-k materials has been presented based on fully physical models. In addition, an accurate thermal model has been proposed to account for the thermal impact of vias. The comprehensive scaling analysis based on fully coupled technological, structural and material factors has showed that the maximum interconnect temperature rise is expected to be about 300-700 °C in sub-50 nm interconnect technologies. It has been shown that the interconnect Joule heating problem will become more severe due to increasing metal resistivity and decreasing ILD thermal

conductivity if other variables follow the ITRS scaling rules. While the surface scattering is an inevitable consequence of wire dimension scaling, the grain boundary scattering could be reduced by engineering the grain boundary density and impurity enrichment in the grain boundaries by modifying processing conditions. Developing non-porous low-k dielectric materials with higher thermal conductivity and considering optimal density thermal vias during the early design phase might be other solutions to achieve lower interconnect temperatures.

Appendix

ITRS based simulation parameters

		Technology Node [nm]				
		90	65	45	32	22
Wire Width [nm]	M1	107	76	54	38	27
	Intermediate	137.5	97.5	67.5	47.5	32.5
	Global	205	145	102.5	70	50
Wire Height [nm]	M1	181.9	129.2	97.2	72.2	54
	Intermediate	233.75	175.5	121.5	90.25	65
	Global	430.5	319	235.75	168	125
Wire Spacing* [nm]	M1	107	76	54	38	27
	Intermediate	147.83	105.17	76.5	53.83	39.5
	Global	223	159	113.5	82	58
ILD Thickness [nm]	M1**	181.9	129.2	97.2	72.2	54
	Intermediate	206.25	156	108	80.75	58.5
	Global	389.5	290	215.25	154	115
Number of Metal Levels	Total	10	11	12	12	14
	M1	1	1	1	1	1
	Intermediate	7	8	8	8	8
	Global	2	2	3	3	5
$\rho_{eff}(T_j)$* [μΩ-cm]	M1	3.26	3.50	3.88	4.44	5.19
	Intermediate	3.08	3.24	3.57	4.00	4.66
	Global	2.88	2.97	3.15	3.44	3.81
Thermal Conductivity* [W/(m-K)]	K_{ILD}, K_{IMD}	0.40	0.30	0.21	0.16	0.12
	$K_{ILD,eff}$ (min)	0.44	0.34	0.25	0.20	0.16
	$K_{ILD,eff}$ (max)	10.66	10.56	10.80	10.70	11.03
	$K_{U,eff}$	2.57	1.86	1.70	1.58	1.41
Barrier Thickness [nm]		10	7	5	3.5	2.5
k_{ILD} (bulk)		2.7	2.4	2.1	1.9	1.7
J_{max} [MA/cm^2]		0.5	1.0	3.0	4.3	5.8
I_{avg} [mA]*		0.161	0.171	0.246	0.184	0.122
T_j [^{o}C]		90	85	85	85	85
T_{amb} [^{o}C]		45	45	45	45	45
A_c [mm^2]		310	310	310	310	310
Solder Bump Pitch [μm]		150	120	100	90	80
Solder Bump Size [μm]		75	60	50	45	40
Number of Solder Bumps***		3072	3072	3840	4224	4416
$R_{th,U}$ [mm^{2}K/W]*		17.51	19.35	17.65	17.09	17.02
$R_{th,eq}$ [mm^{2}K/W]*		7175.54	7177.38	7175.67	7175.11	7175.05

* Calculated from this work using ITRS data.

** The ILD thickness for M1 (PMD thickness) is assumed to be the same as the height of M1.

*** The number of chip I/Os (number of total chip pads) for MPU.

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