# Teaching Microelectronics in the Silicon ICs Showstopper Zone: a Course on *Ultimate Devices and Circuits: Towards Quantum Electronics*

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**Abstract–This paper reports on a new course introduced at the Swiss Federal Institute of Technology Lausanne, Switzerland and dedicated to advanced devices with high potential for future silicon ICs. The course is intended to familiarize students from Electrical Engineering with possible future evolutions in microelectronics and moreover, eliminate the psychological wall towards the field of quantum electronics.**

## 1 Introduction

The present minimum feature size (130-180nm) in silicon integrated circuits (ICs) is expected to be decreased largely below 100nm (around 30-50nm) until 2014, according to the SIA's National Technology Roadmap for Semiconductors (see Table. 1). It follows that by that time nowadays CMOS devices and circuits will approach their physical and functional limitations that are foreseen for the 10nm dimension. The quantum effects, presently neglected in carrier transport, are expected to be then critical issues. This zone of device dimensions is placed under a *no known solution and high risk* label and should become a highly fascinating field of research for Universities.

Recently, Single Electron Devices (SEDs) have come to be considered as promising candidates for future ultra-low power and high-density integrated circuits, independently or by co-integration with CMOS, [1-10]. Their potential for ultra-low power is related to an operation based on only few electrons. The term Single Electron Transistors (SET) has been selected for devices sensitive to the manipulation of a single electron even if the device itself requires in fact few electrons. It appears much more realistic to address the related electronics by the term *Few-Electron Electronics*, which is currently used for one of the EPFL's research project dedicated to such devices.

Table 1: Technology generation predictions extracted from the International Technology Roadmap for Semiconductors (ITRS).

| Year | 1999 | 2002 | 2005 | 2008 | 2011 | 2014 |
|---|---|---|---|---|---|---|
| Technology generation (μm) | 0.18 | 0.13 | 0.10 | 0.07 | 0.05 | 0.035 |
| Equivalent gate oxide thickness (nm) | 1.9-2.5 | 1.5-1.9 | 1-1.5 | 0.8-1.2 | 0.6-0.8 | 0.5-0.6 |
| Supply voltage desktop (V) | 1.5-1.8 | 1.2-1.5 | 0.9-1.2 | 0.6-0.9 | 0.5-0.6 | 0.3-0.6 |
| Substrate diameter (mm) | 200 | 300 | 300 | 300 | 300 | 450 |
| MPU logic transistor density ($cm^{-2}$) | 6.6M | 18M | 44M | 109M | 269M | 664M |

## 2 The structure of the course

Taking into account that *few-electron electronics* is expected to be a serious candidate for the 21st century microelectronics, some years ago, EPFL's Electronics Laboratory has started to investigate SED architectures and their potential IC applications in collaboration with key teams in USA (Stanford University and USAF) and France (LETI-CEA, Grenoble). Our efforts have been concentrated on two major directions: (I) room temperature operated, few-electron memory architectures (under the MEMOWIRE research project) and (II) hybrid CMOS-SET co-integration for realistic ICs applications.

The research activity under these projects provided the idea of a new course that has been introduced starting 2001/2002. The content of the course is essentially dedicated to prepare engineers for the 21st century microelectronics, familiarize them with nano-electronic issues and future possible applications of few-electron devices. Some basic goals of this new course have been defined as following:

- Comprehension of ultimate limitations of microelectronic devices: physical and technological,
- Understanding deep sub-micron (<70nm) novel innovative CMOS device architectures, their modeling, performance and foreseen limitations,
- Be able to qualitatively and quantitatively describe the functionality of few-electron devices (single electron transistor and memory, quantum wires, etc),
- Understand the functionality of quantum logic cells.

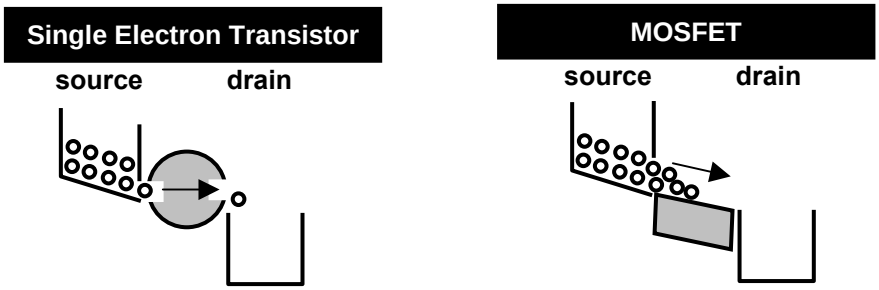
The new course is specially designed for students in the last year of studies in Electrical Engineering in our University (with a possible extension in the EPFL's Doctoral School in Microsystems and Microelectronics) and has the following structure:
*Chapter 1*: Ultimate CMOS technologies and their showstoppers
*Chapter 2*: Phenomena specific to deep sub-micron devices: (I) non-stationary phenomena (velocity overshoot), (II) ballistic transport, (III) quantum effects, (IV) atomic scale parameter fluctuation (fluctuation of number of doping atoms, interface roughness, etc)
*Chapter 3*: Innovative sub-micron device architectures: Double-gate MOSFET – DGMOSFET, dynamic threshold MOSFET – DTMOSFET, Gate-All-Around transistor – GAA, vertical MOS transistors
*Chapter 4*: Nano-scale and quantum devices such as: Single Electron Transistor (SET), quantum wires and single-electron memories (SEM)
*Chapter 5*: Hybrid SET-FET circuits and their possible applications
*Chapter 6*: Novel circuit architectures: quantum dot cellular automata.

The structure of the course reflects some present evolutions in nano-electronics and is projected to be yearly updated with last research developments. An extensive number of references are recommended to the students for more insights as well as more individual work is required compared to other courses. The course structure will be optimized according to the perception and feedback received from students.

## 3 Single Electron Transistor and its applications

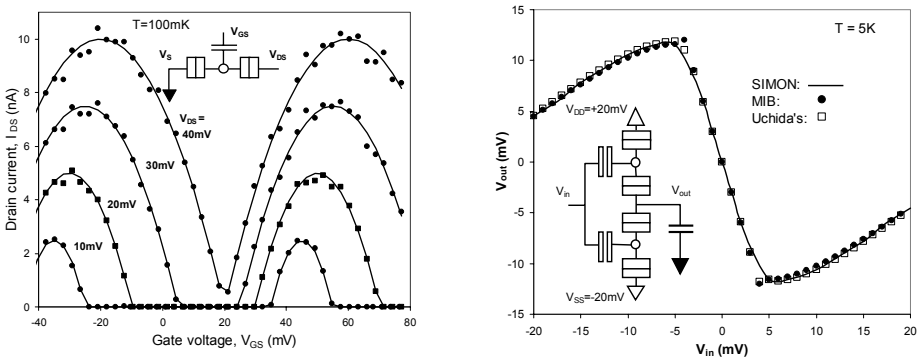
The operation principle of a Single Electron Transistor is suggested in Fig. 1: the electrons are transferred one-by-one (in contrast with conventional MOSFET) due to its particular architecture that includes two tunneling junctions and one conductive island (for a detailed description see [7]). A remarkable characteristic of SET is the Coulomb

blockade phenomenon, resulting in non-conventional (compared to MOSFET) $I_D$-$V_D$ and $I_D$-$V_G$ characteristics (Fig. 2a). However, it's still possible to built a functional SET inverter (Fig. 2b), the characteristics of which are similar with CMOS inverter.



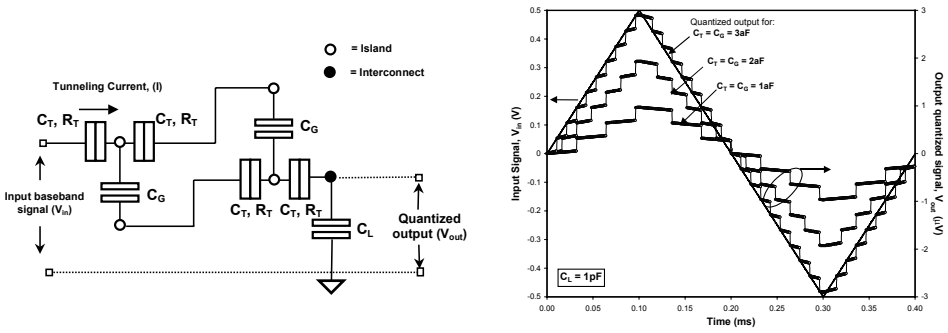

(a) (b)

Fig. 1: Transfer of electrons is (a) one-by-one in Single Electron Transistor (SET), which is in contrast with (b) conventional MOSFET where many electrons simultaneously participate to the drain current (after Uchida et al. [11]).




(a) (b)

Fig. 2: (a) Periodical, parabolic-shaped, $I_D$-$V_{GS}$ characteristics of SET are still able to provide a quasi-conventional behavior of the transfer characteristic of SET inverter (b). Plots are simulated with Monte-Carlo simulator SIMON and also with Uchida [12] and MIB [13] analytical models.




(a) (b)

Fig. 3: (a) A SET-based quantizer for hybrid SET-CMOS communications applications [15]: $C_G$ and $C_T$ are the gate and tunnel capacitance, $R_T$ is the tunnel resistance and $C_L$ is the load capacitance ($C_L >> C_G$, $C_L$) and (b) Effect of device capacitance on the sampling rate of the quantizer working at T=100mK, for three values of device capacitance (1aF, 2aF and 3aF).

Critical issues of SETs are low temperature operation, high output impedance and low drain voltage operation. Their key advantages are the very low power and the high scalability. Only a very few qualified SET technologies have been reported.

Recent studies have also shown that SET could be interesting for some other niche applications except logic circuits. One example is the CMOS-SET hybrid [14] or pure-SET *quantizer*, dedicated to communication applications [15] (Fig. 3). One more obstacle to investigate in detail the CMOS-SET hybrid applications originates in the lack of available hybrid (SET-CMOS) simulators and in poor 'engineering' approaches dedicated to the modeling, characterization and simulations of SET.

## 4 Conclusion

Last year's tremendous progress in microelectronics has pushed the device dimensions towards limits that are expected to impact the basic, well-established working principles of MOSFETs. In the next future it is then probable that MOSFETs will need to share their domination on modern ICs with new device architectures, using a few of electrons, like Single-Electron Transistors. The authors are aware about the fact that there is still a *long* way to run for Single Electron Devices in order to make major progress, be accepted and especially, be used by the IC community. Understanding and teaching *few-electron electronics* principles can help for a more friendly welcome and a deeper understanding of SED usefulness by new generations of engineers.

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