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LEAKAGE AND VARIATION AWARE THERMAL MANAGEMENT OF NANOMETER SCALE ICS

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***Abstract*—For sub-100 *nm* CMOS technologies, leakage power forms a significant component of the total power dissipation, especially due to within-die and die-to-die variations in process (P), temperature (T) and supply voltage (V). Since leakage power and operating temperature are *electrothermally* coupled to each other, increasing power dissipation and thermal problems are becoming key concerns not only from a thermal management point of view but also because most reliability mechanisms are highly temperature sensitive. This paper provides an overview of a novel methodology for making temperature and reliability aware power/performance/cooling-cost tradeoffs in leakage dominant nanometer scale high-performance ICs. First, a framework to accurately estimate subthreshold leakage under both within-die and die-to-die parameter variations is outlined. It is shown that die-to-die temperature variations can significantly increase leakage power, mainly because of electrothermal couplings between power and temperature. Next, a recently developed *self-consistent* electrothermal methodology to accurately estimate the junction temperature is presented and is shown to be significant for thermal management of leakage and variation dominant CMOS technologies. The methodology is then applied to provide a reliability and thermally aware *design space* that can be used to optimize and compare various designs.**

***Index Terms*—cooling, electrothermal couplings, packaging, process variation, reliability, self-consistent methodology, subthreshold leakage, temperature variation, thermal management, voltage variation.**

I. INTRODUCTION

For nanometer scale VLSI technologies, power dissipation and thermal management have been identified as key factors for the design of high performance ICs (including microprocessors) by leading semiconductor manufacturers and by the International Technology Roadmap for Semiconductors [1]. Leakage power, which is rapidly becoming the dominant contributor to the total chip power, is strongly affected by technology (device) scaling and on-chip process, temperature and voltage variations that are rampant in sub-100 nm technologies. Furthermore, subthreshold leakage power, which is the dominant leakage source for high-performance ICs [2], increases exponentially with die (junction) temperature. The die temperature in turn, is determined by the total chip power dissipation and system packaging/cooling technology. As a result of this strong coupling between die temperature and leakage power, technology scaling and parameter variations are beginning to impact thermal management and performance optimization solutions in high-end ICs in a way that previous generations did not. Additionally, both leakage power and temperature have significant implications for IC reliability.

In this paper, we discuss the increasing impact of device scaling and increasing parameter variations on the leakage power dissipation in nanometer scale CMOS ICs and then analyze its implications for thermal management issues including packaging and cooling solutions. Most importantly, we highlight a recently developed system-level electrothermal (ET) analysis methodology and tool [3] that allows accurate estimation of the strongly coupled junction temperature in leakage dominant technologies. The ET-tool can be applied to establish design windows for various power-performance-reliability-cooling cost tradeoffs in high-performance ICs including microprocessors and to evaluate various packaging and cooling solutions for optimizing chip performance.

The paper is organized as follows. Section II presents a framework to estimate subthreshold leakage power considering both within-die and die-to-die parameter variations. In Section III, the electrothermal couplings between leakage power and temperature are shown to have significant impact on junction temperature estimation as well as on packaging and cooling costs. In order to comprehend various electrothermal couplings for thermal management, a self-consistent electrothermal methodology is presented in Section IV. Impact of applying the self-consistent electrothermal methodology on thermal management solutions is discussed in Section V. In Section VI, we formulate a fully analytical and thermally self-consistent energy-delay product (EDP) based V_{dd}-V_{th} evaluation methodology to provide a reliability and thermally aware design space. Finally, concluding remarks are made in Section VII.

II. IMPACT OF TRANSISTOR SCALING AND PARAMETER VARIATIONS ON LEAKAGE POWER

Due to relentless push for high performance and high integration density, power density and on-chip temperature in VLSI circuits have been rising steadily [4]–[9]. The increasing power trend for Intel's microprocessors is shown in Fig.1. Circuit blocks with such higher power densities give rise to higher temperatures and create local hotspots on the substrate. The resulting higher on-chip temperatures can drastically increase leakage power because of its exponential dependence on temperature.

Apart from high temperatures, within-die and die-to-die parameter variations can also result in higher leakage power. Die-to-die parameter variations which result from lot-to-lot, wafer-to-

wafer and a portion of within-wafer variations impact every element on a chip equally. On the other hand, within-die parameter fluctuations consisting of both random and systematic components produce non-uniformity of electrical characteristics across the chip. Within-die parameter variations can be divided into two parts: environmental variations (temperature (T) and power supply (V)) and physical variations which include all process (P) variations. Process variations can be further divided into *extrinsic*: variations in channel length, oxide thickness, interconnect width and thickness, inter-metal layer dielectric thickness, contact and via sizes and *intrinsic*: random fluctuations of dopant atoms in the channel of the MOSFET device.

Parameter variations discussed above have been shown to cause 20X variations for a 180 *nm* technology node resulting in wide spread in the distribution of leakage power [4]. Thus designing with the worst case leakage values may result in excessive guard banding while underestimating the leakage might result in highly optimistic designs. Therefore, in the present scenario, probabilistic modeling is more meaningful in comparison to a deterministic analysis. In a recent work [10], we introduced a probabilistic framework for accurately estimating full-chip subthreshold leakage power distribution under within-die and die-to-die P-T-V variations.

As shown in Fig. 2, the gap between polysilicon gate lengths and the wavelength of light used in optical lithographic process is increasing with technology scaling [8], as a result of which, channel length of a MOSFET shows significant amount of variations. Hence, we first estimate the impact of within-die channel length variations on subthreshold leakage. Fig. 3 plots the percentage increase in subthreshold leakage due to within-die channel length variations as a function of spread in channel length for both PMOS and NMOS [10]. The subthreshold leakage for PMOS shows stronger dependence on channel length variations as compared to NMOS because of steeper V_{th}-roll off slope for a PMOS.

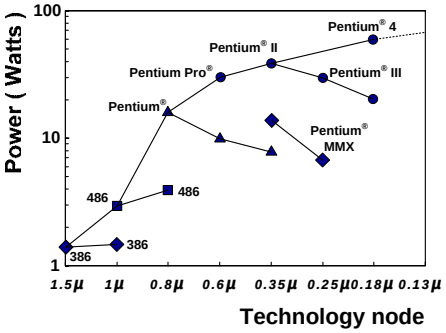

Fig. 1. Power trend in Intel microprocessors [9].

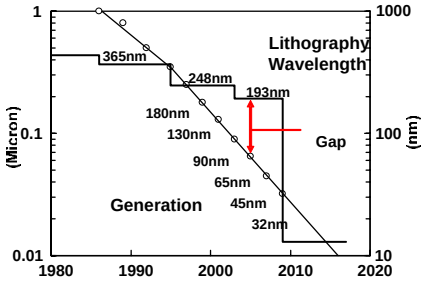

Fig. 2: Increasing gap between polysilicon gate length and lithographic wavelength for different technology nodes [8].

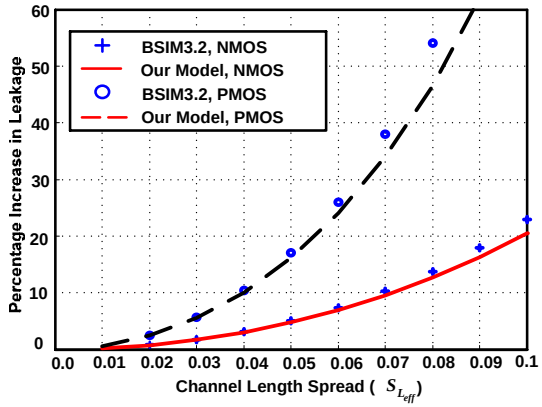

Fig. 3: Percentage increase in subthreshold leakage plotted for different values of $S_{L_{eff}}$ for NMOS and PMOS at 300K [10].

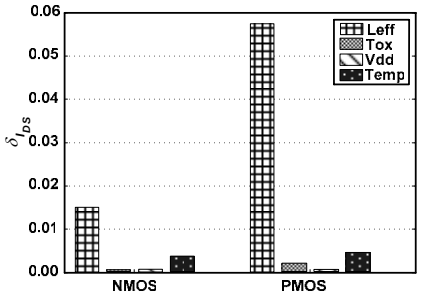

Fig. 4: δ for leakage contributed by different within-die variations for NMOS and PMOS at 300K [10].

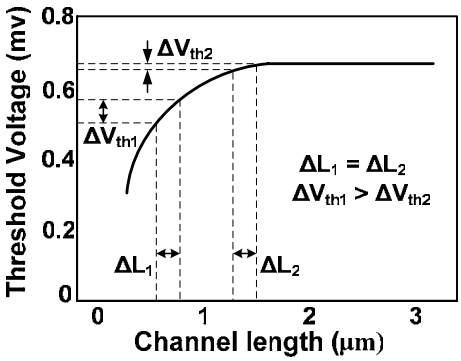

Fig. 5 Schematic for threshold voltage roll-off. With technology scaling, the same amount of channel length variations result in greater variations in threshold voltage.

The relative sensitivities of leakage to different within-die P-T-V variations are shown in Fig.4 [10]. Here $\delta_{I_{DS}}$ is the normalized increase in leakage current and is given by (1), where $\mu_{I_{DS}}$ and $\eta_{I_{DS}}$ are the mean and nominal values of leakage current.

$$\delta_{I_{DS}} = \frac{\mu_{I_{DS}} - n_{I_{DS}}}{n_{I_{DS}}} \quad (1)$$

The above results are derived for the following 3σ variations [1]: channel length (10%), gate oxide thickness (3%), supply voltage (5%) and temperature (5%). As can be seen from Fig. 4, subthreshold leakage is most sensitive to channel length variations since threshold voltage is extremely sensitive to channel length due to V_{th} roll-off, especially for sub-100 *nm* technologies, as shown in Fig. 5.

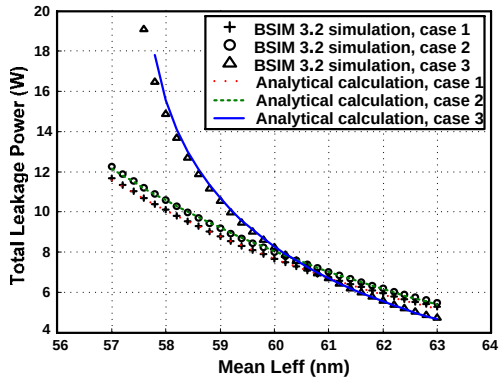

Fig. 6: Total subthreshold leakage power vs. mean die-channel length at die temperature of 320K [10].

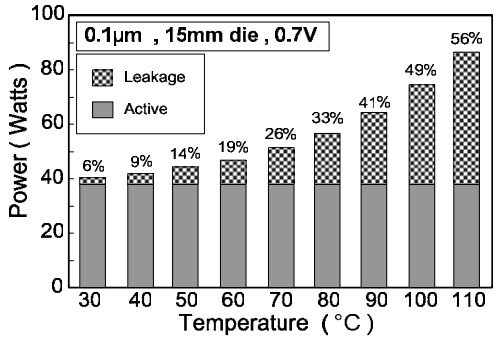

Fig. 7. Temperature dependence of leakage power dissipation for a *100 nm/0.7 V* CMOS technology. The fraction of leakage power component increases superlinearly with temperature.

Apart from within-die variations, die-to-die parameter variations such as channel length and temperature can strongly impact the leakage power. Die-to-die temperature variations are a strong function of total chip power and correlate strongly to within-die variations. Hence, die-to-die temperature variations can be taken into account by self-consistently solving die temperature and total chip power. Die-to-die channel length variations can be taken into account by varying the mean value of channel length for all the transistors across the chip. Fig.6 plots total leakage power for a Pentium M like microprocessor for 3 cases [10].

In case 1, we consider only die-to-die channel length variations. In case 2, apart from die-to-die channel length variations, within-die channel length variations are also considered, while case 3 considers die-to-die temperature variations together with all the variations considered in case 2. It can be clearly observed that die-to-die temperature variations significantly increase the leakage due to the electrothermal couplings between subthreshold leakage power dissipation and die temperature, especially at higher operating temperatures.

III. Implications for Junction Temperature

As mentioned above, due to technology scaling and parameter variations, leakage power dissipation, which is dominated by subthreshold leakage for high-performance ICs, becomes a significant component of total chip power consumption (Fig. 7). Also, subthreshold leakage power dissipation is exponentially dependent on temperature and the dependence gets stronger with scaling (Fig. 8).

Circuit blocks with such higher power dissipation give rise to higher temperatures and create local hotspots on the substrate. Consequently, ICs exhibit significant thermal gradients across the die as shown in Fig.9, which can critically affect performance, power, packaging and cooling costs, especially for high performance microprocessors [11]-[15]. For instance, as illustrated in Fig.10, the average junction temperature T_j, which normally varies approximately linearly with the junction-to-ambient thermal impedance θ_j, increases non-linearly with θ_j, due to the coupling between P_{chip} and T_j, arising primarily due to the exponential dependence of P_{leak} on T_j. Hence, for leakage dominant nanometer scale technologies, in order to maintain a desired value of T_j, a lower value of θ_j will be required, leading to an increase in packaging/cooling costs. The system cooling cost can also be understood using the following equation that relates the thermal impedance θ_j to the chip junction temperature T_j, and the total power dissipation P_{chip}. T_{amb} is the ambient temperature of the chip.

$$\theta_j = \frac{T_j - T_{amb}}{P_{chip}} \tag{2}$$

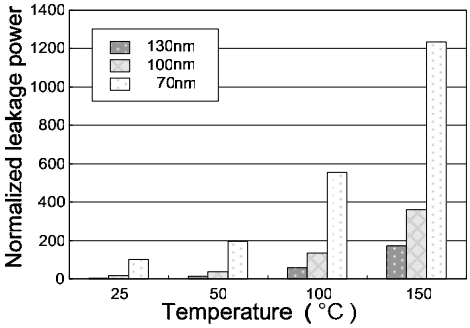

Fig. 8. Leakage power of an *NMOS* device for different technology nodes based on SPICE simulations using BSIM3 models at different temperatures. The leakage power is normalized w.r.t I_{off} at *130* nm node at *25 °C*.

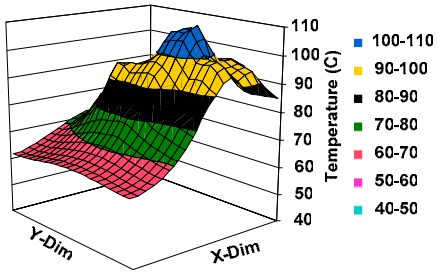

Fig. 9. Die-temperature map for high performance microprocessors [9].

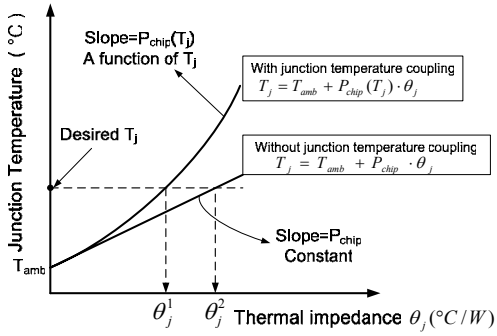

Fig. 10: Schematic diagram illustrating the dependence of junction temperature on the chip-to-ambient thermal impedance for *typical* and *self-consistent* power estimation methods.

From equation (2), it can be observed that a larger junction-to-ambient temperature difference allows a smaller heat sink and air flow rate (i.e., larger θ_j and smaller system cooling cost) for dissipating the same power. Reduction in θ_j will increase the packaging and cooling cost rapidly. Hence, in general, maintaining larger T_j relaxes θ_j requirements in an *active power* dominated technology. However, for technologies that are *leakage dominant*, larger T_j will impact P_{leak} (Fig. 8), and hence the total power P_{chip}, and thereby influence θ_j and the cooling cost.

Fig. 11 summarizes the details of the various electrothermal couplings between supply voltage (V_{dd}), threshold voltage (V_{th}), frequency, power dissipation and junction temperature (T_j). Power dissipation has two major components: switching power and leakage power dissipation. The switching power dissipation increases as the chip frequency increases with an increase in supply voltage. Moreover, the frequency itself is dependent on temperature due to the dependence of the transistor on-current (I_{on}) on T_j. Also, T_j has two counteracting effects on I_{on}: a) increase in I_{on} due to lowering in threshold voltage at increased T_j, and b) decrease in I_{on} due to reduction in mobility at higher T_j [16]. Furthermore, as mentioned earlier, subthreshold leakage power dissipation, the major contributor to leakage power, is exponentially dependent on temperature.

Hence, in order to accurately estimate junction temperature and comprehend various electrothermal couplings for thermal management, a self-consistent electrothermal analysis method is highly desirable for leakage dominant nanometer scale technologies, as discussed in the next section.

IV. Self-Consistent Electrothermal Methodology

The self-consistent electrothermal methodology uses analytical models based on an integrated device, circuit, and system level modeling approach [3] and has been summarized in Fig. 12.

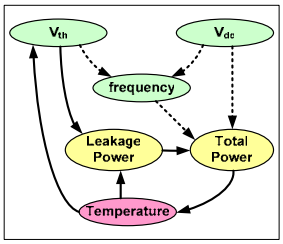

Fig. 11. Schematic view of electrothermal couplings between different design parameters.

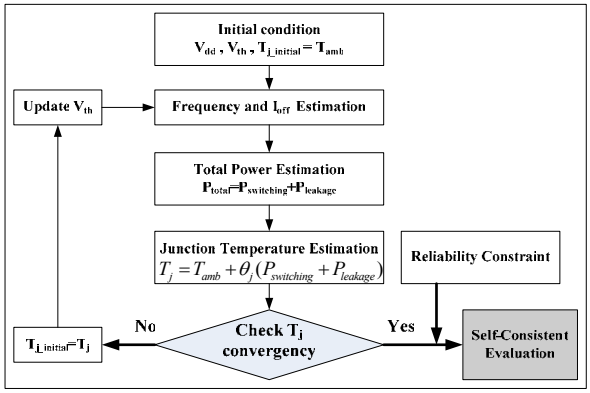

Fig. 12. An overview of the self-consistent electrothermal methodology. The methodology has been implemented as an automated computer program.

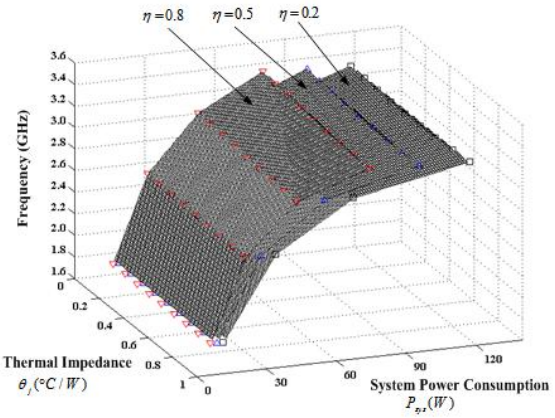

Fig. 13. Design guidelines for integrated packaging and cooling solutions.

For a given V_{dd}, V_{th} and initial T_j (we use ambient temperature as an initial value), the operating frequency and the total leakage current (I_{off}) of the chip are first estimated. The estimated frequency is then used in the calculation of the switching (active) power. Also, the leakage power can be estimated using I_{off}. For our analysis, nominal value of I_{off} was calibrated against measured data at ambient temperature. The total chip power is then used to calculate the new junction temperature using compact thermal models for a specific IC packaging and cooling technology.

The estimated junction temperature is then compared with the initial value of T_j to check for convergence. Also, due to the strong dependence of temperature on threshold voltage, the estimated junction temperature is used to update threshold voltage for every iteration. The process continues till a convergence in the value of T_j is achieved. However, if the value of T_j is not acceptable (too high for a chip) or there is no convergence within reasonable iterations, error messages will be generated, which would invalidate T_j. Besides, a chip-level reliability constraint is also applied to check the validity of the estimated value of T_j for the particular value of V_{dd} used in the analysis.

V. Implications for Thermal Management

By applying the self-consistent electrothermal methodology, various electrothermal couplings between supply voltage, threshold voltage, frequency, power dissipation, packaging and cooling cost can be taken into account. Since the coupling between P_{chip} and T_j (primarily due to the strong dependence of $P_{leakage}$ on T_j), where the latter will be limited by $P_{leakage}$, which cannot increase unbounded due to the constant system power constraint, the methodology would allow designers to avoid employing overly conservative design rules and thereby improve performance. Fig. 13 illustrates how design guidelines can be generated for efficient thermal management of high-performance ICs. Such plots can be used for the selection of various packaging and cooling solutions (corresponding to values of θ_j, cooling efficiency, η and P_{sys}) to get optimum performance and also comprehend the diminishing returns of employing an expensive thermal management system. For example, for the microprocessor used in this study, a maximum frequency of ~3.4 GHz will be obtained even with η =0.8 and θ_j =0.2 ^{0}C/W along with $P_{sys} \approx$ 75 W [3].

VI. Implications for Circuit Design and Reliability

Since power dissipation directly impacts the junction temperature, it is desirable to scale supply voltage (V_{dd}) to reduce active power consumption. Although, scaling V_{dd} will degrade the performance of the circuit, it can be partially compensated by lowering threshold voltage (V_{th}) at the cost of increased leakage power. Thus, for applications, where both performance and amount of computation that can be done for a given energy budget are of importance, energy-delay product (EDP) is an appropriate metric to optimize and compare different designs [17].

Fig. 14 has been generated simply by evaluating energy and delay for a 32-bit microprocessor using the alpha-power law model [18], and shows the operation region containing the iso-performance curves, and contours of the inverse of the relative EDP. The relative EDP can be found by normalizing with respect to the value of the EDP at the optimal point (minimum EDP, denoted by "Δ"). For instance, any point on the curve labeled 0.5 has double the EDP value of the optimal point, i.e., the minimum value. The numbers on the iso-performance curves indicate the normalized value of the frequency where normalization is done with respect to the frequency of operation at the optimal point. Here, note that the entire space is allowed for the design except the region below the $V_{dd} = V_{th}$ line.

However, as mentioned above, leakage power is strongly dependent on the junction temperature. Also, V_{th} is a function of temperature, which in turn, depends on total power dissipation. Traditional EDP evaluation neglects these couplings indicated by solid arrows in Fig. 11. Also, system reliability is directly related to the operation temperature. For instance, reliability mechanisms such as electromigration (EM) and time-dependent gate-oxide breakdown (TDDB) are known to have an inverse exponential dependence on temperature [19]-[22]. Therefore, it is crucial to generate a reliability and thermal aware design space for evaluating various power-performance-reliability tradeoffs and also for comparing different circuit designs under different reliability constraints.

Following the methodology described in section IV, a self-consistent evaluation of energy-delay and performance are obtained as shown in Fig. 15 [23]. It can be observed that not only the EDP contours and iso-performance curves shift but also the design space gets restricted by thermal constraint that cannot be known from Fig. 14. In order to highlight the importance of applying self-consistent electrothermal methodology with technology scaling, Fig. 16 shows the reduction of allowable design space with increasing I_{off}. It can be clearly observed that with increasing leakage, the region prohibited due to thermal runway expands, thus restricting the allowable design space. Moreover, the significance of applying this methodology is expected to increase when parameter variations such as process, supply voltage and temperature variations are also taken into account since they are known to increase subthreshold leakage significantly.

Fig.17 plots the junction temperature vs. V_{dd} for $I_{on}/I_{off} = 220$, and illustrates the impact of using the self-consistent approach on satisfying chip-level *iso-reliability* constraint ($V_{dd} \le V_{max}=T_j.R+c$, c is a constant and R represents a chip-level reliability factor with typical value of -3mV/^{0}C) [3]. It can be observed that for V_{dd}>1.1V, the non self-consistent method predicts lower values of T_j and hence, higher maximum allowable V_{dd} values (determined by the intersection of the curves with the iso-reliability line) and would therefore degrade the reliability of the chip.

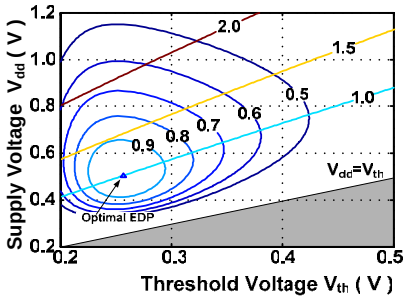

Fig. 14. Contours of constant energy-delay-product (EDP) and iso-performance curves that do not comprehend any thermal and reliability constraints.

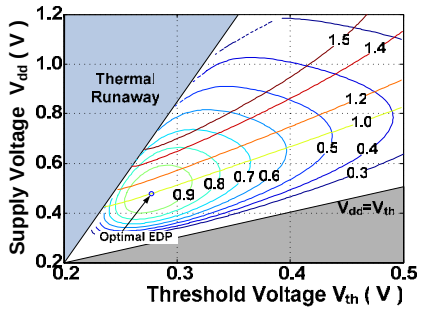

Fig. 15. Contours of constant energy-delay-product (EDP) and iso-performance curves considering thermal constraint. The design space gets restricted by thermal constraint (thermal runaway) when various electrothermal couplings are considered in a self-consistent manner.

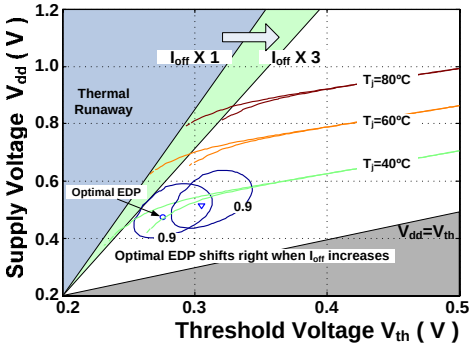

Fig.16. Impact of technology scaling on design space. While the leakage increases due to technology scaling or process variations, the operation region prohibited by thermal runaway expands.

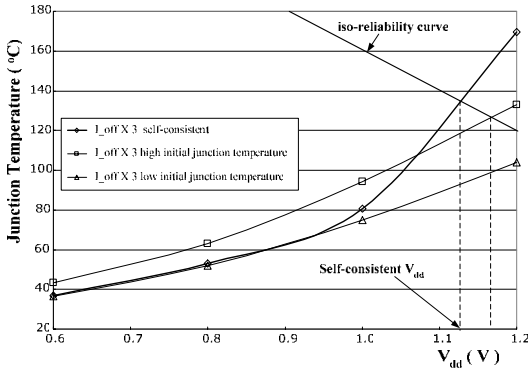

Fig.17. Implications of self-consistent approach on satisfying chip-level reliability constraints.

Furthermore, we have recently quantified the impact of off-state leakage on EM design rules for both unipolar and bipolar stress conditions [24]. It has been shown that for a given system power dissipation, consideration of various electrothermal couplings in subthreshold leakage dominant technologies can lead to lower estimated junction and metal temperatures, which in turn lead to more accurate estimation of EM lifetime. This would allow designers to avoid employing overly conservative design rules and thereby improve performance. These results will also have important implications for burn-in testing of leakage dominant ICs.

VII. Conclusion & Future Work

In conclusion, we highlighted the growing impact of device scaling and parameter variations on leakage power and subsequent implications for junction temperature and thermal management. A probabilistic framework for accurate analysis of the impact of within-die and die-to-die P-T-V variations on subthreshold leakage has been developed. It was shown that die-to-die temperature variations can significantly impact subthreshold leakage power, especially due to electrothermal couplings between power and temperature. Furthermore, a self-consistent methodology that comprehends various electrothermal couplings between supply voltage, threshold voltage, frequency, power and temperature has been developed for accurate estimation of the junction temperature. The electrothermal tool can be applied for making various power/performance/reliability/cooling-solutions tradeoffs in leakage dominant nanometer scale CMOS technologies, and to optimize the performance of ICs. It can also be used to generate a reliability and thermally aware *design space*.

As discussed in Section III, ICs exhibit thermal gradients across the die. Our proposed self-consistent electrothermal methodology is now being extended to capture the spatial temperature profiles across high-performance chips. Based on power distribution map and placement information, the chip can be divided into several suitable blocks (within which the temperature remains invariant), and then the self-consistent electrothermal methodology can be applied along with a full-chip thermal diffusion analysis for obtaining the temperature distribution across the chip. Consequently, system level tradeoffs between packaging, cooling, and reliability can be achieved based on more accurate thermal map of a chip.

Acknowledgement

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