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Modeling and Extraction of Nanometer Scale Interconnects: Challenges and Opportunities (Invited)

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ABSTRACT

We discuss interconnect parasitic extraction in the nanometer domain using the ITRS 2005 roadmap for future technology generations. Resistance becomes the dominant contribution for timing for local wires at 65 nm and beyond, a major qualitative change. For scaled wires, maintaining global wire routes within 1 clock period is expensive in terms of power consumption. An acceptable solution involves reverse scaling of global wires leading to RLC transmission line behavior which results in significant power savings. RLC transmission for scaled signal wires is otherwise negligible.

INTRODUCTION

The traditional gains in microprocessor performance with every technology node slowed down considerably in the transition from 130 to 90 nm. Latest developments at 65 nm node, however, show signs of recovery from this slowdown: Intel announced the Xeon server Tulsa processor, packing 1.3 billion transistors with an expected clock at 3.4 GHz and consumption at 150 watts [1], while IBM's recent Power6 processor chip [2], is clocked at 5.6 GHz (13 FO4 design – see Section IV).

The representative size of layout database for chips of the complexity mentioned above is O(100 Gbytes). With O(N) transistors, and a comparable number of wires, the number of possible electromagnetic couplings is $O(N^2)$. Since the computational cost of analyzing such a large number of electromagnetic interactions is prohibitive, filtering while doing extraction is mandatory so that such interactions are considered only where necessary. However, the challenge while filtering such a large number of wires is to minimize the unwanted side effects on critical timing and noise simulation.

The interconnect wires can be treated as a collection of lumped resistance (R), inductance (L) pairs, coupled via mutual capacitance (C_{ij}) and mutual inductance (M_{ij}) elements. Modelization of these elements must enforce locality of electromagnetic interactions. Beyond a certain distance, *individual* couplings become negligible. Long distance interactions (C_{ij} or M_{ij}) must be replaced by multipole expansion coefficients accounting for collective effects [3]. The total number of local electromagnetic parameters is O(N), significantly smaller than $O(N^2)$. However powerful this reduction is, it remains insufficient for timing simulation since the input file increases by 2 orders of magnitude after incorporating local parasitic data. Model Order Reduction (MOR) [4] must be applied to the resulting parasitic netlist which includes the parasitic resistance, inductance and capacitance elements. Two extra orders of magnitude decrease in data can be gained with controllable impact on accuracy.

Besides the sheer complexity of parasitic extraction data, interconnect parasitic extraction in the nanometer scale faces the additional challenge of new phenomena such as increased variability of interconnect parameters [5] (due to CMP, lithography, temperature, and surface scattering induced variations) and high frequency signal transmission (beyond 100GHz at the 32 nm node with CMOS

gates). The effects of these phenomena will have to be incorporated in parasitic extraction for accuracy and predictability. We examine some opportunities for high frequency signal transmission for unscaled global wire usable for global communications and RF.

In Sections I, II and III we separately and summarily describe the extraction of *R*, *C* and *L*, respectively. In IV we present conservative projections regarding the maximum expected frequencies. Using these projections along with ITRS predictions [6], in V we discuss the resistance and capacitance challenges resulting from increased accuracy requirements for local wires and the power challenges for global wires. In VI we present an opportunity based on unscaled wires for global communication within one clock period. In VII we present our conclusions.

I. Resistance Extraction:

At the lowest level, the parasitic extraction problem comprises extracting *RL* parameters associated with each segment of each wire, as well as the *RLC* parameters characterizing the interactions with other segments.

We review first the problem of wire resistance extraction for nominal parameters. In the Electro-Quasistatic (EQS) regime, for rectilinear conductor segments, with constant resistivity ρ, the resistance is given by: $R = \rho \frac{l}{w.t}$ where *l*, *w*, *t* are the wire length, width and thickness, respectively. Connectivity preservation is the most expensive part of resistance extraction.

Beyond segments, simple formulae exist for corners and T-junctions. Thickness and width are subject to systematic processing variations. These one-dimensional models need to be modified by two-dimensional corrections arising from surface and scattering effects [7], via insertion as well as high frequency skin effects.

II. Capacitance Extraction:

There are no exact expressions for interconnect capacitance, except for the most trivial parallel plate capacitor. For the extraction of capacitance, the purpose is to find the electric charge distribution on the surface of each conductor in the presence of an applied electric field. There are two approaches available for this purpose: Differential and Integral methods. To find the Capacitance matrix, one needs to solve *n* times a linear system, with *n* the number of conductors, wherein each invocation places one wire at V_{dd} and the other (non V_{dd}) wires at zero volt. One-dimensional models (parallel plate capacitance calculations), even with fringe corrections, have been out of fashion for a number of years. Two-dimensional capacitance extraction methods are widely used. The main advantage of two-dimensional models is that the capacitance matrix for a configuration of wires is separable. In other words, the capacitance between two conductors can be computed independent of their neighbors (see, for example, Figure 1, where the capacitance between conductors B and C is independent of conductor A). Moreover, the capacitance between two conductors can be independently parameterized with convenient analytical expressions whose parameters can be adjusted by contrasting these parameterizations to field solvers such as FastCap [8]. This property does not hold in three dimensions: the capacitance between two objects clearly depends on the presence of other objects in the neighborhood. The most favorable approach to deal with three-dimensional capacitance extraction uses a boundary element method.

A simplified approach uses two dimensional models in which the neighborhood is reduced to equal length left and right neighbors and the replacement of top and bottom wires by ground planes. For these configurations separability in the computation of matrix elements is valid, permitting independent modeling of each contribution, thus avoiding matrix inversion. Efficiency rather than accuracy is the goal. For example, a nearest neighbor 2D model often used [9] is:

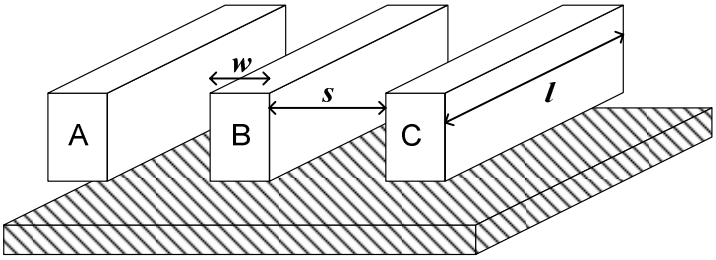

Figure 1: Interconnect schematic showing parameters for capacitance modeling. In 2D, the capacitance between conductors B and C is independent of the conductor A.

$$C_{i,j} = lk_1 w^{k_2} (\exp(-k_3 + k_4 s) + k_5 s^{-k_6}) \tag{1}$$

The coefficients k_i are determined through fits to field solver data, *s* being the separation, and *l* the common length of the conductors.

Such a parameterized 2D modeling approach is friendly for the analysis of systematic process variations. Functional expressions for first and second derivatives with respect to process variables are computationally handy for sensitivity analysis, thus facilitating the incorporation of systematic variations (for example, ILD thickness and conductor separations) to model equations via analytical formulae [10]. However, critical wires must be treated with 3D methods.

III. Inductance Extraction:

Inductance extraction is better described in the frequency domain. As frequency increases, the first manifestations of magnetic behavior on currents arise through the change to the electric field $\vec{E}$. The magnetic field is treated as in Magnetostatics. It is the Magneto-Quasistatic (MQS) regime, Maxwell's and Ohm's laws for a system of conductors lead to the matrix equation:

$$(R + j\omega L)I = \Delta V \tag{2}$$

The matrix elements for *R* and *L* are given by:

$$R_{ij} = \begin{cases} \dfrac{rl}{a_i} & \text{if i = j} \\ 0 & \text{else} \end{cases} \qquad L_{ij} = \frac{\mu_0}{4\pi a_i a_j} \int_{\bar{\Omega}_i} \int_{\bar{\Omega}_j} \frac{\hat{\ell}_i \cdot \hat{\ell}_j}{\|r - r'\|} d\Omega d\Omega' \tag{3}$$

with a_i, $\bar{\Omega}_i$ and $\hat{\ell}_i$ the cross-section area, the volume and the current direction on conductor *i*, respectively, when currents are uniform over the conductor cross-section. Equation (2) is the correct approximation for conductor lengths smaller than the wavelength of light in the medium. When the transverse dimensions become comparable to the skin depth further discretization of the currents into filaments is needed. For rectangular cross section segments, (3) becomes [11]:

$$L = \frac{\mu l}{2\pi} \left[\ln\left(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}} \right) - \sqrt{1 + \frac{d^2}{l^2}} + \frac{d}{l} \right] \tag{4}$$

with *d* the separation (geometric mean distance (GMD)) between the conductors' cross-sections. The task is to solve for the currents in (2). In particular, to obtain the loop impedance of a wire, we include the signal wire plus the collection of ground return paths, and the loop impedance is given by: $I_s^{-1} = Z_{loop}$. On an IC it has been considered difficult to find which wire segments to include as return path. Two approaches are possible: PEEC in which one does not differentiate between signals and grounds and includes them all [12]; the alternative is to identify the local grounds (loop formalism).

Early approaches were of the PEEC type [13]. PEEC and its derivatives (Inverse methods [14]) are computationally expensive: The size of the linear system is of the order of $C = n \times m \times j$, with n number of conductors, m the number of segments per conductor and j the number of filaments per segment. The matrix is dense, and not sparsifiable without side effects [13]. To solve the system demands C^3 operations, making it not scalable beyond simple configurations. Alternatively, within the loop formalism [15] a physical solution to the problem of asserting which ones constitute the return paths is found. It is efficient for all circumstances where inductance effects are important.

In Figure 2, impedance calculations for a global wire configuration with unscaled wires are shown. For low frequencies (under 0.5 GHz in this example) the loop formalism is either inaccurate or computationally expensive. However, low frequency inaccuracies are harmless since the impedance for these frequencies is dominated by the resistance. At higher frequencies solutions are found involving a fixed but not too small number of ground neighbor wires as return candidates [15]. Solving (2), for a reasonable size system, gives the proportion of the total current carried by each ground wire segment. As the frequency continues to increase current distribution within the wires becomes non uniform (skin effect). Both effects are quantitatively accounted for large systems with reasonable performance, generating results in close agreement with Field Solver FastHenry [16] estimates. Beyond its physical relevance, two key advantages of the loop approach are: The computational cost of the loop approach is m times a small and fixed size linear system; and the fall-off of mutual inductance with distance as an inverse power of the separation rather than unrealistic logarithmic behavior of the PEEC method resulting from (4).

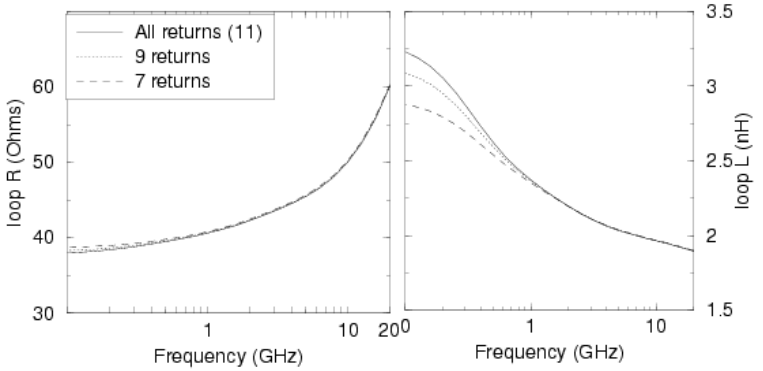

Figure 2: Loop Impedance (resistance and inductance) of 1 signal wire plus 9 closest ground return paths, separate and total contribution. Wire transverse dimensions are unscaled 1 micron widths.

The approach described above is the two-dimensional (2D) approach to impedance extraction (uses same length segments for signal and return wires). Three-dimensional enhancements are easy to incorporate since they basically include the corrections to the 2D approach arising from forward couplings among loops, as shown in Figure 3. These corrections die off as a power law with distance, so nearest neighbor corrections are what matter.

Loop impedance parameters are frequency dependent. This physical fact complicates the numerical simulations of linear systems in the time domain, since it amounts to solving systems of ordinary differential equations with non constant coefficients, a problem significantly harder than the constant coefficient counterpart. An elegant and simple solution is found by replacing $R(\omega), L(\omega)$ with Foster Pairs [17] as in Figure 4. Each element in the Foster pair is a constant inductor or resistor, whose values are found from fits to a small number of frequencies to $R(\omega), L(\omega)$. The alternative circuit faithfully reproduces the frequency dependent behavior up to the maximum frequencies accessible up to the 18 nm node. Both proximity and skin effects are fully developed in this example.

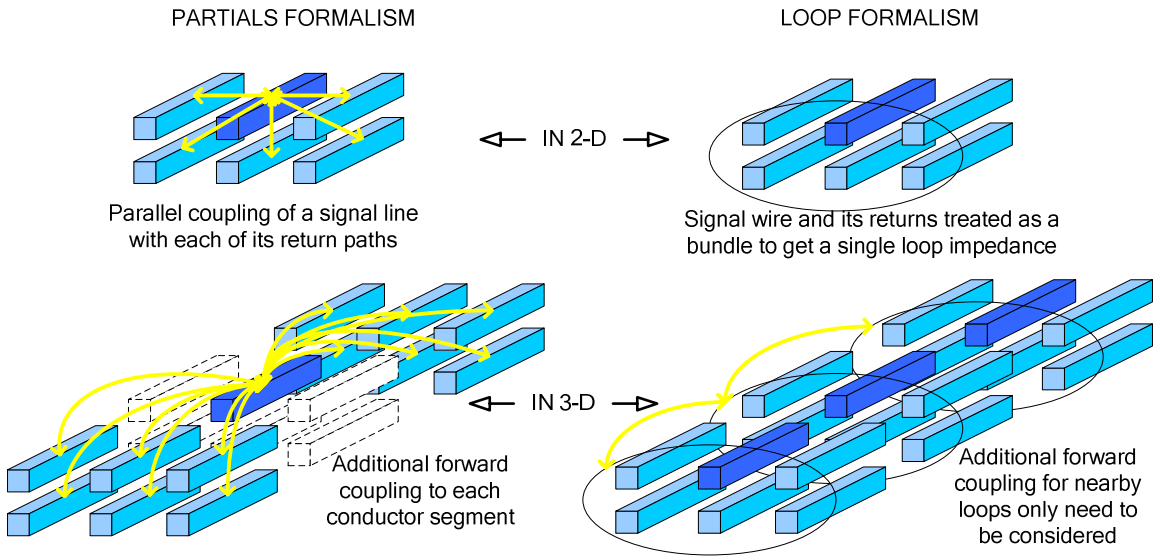

Figure 3: Schematic comparing the partials (PEEC) and loop impedance approaches to inductance extraction, in 2D as well as with corrections due to forward couplings in 3D.

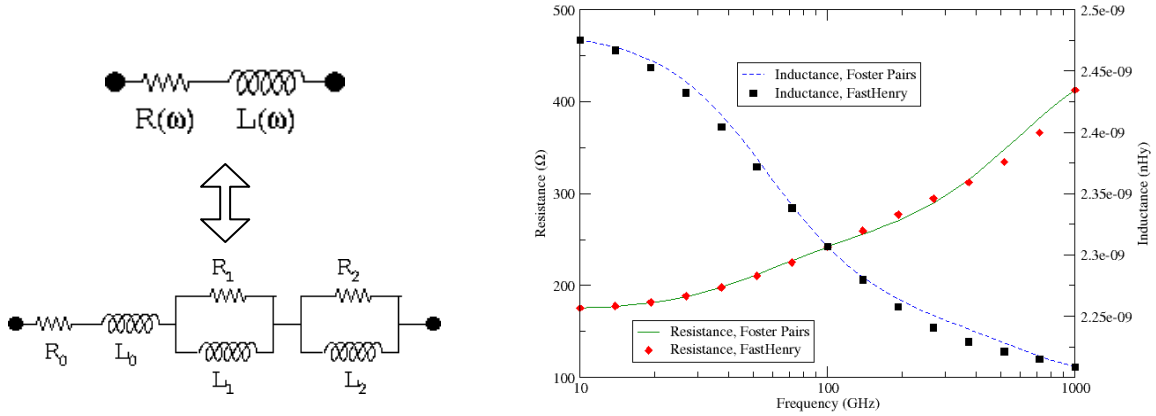

Figure 4: Foster pair representation of frequency dependant RL circuit. The figure at the left shows a typical Foster pair configuration. The plots at the right compare the output of this representative circuit (lines) against FastHenry (symbols).

IV. Frequency Regimes:

To anticipate performance enhancements exclusively due to technology scaling, we compute clock period using fanout-of-four inverters (FO4) delay. It is the right metric, given the property that the ratio of an FO4 delay to the minimal delay for any CMOS family is node independent [18]. We use ITRS 2005 data, and propose as conservative estimate for clock period: 13 FO4 delays as IBM Power6 suggests. In Figure 5 we plot the resulting clock frequencies as a function of technology node. The maximum frequency content of a signal transmitted on an interconnect is given by $f_{\max} \approx 1/\pi T_{rise}$, with $T_{rise} = \tau_{FO4}$ (one FO4 delay). Wires propagate signals in a wide band spectrum up to frequencies near $f_{\max}$. In Figure 5, we present this maximum frequency ($f_{\max}$) as well as clock frequency under these conservative estimates that rely exclusively on technology scaling. These numbers are compatible with a significant slow-down in comparison with the doubling of performance for every node.

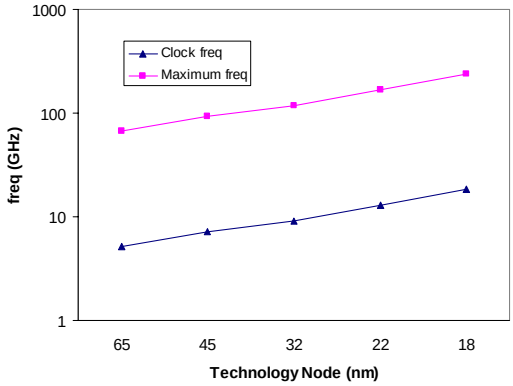

Figure 5: Maximum frequency (corresponding to one FO4 delay) and maximum clock frequency (13 FO4 delays) for a given technology node.

V. Challenges for Nanometer Designs:

Considering high performance digital applications, the accuracy required in wire parasitic extraction is dictated by time delay and noise evaluation. The 50% delay for wires in the RC regime is given by [19]:

$$t_{50\%} = 0.4rcl^2 + 0.7(R_{source}cl + (rl + R_{source})C_{load}) \quad (5)$$

with r and c the per-unit length resistance and capacitance, respectively; l the length of the wire; R_{source} the resistance of the driver; and for FO4 C_{load} the sum of the input capacitance of all inverters (capacitance ratio for the p to n devices Cp/Cn = 2/1).

We first review resistance related challenges in nanometer scale technologies. For local wires in M1 to M3 metal planes, the transverse dimensions under scaling are of the order of the mean free path of electrons in Cu (40 nm at room temperature). For these dimension significant corrections due to surface and ground boundary scattering need to be included. We plot in Figure 6 the percentage of delay due to terms involving wire resistance for local and intermediate wires, with parameters chosen from ITRS 2005 and corrected local resistivity.

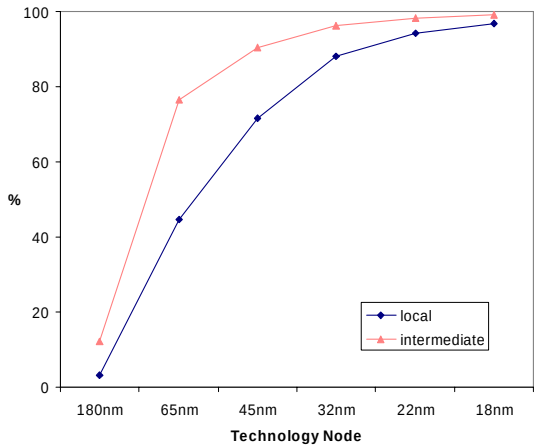

Figure 6: Percentage of RC wire delay influenced by wire resistance.

The large percentage of delay contributed by local wire resistance is a qualitative break when compared to previous technology nodes. At 180 nm, only 5% of the delay was accounted by wire resistance. In fact for local wires the dictum has traditionally been to include only wire capacitance. One could afford a wide margin of latitude in extracting wire resistance. This is no longer tenable even for local wires. High precision wire resistance extraction is demanded. Local wires are the most sensitive to process variations. These corrections must be added to the scattering corrections. The resistance extraction task becomes significantly more complex.

In the process of extracting wire capacitance (total and cross coupling capacitance) for short and intermediate wires, the first order concern that bounds the lengths of these wires can be simply examined using noise considerations. Conservative noise bounds for short wires are given by [20]:

$$\frac{V_n}{V_{dd}} = 0.5 \frac{r\, c_{cc}\, l^2}{T_{rise}} \tag{6}$$

with V_{dd} and V_n the power supply and noise potentials; c_{cc} the per unit length cross-coupling capacitance. The expression is valid when the numerator, diffusion delay is smaller that the denominator. For T_{rise} we use $\boldsymbol{\tau_{FO4}}$, and we bound the noise limit to $V_n/V_{dd} = 0.25$. In Figure 7 we display the restrictions in length due to these noise bounds. Additional care is needed in the extraction of cross coupling capacitance of intermediate wires particularly in the boundary of these noise limits. The forest of wires in M1-M3 follows anything but simple straight line layout. 2D models predictions are expected to be inadequate for critical wires. A solution to tackle the added accuracy requirement is 3D field solver for isolated groups of signal lines. This adds a new dimension to the capacitance extraction demands.

For upper metal layers (M4-M8), electrical noise concerns can be efficiently handled by relaxing the minimum separation requirements. Noise ratios for longer wires become proportional to the ratio of cross coupling capacitance to total capacitance [20]. A router sensitive to this ratio can avoid noise pitfalls. It is better treated by construction rather than extraction followed by simulation. Equation (5) provides an upper bound for timing for semiglobal wires, since they are distributed RC circuits. Setting the delay to say 80 % of the clock cycle identifies repeater demands. It is not accuracy but size complexity that dominates.

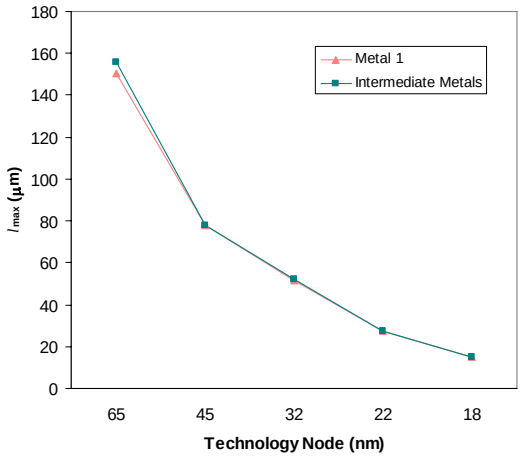

Figure 7: Length limits for local and intermediate wires with maximum noise of $V_n/V_{dd} = 0.25$.

Before analyzing global wires, we provide a brief incursion into design clock boundaries. We first estimate the maximum distance that can be traversed by a signal traveling at maximum possible

speed in a time within one clock period, for the clock frequencies shown in Figure 5. We fix this boundary at a reasonable fraction of the period, say:

$$l_{bound} = 10\tau_{FO4}v \tag{7}$$

with *v* the speed of light in the medium. This figure of merit constitutes a physical limit for communication within 1 clock period. In fact this is one reason for multi-core architectures. Two groups of logic separated by distances longer than l_{bound} cannot be within a clock equipotential [21]. A generous bound of $l_{bound} \sim 3$ mm follows at 18 nm node. At the 18 nm node a sizable embedded processor can fit into such boundary. The presence of such boundary naturally separates global wires into two categories: global and super global ones. The first ones (global wires) can feed signals within a clock equipotential, and the super global wires in between equipotentials. The timing demands on the second category are considerably relaxed. Let us consider a 3mm global wire intended to be used within an equipotential. In Figure 8, we plot the delay for a global wire with scaled parameters ($\omega = 3\lambda$) with and without scattering corrections to the resistivity.

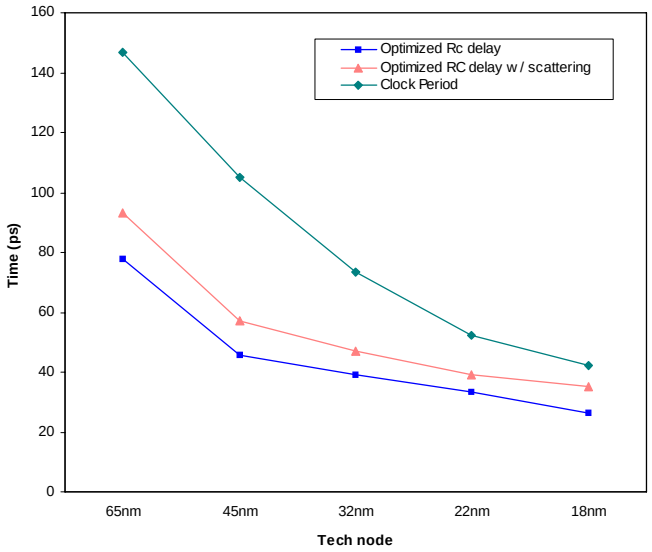

Figure 8: RC delay (with and without scattering effects) for a 3 mm long optimally buffered global interconnect with scaled wires. The clock period at each technology node is shown for comparison.

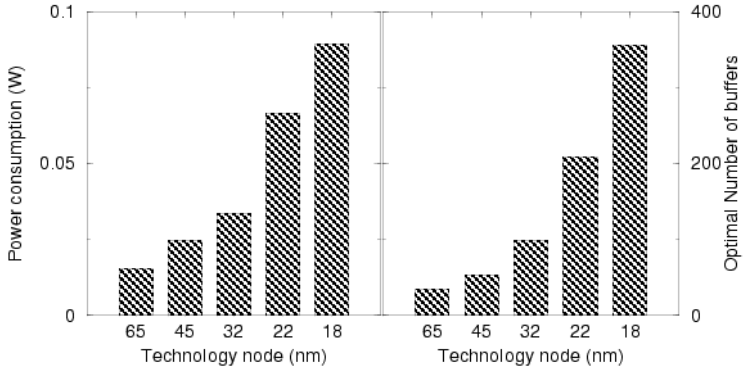

Figure 9: Number of repeaters and their power consumption for optimal delay on a 3 mm scaled RC line (w=3λ).

Figure 8 shows that optimally buffered (RC) wires can transmit signals in less than a clock period for all technology nodes. Thus, with optimal repeater insertion, *RC* scaled wires can satisfy the equipotential boundary. Due to the large resistance of scaled wires, inductance is also not of concern in this scenario [22]. However, the power consumption associated with the large size and large number of repeaters needed to satisfy these delay requirements becomes prohibitive [23]. The number of repeaters needed for optimal delay grows from nearly 25 at 65 nm to nearly 400 at 18 nm node (see Figure 9). Although [23] presents a power-optimal repeater insertion approach to reduce power consumption, this come at the cost of delay which may not be acceptable for critical signals such as the clock. We seek a different solution.

VI. RLC Domain for Scaled and Unscaled Wires - Opportunities:

For wires in the RLC domain (5) is no longer valid. In particular, bounds based on diffusion delay could lead to unphysical signal propagation at speeds larger than the speed of light in the medium. The time delay for a signal in the RLC domain is [24]

$$t_{50\%} = \sqrt{LC} + \frac{T_{rise}}{2} + 0.7 Z_0 C_{gate} \tag{8}$$

With Z_0 the characteristic impedance: $Z_0 = \sqrt{L/C}$. The most important feature of RLC wire propagation is its linear behavior with distance. This implies an economy in repeater insertion. Repeaters are needed to overcome signal attenuation and impedance matching.

The domain boundaries for near speed of light propagation are:

$$l'_{\min} = \frac{T_{rise} v}{2},\ l'_{\max} = \frac{2 Z_0}{r} \tag{9}$$

with *r* the per unit length loop resistance. Consider a sandwich configuration consisting of a scaled signal line between symmetrical ground wires [24]. We plot in Figure 10 the maximum and minimum length bounds for scaled and unscaled wire loops behaving as RLC uniform transmission lines. Evidently, for realistic values of the parameters, scaled wires cannot operate in the RLC domain since the lower length limits becomes longer than the upper limit. The result may seem perplexing were not for the knowledge of the penalty associated with the large resistance of scaled wires. Unscaled wires, on the other hand, satisfy the requirements with ease, as Figure 10 indicates. They can be used for global signals within an equipotential for critical signal and clock propagation.

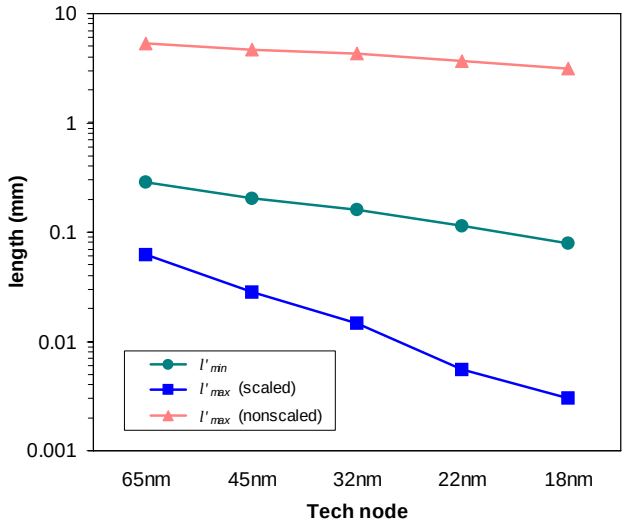

Figure 10: Length restrictions on global wires for RLC transmission.

To understand the advantages of using RLC domain transmission (TEM transmission lines) we compute the ratio of power consumption between a power optimal scaled RC line with repeaters inserted at regular intervals, to the power dissipated in a transmission line by a driver-receiver configuration that ensures large current driving capabilities to permit RLC transmission for that length. The results are shown in Table I. Hence, RLC propagation can be used to save significant amount of power for critical wires such as local clock within an equipotential. Moreover, since these wires by construction are surrounded by symmetrical ground wires, their magnetic coupling to other wires is small. In fact, within the dipole approximation the coupling is zero [24].

Table I: Ratio of power consumption in a 5 mm long optimally buffered scaled RC line to that in an unscaled RLC transmission line.

Node	65nm	45nm	32nm	22nm	18nm
Power consumption ratio (RC/RLC)	4.71	6.4	7.75	14.04	19.83

VII. Some Remaining Concerns and Conclusions:

Process variations in interconnects [5] are a major emerging concern. The various forms of process variation need to be separated into systematic and random components. The systematic variations (CMP, dishing, erosion etc.) must be handled within models; the profile for the variation should be represented analytically for expediency in the computation. In the presence of Capacitance models as, for example, in Equation (1), accounting for process variations is simplified. The extraction of power and ground network is a major challenge, mainly due to limitations in the ability to effectively reduce the size of the resulting electrical database with MOR techniques. The global power distribution wires in the top layers do not scale and for high performance systems and needs to account for Inductance effects. We do not include super global wires, since their timing budget is significantly relaxed. Scaled wires with repeaters, whose number is fixed by latency consideration rather than timing, do not pose new concerns. Power consumption can be significantly reduced by the use of reverse scaling on upper metallization layers for critical signal propagation within a single core logic of length smaller than 3-4 mm.

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